行政院國家科學委員會研究計畫成果報告

計畫題目: 寄生氧化層對具有原子層平坦之超薄氧化層的影響

計畫編號: NSC 88-2215-E-009-033E
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一、 中文摘要

元件的scaling down已經是未來不可避免的趨勢之一。隨著MOSFET中oxide厚度的減小，若想要防止direct-tunneling current density增加，那麼oxide的完整性就很重要。

我們使用一種新的製程技術，用來去除原生氧化層以成長出高品質的gate oxide。利用此技術，我們可以成長出均勻度高、平滑性佳、漏電流低的thin gate oxide。

關鍵詞：均勻度、平滑性、漏電流

Abstract **We have studied the inversion layer mobility of nMOSFET's with thin-gate oxide of 20 to 70 A.Direct relationship of electron mobility to oxide/channel interface roughness was obtained from measured mobility of MOSFET's and high-resolution TEM. By using a low-pressure oxidation process with native oxide removed *in situ* prior to oxidation, atomically smooth interface of oxide/channel was observed by high-resolution TEM for oxide thicknesses of 11 and 38 A. The roughness increased to one to two monolayers of Si in a 55-A oxide. Significant mobility improvement was obtained from these oxides with smoother interface than that from conventional furnace oxidation. Mobility reduction with decreasing oxide thickness was observed in the 20and 35-A oxide, with the same atomically smooth oxide/channel interface. This may be due to the remote Coulomb scattering from gate electrode or the gate field variation from poly-gate/oxide interface roughness.**

keywords : TEM, monolayer and atomically smooth

Introduction

BY continuously scaling the thickness of gate oxide, both the current drive capability and the transconductance of MOSFET's increase [1]-[5]. Current drive more than 1.0 mA/cm2 and transconductance over 1000 mS/mm are reported for deep submicrometer MOSFET's with a 10A direct tunneling oxide [4]. This performance can ensure the transistors to operate at low battery voltage for portable wireless communication [4], [6]. However, the most important issues for MOSFET made by ultrathin gate oxide are thickness uniformity and interface smoothness. The interface roughness can strongly affect the carrier transport that can be characterized by measuring the electron mobility in the inversion layer of MOSFET's [7]-[9]. Furthermore, electron mobility is an important parameter for device modeling and design, and the speed of MOSFET is dependent on the mobility at the low electric field near source. In this letter, we have measured the electron mobility with different interface roughness. Very smooth interface of oxide/St is achieved by desorbing the native oxide in *situ* in a low-pressure oxidation system before thermal oxidation. Atomically smooth interface between oxide and Si is observed by high-resolution TEM for oxide thicknesses of 11 and 38A. The electron mobility dependence on oxide thickness of 20 to 70A was also measured, and a mobility reduction is observed in thinner oxide.

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二、 實驗方法

To reduce the interface roughness of oxide/St, we have designed a low-pressure oxidation system that can desorb native oxide in *situ* before oxidation. A leak-tight reactor design and a high flow rate of hydrogen are used to avoid further growth of native oxide after wafer loading. Similar leak-tight technique and native oxide desorbing process have been used for low-pressure chemical vapor deposition (LPCVD) to grow high quality Si epitaxy at 550C [10]. P-type 4-in [100] Si wafers with typical resistivity of 10 Q-cm are used in this study, and the oxide is grown at 900C using N2O under a reduced pressure of 4.5 torn The advantages of the low pressure oxidation are slow oxidation rate for precise thickness control and good thickness uniformity due to increased N2O migration length. Ultrathin oxide of 11A [Fig. l(b)] can be reproduced and thickness variation less than 1A is obtained across 4-in wafer for a 20A oxide. More detailed growth of ultrathin oxide and process flow will be published elsewhere. High-resolution TEM and 100-1bm wide MOSFET are used to characterize the interface roughness and mobility behavior. To avoid the drain voltage (Vd) bias dependence, the electron mobility was determined from the drain conductance and the gate-channel capacitance at a low Vd of 50 mV [8]. The effective normal field can be expressed as

$$Eeff = (Qinv/2 + QB)/\varepsilon si$$

where Qinv is the inversion layer charge, QB is the bulk depletion-layer charge and ε si is the permittivity of Si.

三、 結論與討論

Fig. l(a) and (b) show the atomic image of a 38- and 11A oxide grown in the low-pressure oxidation system with native oxide removed *in situ.* Atomically smooth interface of oxide/St can be observed in Fig. 1, and only one atomic layer of Si, just beneath the oxide, is disturbed from its original crystal structure. It is noticed that there are only two Si-atomic layers oxidized to form the ultrathin oxide of 11A.

We have also grown oxide from conventional furnace for comparison. Fig. 2(a) presents a ~55A oxide grown by a conventional furnace, where both interface waving and roughness up to four to five layers of Si are observed. In contrast, as shown in Fig. 2(b), the interface of oxide/St is much smoother for the same oxide thickness grown in our system with native oxide removed in *situ.* The local thickness variation up to one to two Si-atomic layers observed in Fig. 2(b) may be due to the increased thermal stress of the thicker oxide than that shown in Fig. 1.

Based on the smooth oxide/St interface, we have therefore studied the electron mobility improvement due to reduced interface roughness. Wafers with low concentration of impurity doping are used to reduce the ionized impurity scattering in the inversion layer, which dominates the low-field mobility. Fig. 3 shows the measured mobilities with 70-A oxide from conventional furnace oxidation and from low-pressure oxidation with native oxide removed *in silu,* respectively. The measured electron mobility from conventional furnace oxidation follows the universal mobility-field dependence reported in previous papers [7]-[9]; however, significant improvement of mobility is measured from our low-pressure oxidation with a clean surface free of native oxide. It is important to note that both wafers from conventional furnace oxide and low-pressure oxide were fabricated at the same time, and they have the same thickness of poly-gate and doping concentrations at source and drain. Therefore the higher electron mobility measured from low-pressure oxide is not process-related. The improved mobility is due to the reduced interface roughness scattering SIIUWII 111 Atlas. I dIIU it, anu Slmllar moDlll~y improvement to interface roughness was also reported for the comparison of thermal and deposited oxide [7].

We have also measured the effective mobility as a function of gate oxide thickness, for oxide thicknesses of 20-, 3s-, and 70-A, respectively. As shown in Fig. 4, a mobility decrease in the low gate-field region is observed for the 20and 3s-A oxide as compared to the 70-A one. It is well know that the total electron mobility is governed by individual contributions from phonons, channel doping impurities and interface roughness, where the Coulomb scattering from doping impurities dominates the low-field mobility and the interface roughness dominates the high-field mobility [8], [9]. Therefore interface roughness scattering limits the mobility of modern deep submicrometer devices even though the channel doping is higher than that used in this work [7]. Because the same resistivity of substrates are used, the reduction in low-field mobility

is not due to the different concentrations of impurities. Although the decay of mobility as decreasing oxide thickness is generally explained by the over-estimation of inversion carrier concentrations in thin oxides [2], [11], other possibilities such as Coulomb scattering from remote charge at poly-gate or the poly-gate/oxide interface roughness may also be responsible to the mobility degradation. The remote charge scattering is due to poly-gate depletion [12] and is well known in III-V modulation-doped FET and was also predicted in [13] and [14]. The interface roughness of polygate and oxide, shown in Figs. 1 and 2, may also contribute local gate field variation [15], [16] and provide additional scattering mechanism to reduce the mobility at thin oxide.

Conclusion

In conclusion, we have shown direct relationship of electron mobility to oxide/channel interface roughness. Significant mobility improvement is obtained from a smoother interface with *in situ* removing native oxide prior to oxidation. Atomically flat interface of oxide/channel can be obtained by this method for oxide thickness in the range of 20-38 A. Mobility reduction with decreasing oxide thickness was observed in the 20- and 35-A oxide, with the same atomically smooth oxide/channel interface. This may be due to the remote Coulomb scattering from gate electrode or the gate field variation from polygate/oxide interface roughness.

四、 參考文獻

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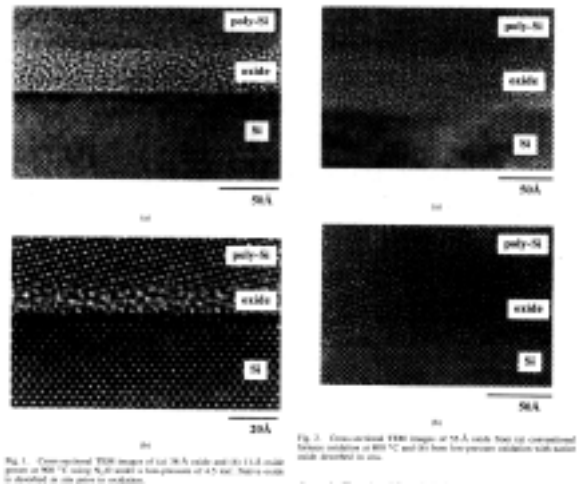
Figure Captions:

Fig1. Cross –sectional TEM images (a) 38A oxide and (b) 11A oxide grown at 900C using N2O under a low pressure of 4.5 Torr. Native xoide is desorbed *in situ* prior to oxidation.

Fig2. Cross –sectional TEM images of 55A from (a) conventional oxidation at 800C and (b) from low-pressure oxidation with native oxide desorbed *in situ.*

Fig3.Electron mobilities of MOSFET's with 70A oxide from conventional furnace oxidation and from low-pressure oxidation with native oxide desorbed *in situ.*

Fig4. Electron mobilities of MOSFET's as a function of effective field of (a) 70A (b) 35A and (c) 20A oxide from low-pressure oxidation with native oxide desorbed *in situ*.



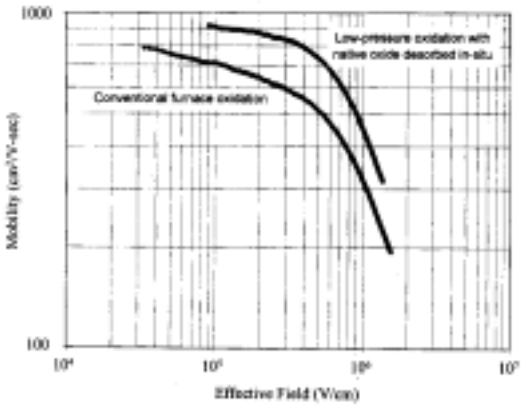


Fig. 3. Electron mobilities of MOSFET's with 70-Å oxide from conventional furnace oxidation and from low-pressure oxidation with native oxide desorbed *in situ*.

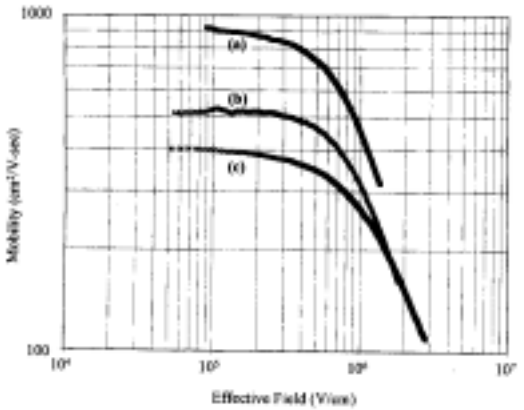


Fig. 4. Electron mobilities of MOSFET's as a function of effective field of (a) 70 Å, (b) 35 Å, and (c) 20 Å oxide from low-pressure oxidation with native oxide desorbed *in situ*.