High-Performance Nanowire TFTs With Metal-Induced Lateral Crystallized Poly-Si Channels

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***Abstract*—High-performance poly-Si thin-film transistors (TFTs) with 50-nm nanowire (NW) channels fabricated by integrating a simple spacer formation scheme and metal-induced-lateral-crystallization (MILC) technique are proposed. By using the sidewall spacer formation scheme, the NW channels with nanometer-scale feature sizes can be easily fabricated, exhibiting superior channel controllability through the triple-gate structure. In employing the MILC technique, the grain crystallinity of NW channels is significantly superior to that formed by the solid-phase-crystallization (SPC) technique. Therefore, the MILC NW TFT exhibits greatly improved electrical performances, including lower threshold voltage, steeper subthreshold swing, and higher field-effect mobility, as compared to those of the SPC NW TFT. Moreover, the superior threshold-voltage rolloff characteristics of MILC NW TFT are also demonstrated.**

***Index Terms*—Metal-induced lateral crystallization (MILC), nanowires (NWs), thin-film transistors (TFTs), triple-gate structure.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) have been a promising technology for the application of active-matrix liquid crystal devices (AMLCDs) and 3-D integration [1], [2]. To improve the performance of poly-Si TFTs, several advanced crystallization techniques such as excimer-laser annealing (ELA) [3] and metal-induced lateral crystallization (MILC) [4]–[6] have been developed to produce high-quality poly-Si films with large grain sizes and low microstructural defect densities. However, the most widely used ELA technique still has many issues to be addressed for further development. The MILC technique is a low-cost batch process and is also attractive for obtaining needlelike poly-Si grains with grain boundaries that are parallel to the crystallization direction. Although considerable grain length can be obtained by MILC, the grain width achieved is still smaller than the device channel width, which cannot realize nearly single-grain TFT devices. Poly-Si TFTs constructed from nanowire (NW) channels [7], [8] or specific gate structures [9]–[11] have been proposed to improve the device performance by reducing the effects of grain boundaries or enhancing the gate controllability over channel potential, respectively. However, the application of TFTs with specific channel or gate structures are restricted by costly electron beam lithography technology or complicated fabrication processes, which could not be practicable in flat panel displays. Additionally, a poly-Si NW TFT with a side-gate structure would suffer from an undesirable gate-induced drain leakage (GIDL) current and must be resolved by additional processes [8]. Recently, we have proposed a simple spacer formation technique to fabricate poly-Si NW TFTs with top-gate planar structures [12], which addressed the issues mentioned previously. However, the solid-phase crystallized (SPC) poly-Si film still has a large amount of randomly oriented grain boundaries, inevitably degrading the device performance [13].

In this letter, novel poly-Si TFTs with NW channels crystallized by the MILC technique have been successfully fabricated and characterized. The fabricated NW channel with a 50-nm linewidth, which is the smallest reported channel width in planar TFTs to date, can reduce the effects of grain-boundary defects. Therefore, fabricating NW TFT with the entire channel region in a single-crystal grain is realizable, which accompanies improved channel controllability through the triple-gate structure. This fabrication process is very simple, low cost, and suitable for system-on-panel applications.

II. Device Fabrication

The key fabrication steps and the schematic top view for the proposed MILC NW TFT structure are shown in Fig. 1(a), (b), and (c), respectively. First, a 150-nm SiN_X and a 100-nm tetraethooxysilane (TEOS) SiO_2 were deposited by a plasma-enhanced chemical vapor deposition (PECVD) system to serve as the starting substrate and the dummy oxide layer, respectively. After patterning and etching to be the dummy oxide stripe, a 100-nm amorphous silicon (α-Si) layer was conformally deposited by low-pressure CVD (LPCVD) at 550 °C and then anisotropically etched to form a square-coil α-Si sidewall spacer [Fig. 1(c)] in a self-aligned manner. The feature size of the α-Si spacer could be readily shrunk into nanoscale dimension without advanced photolithography technology and could be well controlled by the dry etching condition. Next, a 200-nm low-temperature oxide (LTO) was deposited and patterned to expose the MILC window [Fig. 1(a)]. A 10-nm nickel (Ni) layer was deposited, and lateral crystallization was subsequently carried out at 550 °C for 24 h in N_2 ambient.

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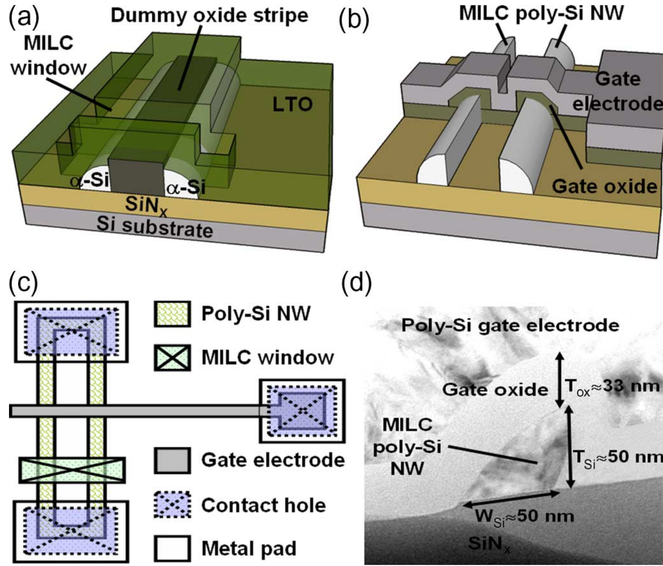


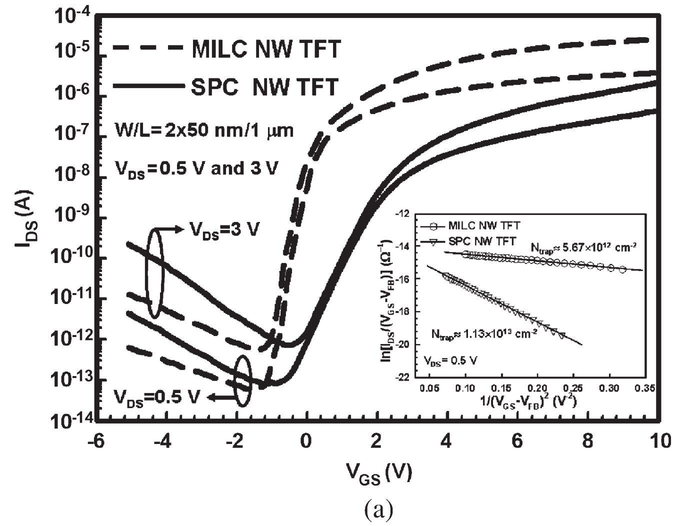
Fig. 1. (a)–(b) Key fabrication steps and (c) schematic top view for the proposed MILC NW TFT. (d) Cross-sectional TEM image of the MILC NW TFT structure.

After the MILC process, the remaining Ni and LTO as well as the dummy oxide stripe were etched away by hot sulfuric acid and hydrofluoric acid, respectively. Then, a 33-nm TEOS gate oxide and a 250-nm n^+ poly-Si were deposited and patterned to form the gate electrode [Fig. 1(b)]. Next, a self-aligned phosphorus ion implantation was performed at 15 keV to a dose of 5×10^{15} cm^{-2} to dope the source/drain region, followed by the dopant activation at 600 °C for 12 h in N_2 ambient. Finally, a typical passivation layer deposition, contact hole opening, and metal pad formation completed the device fabrication. For comparison, the control SPC NW TFT crystallized at 600 °C for 24 h in N_2 ambient was also prepared. To study the impacts of grain boundaries on TFT performance, no additional hydrogenation or sintering processes were performed.

III. Results and Discussion

Fig. 1(d) shows the cross-sectional transmission-electron-microscopy (TEM) image of the proposed NW TFT with an MILC poly-Si channel. Both the vertical sidewall thickness (T_{Si}) and the horizontal width (W_{Si}) are approximately 50 nm. Such high aspect ratio ($T_{\mathrm{Si}}/W_{\mathrm{Si}} \approx 1$) of NW TFT has the advantage of forming a triple-gatelike structure with well electrostatic controllability on the NW channel potential due to the sidewall and corner contribution effects [14].

Fig. 2(a) shows the typical transfer characteristics of the proposed NW TFTs with MILC and SPC poly-Si channels at $V_{\mathrm{DS}} = 0.5$ and 3 V. The TFT device composed from a couple of NW channels has a nominal channel length (L) of 1 μm and an effective channel width (W) of 100 nm ($2 \times W_{\mathrm{Si}}$). The threshold voltage (V_{TH}), subthreshold swing, and field-effect mobility were extracted at $V_{\mathrm{DS}} = 0.5$ V, whereas the maximum off-state GIDL current ($I_{\mathrm{GIDL,max}}$) and on/off current ratio ($I_{\mathrm{on}}/I_{\mathrm{off}}$) were extracted at $V_{\mathrm{DS}} = 3$ V. The threshold voltage was defined as the gate voltage required to achieve a normalized drain–current of $I_{\mathrm{DS}} = (W/L) \times 100$ nA. The



(a)

Key parameters	SPC NW TFT	MILC NW TFT
Threshold voltage, V_{TH} (V)	2.7	0.1
Subthreshold swing, S.S. (mV/dec.)	594	199
Field-effect mobility, μ_{FE} (cm^2/V-s)	42	156
Maximum GIDL current, $I_{GIDL,\ max}$ (A)	2.39×10^{-10}	1.18×10^{-11}
On/off current ratio, I_{on}/I_{off}	3.2×10^6	4.7×10^7

(b)

Fig. 2. (a) Comparison of transfer characteristics for the MILC and SPC NW TFTs with $L = 1$ μm and $W = 2 \times 50$ nm. The inset shows $\ln[I_{\mathrm{DS}}/(V_{\mathrm{GS}} - V_{\mathrm{FB}})]$ versus $1/(V_{\mathrm{GS}} - V_{\mathrm{FB}})^2$ curves at $V_{\mathrm{DS}} = 0.5$ V and the extracted effective trap state density. (b) Comparison of device characteristics for the MILC and SPC NW TFTs.

key device parameters are shown in Fig. 2(b). Accordingly, the threshold voltage and the subthreshold swing of the MILC NW TFT are 0.1 V and 199 mV/dec, respectively, which are superior to 2.7 V and 594 mV/dec of the SPC NW TFT. Notably, the maximum GIDL current of the MILC NW TFT is more than one order in magnitude lower than that of the SPC NW TFT. The on/off current ratio of the MILC NW TFT (4.7×10^7) is much higher than that of the SPC NW TFT (3.2×10^6). Additionally, the MILC NW TFT has an obvious enhancement in the maximum field-effect mobility from 42 to 156 $\mathrm{cm}^2/\mathrm{V \cdot s}$, as compared to the SPC NW TFT. Note that the major performance improvements in the MILC NW TFT are due to the alignment of poly-Si grains in a direction that is parallel to the current flow. Also, the growth of poly-Si grains perpendicular to the channel direction is effectively limited by the nanoscale channel width of 50 nm. Therefore, the effects of parallel grain boundaries could be relieved by decreasing the channel width to be comparable to or even smaller than the poly-Si grain size. However, the grain boundaries are randomly oriented in the SPC NW TFT.

In order to verify the reduction of grain-boundary defects in the MILC poly-Si, the effective trap state density (N_{trap}) was calculated from the square root of the slope of $\ln[(I_{\mathrm{DS}}/(V_{\mathrm{GS}} - V_{\mathrm{FB}})]$ versus $1/(V_{\mathrm{GS}} - V_{\mathrm{FB}})^2$ plot, which was proposed by Proano *et al.* [15], as shown in the inset of Fig. 2(a). It is observed that the MILC NW TFT shows a much reduced

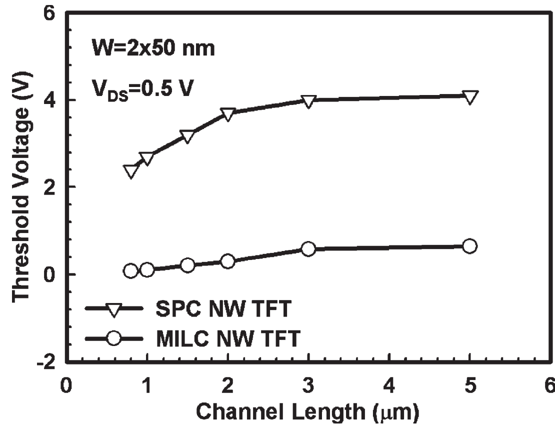


Fig. 3. Threshold-voltage rolloff properties of the MILC and SPC NW TFTs with channel lengths (L's) varying from 5 μm to 0.8 μm; the channel widths (W's) are kept at 2×50 nm.

effective trap state density from 1.13×10^{13} to 5.67×10^{12} cm^{-2} as compared to the SPC NW TFT. This figure strongly implies that the MILC technique can obtain a good-quality poly-Si film with a larger grain size and fewer microstructural defects.

Additionally, to examine the grain crystallinity of poly-Si NWs with different crystallization techniques, the threshold-voltage rolloff properties of the MILC and SPC NW TFTs are shown in Fig. 3. Apparently, the SPC NW TFT exhibits a serious threshold-voltage rolloff property, which is dominated by the decrease of randomly distributed grain boundaries contained in the channel [16]. However, a much more improved scaling characteristic is observed in the MILC NW TFT, which could be ascribed to the fabrication of an entire device on a nearly single-crystal grain; therefore, compared to the SPC NW TFT, the MILC NW TFT could not only relieve the effects of grain boundaries but also achieve a lower threshold voltage.

IV. Conclusion

We have proposed a novel high-performance poly-Si TFT with 50-nm NW channels crystallized by the MILC technique. The experimental results show that the proposed MILC NW TFT not only depicts improved turn-on characteristics by forming good-quality poly-Si films as well as superior triple-gate controllability over the NW channel potential but also maintains a low off-state leakage current by reducing the microstructural defects. Superior short-channel characteristics are also achieved, which might be explained by the formation of single-crystal grains in the entire channel region. Therefore, the proposed MILC NW TFT could be indeed suitable for implementing low-cost, high-density, and high-performance driver circuits on the glass panel for AMLCD applications.

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