對以智財單元為基系統晶片設計之驗證與測試技術開發研究
Verification and Testing Technology Exploitation for IP-Based SOC Design

計畫編號：NSC 90-2215-E-009-082
執行期限：2001 年 8 月 1 日至 2002 年 7 月 31 日

主持人：李崇仁教授　交通大學電子工程系
共同主持人：董蘭榮教授　交通大學電機與控制工程系
陳竹一教授　中華大學電機系

一、中文摘要

以系統晶片來實現複雜的系統已成為積體電路設計的主要趨勢。系統晶片的設計一方面要利用強大計算機輔助設計整合多個智財(IP)單元於單一的系統晶片上，另一方面要驗證設計結果以符合系統要求。為達成後者目的需要有強大有效之驗證測試系統。本研究團隊基於多年研究積體電路驗證測試技術的經驗提出此計畫以開發出完整的系統晶片驗證測試技術。

本計劃第二執行年度分成三子計劃，分別為：(1)於組織探索階段互動之系統階層驗證技術；(2)以智財為基系統晶片設計之測試技術研究；與(3)系統晶片矽晶偵錯之良率提昇。分別於系統階層驗證、IP 單元測試、與元件偵錯三層面上發展驗證、測試、偵錯與良率提昇技術，以減少再設計週期。藉由探討此三個部分的驗證技術及相互間的分工整合建構成一套具實用性的系統晶片驗證測試偵錯技術。

關鍵詞：系統晶片、驗證、測試、偵錯、超大型積體電路/計算機輔助設計、良率

Abstract

To use an SOC (System-On-a-Chip) realize a complex system has become the main trend for today's IC design. To design an SOC, in one hand, it needs to have a powerful CAD system to incorporate many IP's into one single chip; in the other hand, it needs to verify the designed system and test the finally fabricated chip to guarantee its proper function and performance. To achieve the latter goal, it needs to have a powerful and effective verification, testing and debug system. In view of this, this integrated joint project is proposed to investigate the verification, testing and diagnostic technology for the SOC design.

The project, to be carried out in three year period, has three sub-projects in the second year, which are : (1) system-level verification interacting with architecture exploration; (2) Testing technology development for IP-based SOC design; and (4) SOC silicon diagnostics and yield improvement. It is dedicated to investigate the verification, testing and debug techniques at three levels, i.e., system level, IP-level and silicon wafer debug of SOC design. The final aim is to develop a complete and practical verification and testing system for SOC design.

Keywords: SOC, Verification, Testing, Diagnosis, VLSI/CAD, Yield

二、緣由與目的

系統晶片的設計一方面要整合多個智財(IP)單元於單一的系統晶片上，另一方面要驗證設計結果以符合系統要求。合成智財單元與整合系統晶片的過程繁複已屬不易，而要確認該系統晶片製造完成後，是否能正確地運作則是更大的挑戰。目前學術及產業界大多投入於系統晶片的開發設計上，對於系統晶片的驗證測試技術則著墨不多。鑑於此，本研究團隊提出此計畫以開發出完整的系統晶片驗證測試技術。

系統晶片設計通常採用由上而下的

流程，分為 System-Level Design，Circuit-Level Design 以及 Manufacturing，在每一層次設計均產生 intermediate 設計結果供下一層次之設計使用。在每進入下一個層次之前，必須先確認設計結果之正確性與其之可測試性。我們所提出一套結合設計流程的驗證程序，分階段地：即 System level, Circuit level 及 Manufacturing level 完成系統晶片的驗證工作及產生測試偵錯圖樣(test and diagnostic patterns)。

第一階段主要是由第一子計畫執行，其主要工作是成本評估、效能模型、軟硬體共模擬。此計畫首先就耗電功率、面積、延遲時間三項因素來評估系統之組織成本。根據與系統組織配置的設計階段互動，一方面驗證該組織是否符合系統要求、一方面提供組織配置的設計參考。此步驟完成後，再在效能抽像階層上模擬候選組織。在此階層的模型不強調實際的資料值而僅考慮系統內的資料流動。因此，由於模型複雜度的簡化縮短模擬時間。而設計者依據時間性效能的模擬結果驗證候選組織並進而改善設計。完成此二步驟後，軟硬體共模擬開始就包含軟、硬體元件的異質組織實施模擬以驗證系統晶片行為結果。至此，系統階層驗證便告完成。此時將再進行下列階段 Circuit-level 之驗證。

第二階段主要是由第二子計畫執行。於 SOC 設計過程中，除各層次之設計驗證外，為保證系統晶片製造出來時，無因製程缺陷等因素而發生不能工作情況，必須加入可測試性設計之考慮，並對各 IP 產生其測試與偵錯圖樣。晶片測試，長久以來即是一困難問題。於系統晶片設計中，由於晶片之規模是更大而複雜，且其中許多 IP，皆是由不同公司或設計者提供，所設計出來之晶片測試問題更是嚴重。又未來之系統晶片，必是屬混合信號(mixed-signal)，其製造技術亦必是以深次微米為主之技術，其信號傳輸是以奈秒(nano-seconds)(甚至以下)為單位。對於此種晶片，有一些新的現象，如：信號於 interconnection wires 傳輸所花費時間將超過於 MOSFET 電晶體傳輸所花費時間，interconnection wires 間之信號干擾現象嚴重，MOSFET 漏電流增大等，晶片測試需要有新的考量。

故第二子計畫：擬在下列三方向對 SOC 晶片測試之諸問題，作一研究：(1) 數位與類比 IP 之測試與驗證；(2) 深次微米連接線之測試；(3) 以統計方法研究深次微米 VLSI 測試。其中第一項係於 gate 或 circuit level 對各類 IP 研究其測試方法，特別是採用自我測試之方式；第二項係針對未來 SOC 必是將許多 IPs 用連接線連接，此連接線會因次微米而有一些如上所述現象，其測試值得研究；第三項係因深次微米晶片，其功能受製程參數影響甚大，處理測試問題已不可循往常固定值之測試觀念，而必須以統計方式處理。

於第三晶片製造階段，由於製程初始之 immature tuning，所生產之晶片良率必低，或於晶片測試時發現晶片不符規格，必須經由晶片偵錯，甚或設計偵錯，發現原因，而提升晶片生產良率。此時甚或需全面檢討晶片設計，以求達到最符經濟效率的測試與晶圓良率，此階段工作係由第三子計畫執行。其於矽晶片製造完成後，就其測試資料，即 wafer map，尋求設計、測試與製造流程之缺失，並藉統計理論分析良率以增進晶片良率與提升晶片品質。另外亦欲以系統分析方式研究系統晶片之整個設計、測試與製造的流程，以改進晶片良率與提升晶片品質。最後此子計畫更擬研究系統晶片之 Test Economics，希望能建構一軟體系統，考量各 IP 特性與測試機之規格與限制，對一系統晶片之測試成本效益能有一預估並做最佳化。

由上所述可知，各子計畫於本整合計畫各佔地位且環環相扣，互為幫補。計畫之完成將對國內 SOC 驗證及測試技術之提升有幫助。

三、結果與討論

(1) System-level verification interacting with architecture exploration:

In this sub project, The system-level

co-simulation technology described in this report has been validated successfully on several applications, and at different design stages of several telecommunications and multimedia products. We have applied our wrapping technology on a H.263 CODEC, an ADSL application, a High-Density Central Site Modem (HDSM), and an MPEG-4 decoder. In all cases, we had to deal with in-house and third-party IP cores. Some of the in-house IP cores were still under development, and our wrapping scheme helped plug them into the system prior to, or upon, their completion. It also helped us, when we started developing the wrapping scheme, to work first on in-house IP cores. This gave us the opportunity to develop the API functions for the cores ourselves, after collaboration with the (in-house) IP core designers.

Besides, a wrapping technology for hardware/software co-simulation is proposed. It includes three phases: (1) *Initialization phase*. (2) *Execution phase*. (3) *Termination phase*. Our hardware/software co-simulation technology is verified to be an efficient and fast way to run heterogeneous cosimulation, and quickly incorporate foreign IP cores into embedded systems. Substantial productivity gains and design-time reductions have resulted from its use. In a high-density central site modem (HDCSM) application, we have been able to wrap several in-house IP cores and set up a heterogeneous cosimulation system platform in less than two weeks. This includes the development of the API functions for the IP cores, and the interaction models with the system. We have developed and tested the heterogeneous cosimulation IP models with little knowledge about the cores themselves. Applying different speedup techniques, we have been able to accelerate the heterogeneous system cosimulation substantially (often by three orders of magnitude). For example, we have been able to speed up the system simulation of the HDCSM application from three instructions per second (RTL) to 1600 instructions per second. Thus far, the IP-based synthesis technology is only partially automated. The communication layer and the client/server interfaces are generated automatically. However, the designer's assistance is needed to define the interaction model, and the API functions.

(2) Testing technology development for IP-based SOC design:

For the second year of the sub-project, there are four topics under investigation. For all the topics, significant progress has been obtained and some of results are being or have been written into papers for publication:

2.1 "Signal induced coupling fault testing for IP interconnection wires"

In this work, we propose a test scheme to test crosstalk faults. It uses an oscillation signal applied on an affecting line and detects induced pulses on a victim line if a crosstalk fault exists between these two lines. It is simple and eliminates the complicated timing issue during test generation for the crosstalk fault. The scheme is very simple and easy to be implemented. Two test generation approaches, i.e., the guided random test generation and the deterministic test generation are described and experimental results are presented. The experimental results show that the proposed test generation approach, i.e., it first uses the guided random test generation then a deterministic approach can effectively generate crosstalk fault test patterns for circuits. Some results of this work have been presented in ATS'2002 [1].

2.2 "Test tolerance on observation signature for analog signal IP circuit testing"

In this topic, we have presented a structure-based specification-constrained test generation method which starts with derivation of the relationship between the specifications and the device and/or component parameters, and it then considers variations of component parameters due to fabrication process fluctuation by using a statistical model. The relationship between the observed signature and the parameter may

be monotonic or non-monotonic. A criterion that combines signature sensitivity and input-output transfer factor is used to generate test patterns for monotonic type parameters. For non-monotonic type parameters, test generation with the aim of reducing the degree of misclassification has also been proposed. Simultaneously, a tolerance range that corresponds to the limitations imposed by the specifications is obtained. An example circuit has been used to demonstrate the test generation procedure and to show the effectiveness of the generated test frequency in increasing the observability and reducing the degree of misclassification. Besides, we have written several papers based on this work [2, 3].

2.3 “Specification reduction for analog IP testing”

In this topic, we have presented an approach to reduce the number of test specifications for analog circuits. It starts with derivation of the relationship between specifications and device and/or component parameters then defines upper and lower bounds for parameters to find essential test specifications. Then the variations on component parameters due to fabrication process fluctuations are considered by using a statistical model to reduce test specifications with a testing confidence probability. A continuous time state-variable filter example circuit has been used to demonstrate the specification reduction procedure and it has been shown that 2, 3 or 4 out of 10 specifications can be ignored during specification testing under the 99%, 90% and 50% testing confidence level respectively. The procedure is effective and can be used in manufacturing specification test for analog circuits to reduce test time. Besides, several papers based on this research work have been presented [4, 5].

2.4 “Analog PLL IP testing and diagnosis”

In this topic, we have presented a design for diagnosis scheme which make the PLL output a periodic signal through the use of some extra circuit. This enhances the conveniences to observe signals under test. In addition, the design for the PLL diagnosis proposed is simple but efficient in identifying representative faults for the PLL during the manufacturing stage when the PLL does not oscillate or meet the performance specifications. Some results of this work have been presented in IMSTW [6].

(3) SOC silicon diagnostics and yield improvement:

茲將本年計畫達成規劃書所列的目標之五項工作，分述於下：

3.1 完成針對可分割電路模型容忍分析之新穎規劃。

3.2 完成多次測試對良率和品質的改善。

3.3 完成高效能序列匯流排(IEEE 1394-1995)之傳輸品質分析。

3.4 完成元件匹配特性在空間上的相關分析。

3.5 完成適用於規格分析之多變量密度表達。

四、計畫成果自評

子計畫一：本計畫第二年已建立軟硬體共模擬環境，可有助於組織探索階段完成軟硬體互動之驗證工作。本計畫之研究成果已發表下列兩篇國際會議論文與一篇國內會議論文[1-3]。另外，部分研究成果正投稿于 IEEE 期刊。

經由本計畫之執行已培養四名碩士畢業生。該四名碩士畢業生目前服務於系統晶片相關之高科技企業。

子計畫二：本計畫於第一年已建立智財單元本身與相互間連線的測試機制，在本執行年度(第二年)的期間也順利地分別對數位、類比與混合訊號電智財單元提出有效的測試與診斷的架構與方法，相信將有助於後續計劃之執行。大部分的研究成果皆符合吾人原提計劃，完成度應達 90%以上，且部分成果已發表於國際之期刊[4-9]。

子計畫三：本計畫研究內容與原計畫目標相符，尤其是在類良率模型的建立，以此模型所做的良率評估，可使吾人分段模擬，其結果幾乎與不分段一致；另外對於不同規格參數轉換的探討，不僅可用於設計時做最佳化之指引(尤其是高靈敏度電路如:高速數位電路、類比電路、高頻電路)，亦可用於測試圖樣產生時最佳測試參數選取以及測試圖樣減少的指引，亦可用於晶片測試時做為晶片診斷的指引。是以本計畫在這一年度的工作中，獲得豐碩的成果，亦在許多項目上值得繼續延伸。

五、參考文獻

[1] Ting-Hsun Wei, Shiuh-Rong Huang, and Lan-Rong Dung, 2002, "An Automated IP Synthesizer for Limited-Resource DWT Processors," ICASSP 2002.

[2] Shiuh-Rong Huang and Lan-Rong Dung, 2002, "A MAC-level Synthesis of Resource-Constrained DWT SIP," VLSI/CAD Symposium 2002.

[3] Shiuh-Rong Huang and Lan-Rong Dung, 2002, "VLSI Implementation for MAC-Level DWT Architecture," ISVLSI 2002.

[1] M. S. Wu, C. L.Lee, C. P. Chang and J. E Chen, "A Testing Scheme for Crosstalk Faults Based on the Oscillation Test Signal," *The 11th Asian Test Symposium*, Session 4A-2, 2002

[2] Soon-Jyh Chang, Chung Len Lee and Jwu E Chen, "Structure-Based Specification-Constrained Test Frequency Generation for Linear Analog Circuits," accepted for publication in Journal of Information Science and Engineering.

[3] Soon-Jyh Chang, Chung Len Lee and Jwu E Chen, "Structure-Based Specification-Constrained Test Frequency Generation for Linear Analog Circuits," *IEEE International Mixed-Signal Test Workshop*, pp.109-117, 2002.

[4] S. J. Chang, C. L. Lee and J. E Chen, "Structural Fault Based Specification Reduction for Testing Analog Circuits," *Journal of Electronic Testing: Theory and Applications*, pp.571-581, 2002.

[5] S. J. Chang, C. L. Lee and J. E Chen, "Structural Fault Based Specification Reduction for Testing Analog Circuits," *IEEE European Test Workshop*, pp.261-266, 2002.

[6] J. W. Lin, C. L. Lee and J. E Chen, "A Design for Diagnosis Scheme for the PLL," *IEEE International Mixed-Signal Test Workshop*, pp.5-8, 2001.