Realization of ambipolar pentacene thin film transistors through dual interfacial engineering

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Realization of ambipolar pentacene thin film transistors through dual interfacial engineering

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Ambipolar conduction of a pentacene-based field-effect transistor can be attributed to dual interface engineering, which occurs at the dielectric/semiconductor interface and electrode/semiconductor interface. While the former was realized by utilizing a hydroxyl-free gate dielectric, the latter was made feasible by the use of appropriate metal source and drain electrodes. The field-effect hole and electron mobilities of 0.026 and 0.0023 $cm^2/V\,s$, respectively, were extracted from the transfer characteristics of pentacene organic field-effect transistors utilizing polymethyl methacrylate as the trap-reduction interfacial modified layer and Al as the source and drain (S/D) electrodes. We demonstrated a complementarylike inverter by using two identical ambipolar transistors and it can be operated both in the first and third quadrants with a high output voltage gain of around 10.
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I. INTRODUCTION

For the next-generation electronics and circuits, organic field-effect transistors (OFETs) are the key elements because of their extraordinary advantages, such as low cost, large-area coverage, mechanical flexibility, and low-temperature fabrications. The performance of OFETs has already reached the level of hydrogenated amorphous silicon, which has been widely adopted in numerous practical applications.[1] The development of organic complementary technology demands the coexistence of both *p*- and *n*-type transistors to achieve efficient operational stability. For example, the inverter, which is usually a basic building block of organic integrated circuits, consists of *p*- and *n*-channel transistors. It is one of the most important and basic elements for the complex integrated circuits. In order to simplify the fabrication process, ambipolar OFETs employing a double-layer scheme and bulk-heterojunction configuration have been utilized to achieve complementarylike inverters.[2–5] However, the feasibility of such devices demands an additional deposition step and some critical fabrication conditions.[6,7] An additional drawback observed in those ambipolar systems is that the organic semiconductors utilized as the active channel layers exhibited poor crystallinity while stacking or blending them together. Perhaps, it will be more advantageous if the ambipolar conduction could be achieved without any stacking or bilayer scheme during the deposition of active layer. Thus, ambipolar FETs with sole organic semiconductor layer have to be addressed for ease of circuit design and simplification of the fabrication process and are able to operate both in the first and third quadrants.[8,9]

The unipolar transport is usually observed in organic semiconductors and thus most of the reports demonstrated that organic transistors typically operate as either *p*- or *n*-channel devices.[10,11] For instance, *n*-type transport characteristics have been recently revealed in the pentacene OFETs; however, this observation was achieved at the cost of *p*-type conduction.[12–14] Moreover, Ahles *et al.*[15] utilized the interface-doped method to reduce the electron traps at interface and thus to form the *n*-channel FETs. Besides, Chua *et al.*[16] also demonstrated the *n*-channel OFET operation with various *p*-type conjugated polymers by using a hydroxyl-free gate dielectric. One of the reasons for such a unipolar transport in these devices is mainly due to the energy mismatch between the molecular orbital of semiconductor and the work function of metal. Hence, there is a demand to find a surface energy match between the gate dielectric and the organic layer, which could possibly result in the ambipolar phenomena. On the other hand, ambipolar transport characteristics have been recently demonstrated in an organic heterostructure by utilizing asymmetric source and drain electrodes.[17] An alternative approach to achieve such a phenomenon is to utilize a low bandgap or high electron affinity organic semiconductors.[18,19] Therefore, in the operation of ambipolar OFETs, charge carrier transport not only depends on the semiconductor/dielectric interface, but also on the metal/semiconductor interface.

Keeping in view of the aforementioned facts, in this article, we succeed in achieving the ambipolar pentacene FETs by interface engineering. The improved performance is primarily attributed to the reduced electron traps at SiO_2/semiconductor interface by incorporating an interfacial-modified layer made of polymethyl methacrylate (PMMA). Additionally, the metal with a suitable work function as source/drain (S/D) electrodes also helps us to inject sufficient holes and electrons for effective observation of *p*- and

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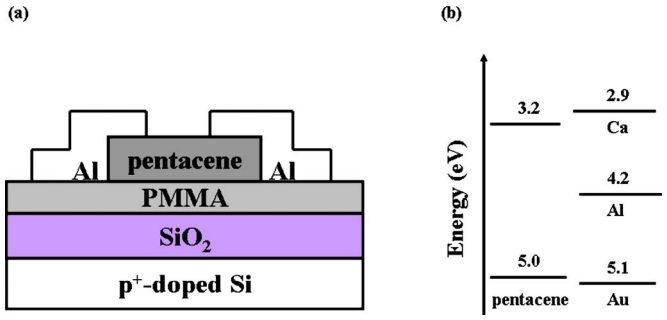

FIG. 1. (Color online) (a) Schematic structure of ambipolar pentacene top-contact FET. (b) Energy band diagrams of pentacene and work function of Ca, Al, and Au.

n-channels in OFETs. Finally, we demonstrate the formation of inverter by the integration of two identical ambipolar transistors.

II. EXPERIMENTAL DETAILS

The heavily doped *p*-type silicon (p^+-Si) wafer and a 300 nm thermally oxidized SiO_2 film were used as the gate and dielectric of the ambipolar transistors, respectively. The substrates were cut to 2×2 cm^2 in size through mechanical scribing. Prior to the deposition, the substrates were cleaned by acetone and isopropanol in an ultrasonic bath followed by UV-ozone cleaning for 15 min. The crucial interfacial-modifying layer was prepared by spin-coating a solution of PMMA (2 wt %) in tetrahydrofuran at 1000 rpm and with a thickness of 150 nm. The PMMA-coated substrates were baked at 70 °C for 30 min to remove the residual solvent. Then, the wafers were quickly transferred to a vacuum chamber for the deposition of the active layer. The semiconductor layer, consisting of a 50 nm thick pentacene layer, was then deposited at a growth rate of 0.2 Å/s, a substrate temperature of 60 °C, and a base pressure of 6×10^{-6} torr. Pentacene was used without further purification from Sigma-Aldrich. Finally, the 50 nm thick aluminum film was thermally evaporated onto the pentacene film through a shadow mask to form the *S*/*D* electrodes. In addition, Au, Ag, and Ca were also investigated as alternatives to the Al as *S*/*D* contacts. A schematic cross section of the top-contact OFETs is presented in Fig. 1(a). The length and width of the channel were 100 μm and 2 mm, respectively. The electrical measurements of the devices were performed at room temperature in a nitrogen environment inside a glovebox by using HP 4156C and Keithley 4200 semiconductor parameter analyzers. The capacitance-voltage (*C*-*V*) measurement was performed by an Agilent E4980A precision *LCR* meter.

III. RESULTS AND DISCUSSION

In the operation of ambipolar FETs, charge carrier transport strongly depends on two factors: (1) semiconductor/dielectric interface, where the charge transport takes place in the semiconductor layer, and (2) metal/semiconductor interface, where the charge injection occurs from the electrode into semiconductor. For the realization of ambipolar pentacene FETs, the devices were first fabricated on the SiO_2 gate dielectric and later on a PMMA-capped SiO_2 (PMMA/SiO_2)

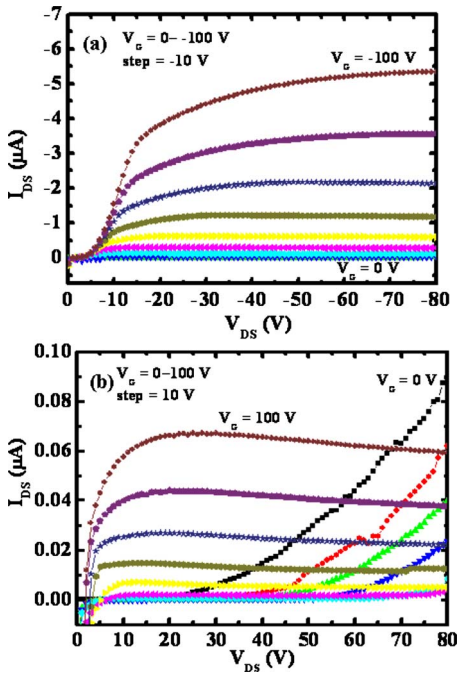

FIG. 2. (Color online) Output characteristics of ambipolar pentacene FET grown on a PMMA/SiO_2 dielectric in (a) *p*- and (b) *n*-channel operations.

as the dielectric with Al as *S*/*D* electrodes. However, the devices fabricated on a SiO_2 dielectric only exhibit a *p*-type behavior, even at a positive bias of 100 V to the gate and drain electrodes (not shown here). In contrast, the devices fabricated on a PMMA/SiO_2 exhibit an ambipolar behavior for a gate voltage $V_G \geqq |40|$ V. The reason for the presence of ambipolar behavior is attributed to the relatively small surface energy on the PMMA-modified SiO_2 gate dielectric as compared to that on the bare SiO_2 surface. Due to this, the enhanced grain growth of pentacene takes place and hence the reduced grain boundary density; the details will be described in the next section. Figure 2 shows the drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) of pentacene FETs on the PMMA/SiO_2 dielectric at different gate voltages (V_G). It is noted that the output characteristics exhibit significant saturation, which behaves quadratically as a function of gate bias. The sharp increase in the drain current at low gate voltages and below the threshold voltage was observed. Such phenomenon was also reported in literature.[20,21] Figure 3 shows the corresponding plots of $|I_{DS}|$ and $|I_{DS}|^{1/2}$ vs V_G. It can be observed that these devices exhibit strong field-effect modulations of channel conductance in the ambipolar operation with threshold voltages (V_T) of −27 and 42 V for *p*- and *n*-type operations, respectively. The saturated drain current ($I_{DS,\mathrm{sat}}$) is close to 7×10^{-8} A at V_G=100 V for *n*-type operation and 5.5×10^{-6} A at V_G=−100 V for *p*-type operation. The field-effect mobilities (μ) are extracted from the measured transfer curves by comparing it to the standard transistor's current-voltage equation in the saturation regime as follows:

$$I_{DS,\mathrm{sat}} = (WC_i/2L)\mu(V_G - V_T)^2,$$

where *W* and *L* are the width and length of the channel, respectively, and C_i is the gate dielectric capacitance. The μ

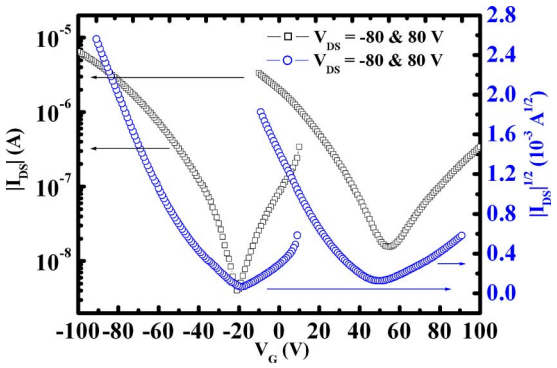

FIG. 3. (Color online) Transfer characteristics of $|I_{DS}|$ and $|I_{DS}|^{1/2}$ vs V_G for ambipolar pentacene FET in *p*- and *n*-channel operations.

values for hole and electron are estimated as 0.026 and 0.0023 cm^2/V s, respectively.

To observe the charge accumulation capability, we measured the *C-V* characteristics of metal-insulator-semiconductor (*MIS*) devices for the pentacene on SiO_2 and $PMMA/SiO_2$ insulators at 5 kHz, which is displayed in Fig. 4. The inset of Fig. 4 shows the scheme of *MIS* devices. In the case of $PMMA/SiO_2$, it can be observed that the capacitance increases with increasing $|V_G|$. It implies that sufficient holes and electrons can be accumulated at the interface to reveal the ambipolar transport in the pentacene on $PMMA/SiO_2$. However, the devices with SiO_2 show the hole accumulation and indistinct electron accumulation. Therefore, the insufficient electron accumulation accounts for unipolar carrier transport in pentacene on SiO_2. These results show the presence of serious electron traps at semiconductors/SiO_2 interface, which is in agreement with the observations by Chua *et al.*[16] It has been suggested that the electron trapping hydroxyl groups will attenuate the *n*-type behavior in various conjugated polymers and thus the organic FETs. These electron trap states will prevent the Fermi level from shifting within the semiconductor band gap as the gate potential is changed. In the case of *n*-type devices, the resistance to the Fermi-level shift will result in a potential barrier for charge transport. Hence, the use of

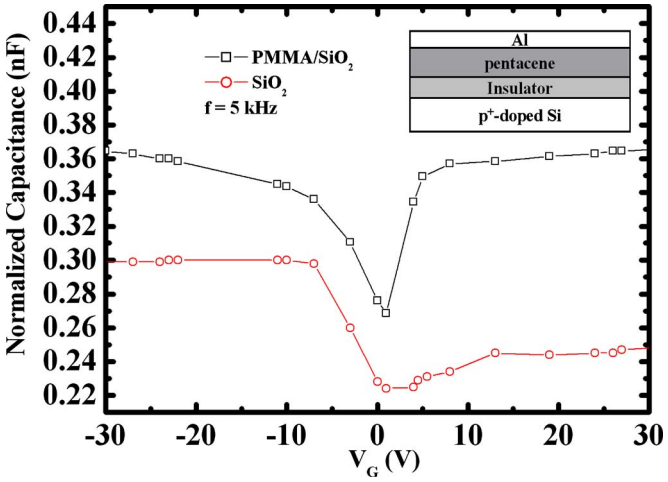

FIG. 4. (Color online) Comparison of capacitance-voltage characteristics for the ambipolar pentacene FETs with/without a PMMA layer measured from the *MIS* configuration with a frequency of 5 kHz.

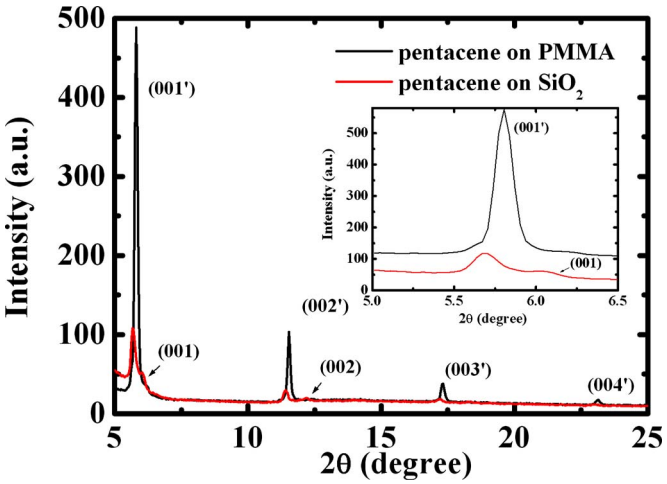

FIG. 5. (Color online) XRD patterns with Cu $K\alpha$ radiation for the pentacene thin films grown on SiO_2 and PMMA-modified SiO_2, and the inset is the enlarged first peak of XRD patterns.

hydroxyl-free polymer, PMMA, as the dielectric can reduce the electron traps and reveal the *n*-type conduction.

In order to further understand the existence of the ambipolar behavior, the structural properties and morphology of pentacene thin films were investigated by x-ray diffraction (XRD) and atomic force microscopy (AFM). Figure 5 shows the XRD patterns with Cu $K\alpha$ radiation for the pentacene thin films grown on SiO_2 and PMMA-modified SiO_2. The pentacene films grown on PMMA exhibit a conspicuous peak intensity as compared to the pentacene films directly grown on SiO_2. In addition, the first-order reflection peak of pentacene on PMMA-modified SiO_2 shows only single-crystal phases $(00l')$, but the reflection peak of pentacene on SiO_2 shows a mixture of the thin film phase $(00l)$ and the single-crystal phase. It has been found that the growth of pentacene thin film on PMMA is well favored due to the reduced surface energy of PMMA as compared to that on the bare SiO_2 substrate, which thereby leads to high-quality crystalline peaks. Such a behavior has been reported previously.[22,23] Hence, the surface energy plays a major role in obtaining high-quality pentacene films. It has been suggested that the match of the surface energy between the PMMA insulator and the pentacene can contribute to polycrystalline pentacene film.[24] The present AFM images support the contention that the pentacene films deposited on PMMA have better crystal quality, which is shown in Fig. 6. Moreover, the grain size (300–1000 nm) of pentacene films on PMMA is much larger than that (100–500 nm) on SiO_2. It indicates that the insertion of PMMA layer on SiO_2 gate dielectric will favor the substantial grain growth of pentacene. Since the smaller grain sizes on SiO_2 normally result in active trapping sites, free carriers will be captured at the grain boundaries. Due to these charge traps, a potential barrier is formed at the grain boundary, which limits the charge transport between grains. The degree of charged traps can be further demonstrated by extracting the subthreshold swing from the transfer characteristics of OFETs. The subthreshold slope (S) is defined by the equation

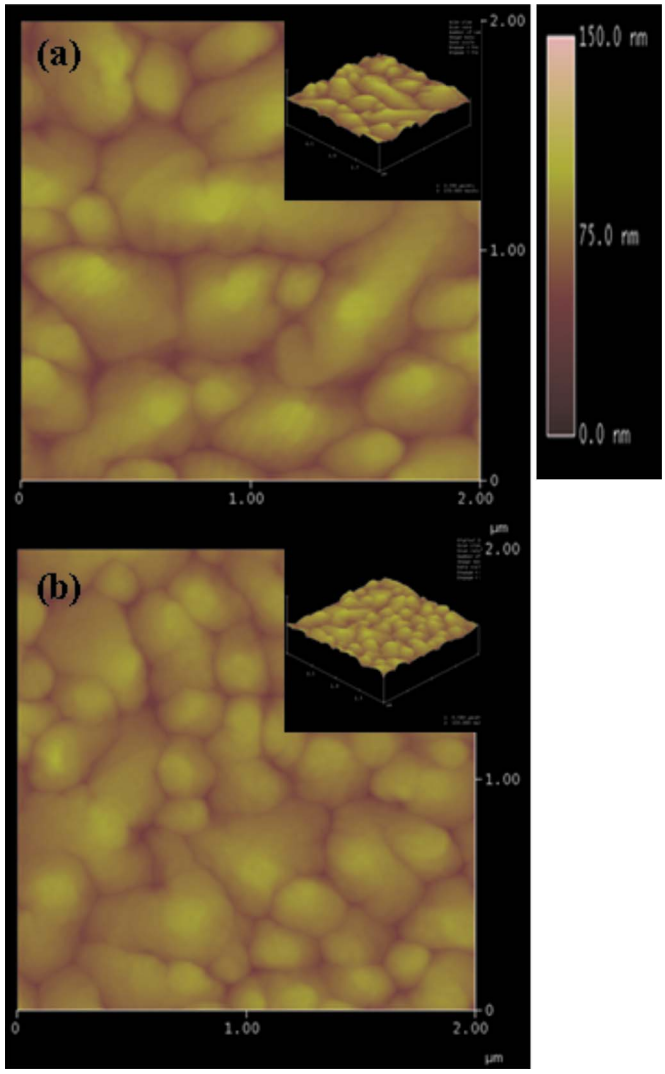

FIG. 6. (Color online) AFM images of pentacene grown on the (a) PMMA and (b) SiO_2 surfaces. The inset shows the corresponding three-dimensional (3D) images.

$$S = \left(\frac{d \log I_D}{dV_{GS}} \right)^{-1}$$

and the corresponding density of traps (N_{SS}) is given by the approximation

$$N_{SS} = \left(\frac{S \log e}{kT/q} - 1 \right) \frac{C_i}{q},$$

where k is Boltzmann's constant, T is the absolute temperature, q is the electron charge, e is a constant and has a value as 2.718 28, and C_i is the dielectric capacitance per unit area.[25] The subthreshold slopes of the p-channel devices with SiO_2 and PMMA/SiO_2 are 1.43 and 0.4 V/decade, respectively. In addition, the corresponding trap densities are 1.11×10^{12} and 2.85×10^{11} cm^{-2}, respectively. Moreover, the C-V measurements show a larger capacitance for the pentacene on PMMA in the reserve bias. The consistency of these results strengthens the argument as to the reduction of charge traps.

The influence of the interface between semiconductor and metal for the pentacene FETs can be ascertained by varying the S/D electrodes. In this case, three different metal electrodes, Ag, Au, and Ca, are used as the S/D contacts to vary the barrier height for hole and electron injection into the pentacene layer. Energy band diagrams of pentacene and the work function of different metals are shown in Fig. 1(b). All of these devices show ambipolar characteristics as well. Figures 7(a) and 7(b) show the transfer characteristics for different metals as the S/D electrodes. The devices with Au as electrodes show the enhancement of p-type behavior, but poor n-type behavior. Since the work function of Au is 5.1 eV, which is very close to the highest occupied molecular orbital of pentacene, it is much easier for a hole than an electron to inject from the metal electrode into semiconductor. Using Ca as S/D electrodes, the results obtained are vice versa, i.e., the enhancement of n-type behavior but poor p-type behavior is observed. Al and Ag metals, when used as S/D electrodes, possess a suitable work function to balance the hole and electron injection into the highest occupied and the lowest unoccupied molecular orbitals of pentacene. Although the charge injection barriers are balanced in both polarities, the increase of potential drop at organic/metal interface will increase the $|V_T|$ as compared to Au in p-channel operation and Ca in n-channel operation.[26] The summary of ambipolar pentacene FETs with different metals as S/D electrodes is given in Table I. These results demonstrate that the incorporation of the suitable metal in pentacene FETs also plays an important role to reveal the ambipolar characteristics.

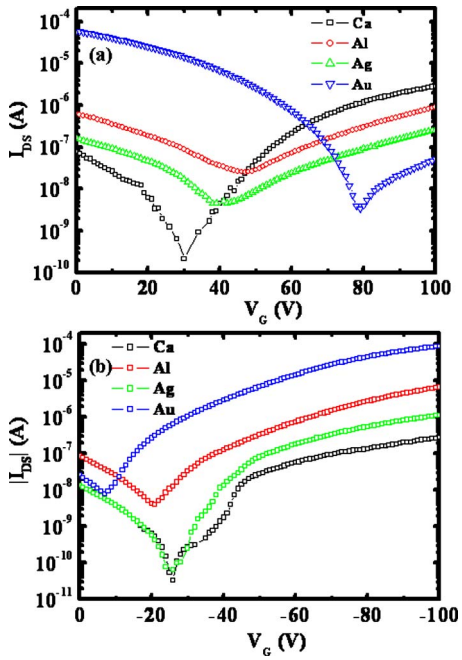

FIG. 7. (Color online) Transfer characteristic of ambipolar pentacene FETs with different S/D metal electrodes in (a) n- and (b) p-channel operations.

We have fabricated a complementarylike inverter by connecting two identical pentacene transistors, which are shown in the inset of Fig. 8. Due to the unique ambipolar characteristic, the inverter is capable of operating in the first and third quadrants. The typical transfer characteristics of such an inverter are shown in Figs. 8(a) and 8(b). A sharp inversion is observed in both quadrants. When the supply

TABLE I. Summary of parameters extracted from the ambipolar pentacene FETs using different metals as source and drain electrodes.

S/D metal	Mobility ($cm^2/V\,s$)		On/off current ratio		Subthreshold slope		V_T (V)	
	n	p	n	p	n	p	n	p
Ca	8.5×10^{-3}	7.5×10^{-3}	1×10^{4}	1×10^{4}	0.4	1.1	31	−47
Al	2.3×10^{-3}	2.6×10^{-2}	1×10^{2}	1×10^{3}	1.0	0.4	42	−27
Ag	2.1×10^{-3}	2.2×10^{-2}	1×10^{3}	1×10^{4}	0.7	0.4	37	−35
Au	1.0×10^{-4}	9.0×10^{-2}	1×10^{2}	1×10^{4}	1.1	0.3	55	−15

voltage (V_{DD}) and input node (V_{in}) are biased positively, the ambipolar transistors are operated as *p*- and *n*-channel FETs, and the inverter works in the first quadrant with the a maximum voltage gain of 8. Whereas the supply voltage (V_{DD}) and input node (V_{in}) are biased negatively, the ambipolar transistors can be operated as *p*- and *n*-channel FETs, and the inverter works in the third quadrant with the a maximum voltage gain of 11.

IV. CONCLUSIONS

In this work, the ambipolar pentacene FETs have been demonstrated through interface engineering. Incorporating the PMMA acting as an interfacial-modified layer, ambipolar transport can be observed as a result of the elimination of surface traps. Meanwhile, using a suitable work-function metal electrode can balance the carrier injection of both polarities thereby leading to the ambipolar conduction. Accordingly, the achievement of ambipolar conduction of OFET from a single semiconductor layer can be realized by interface modification. For further enhancing the performance of the devices, the optimization of the quality of interfacial-modified layer and the facilitation of carrier injection from metal electrodes to semiconductor will be promising.

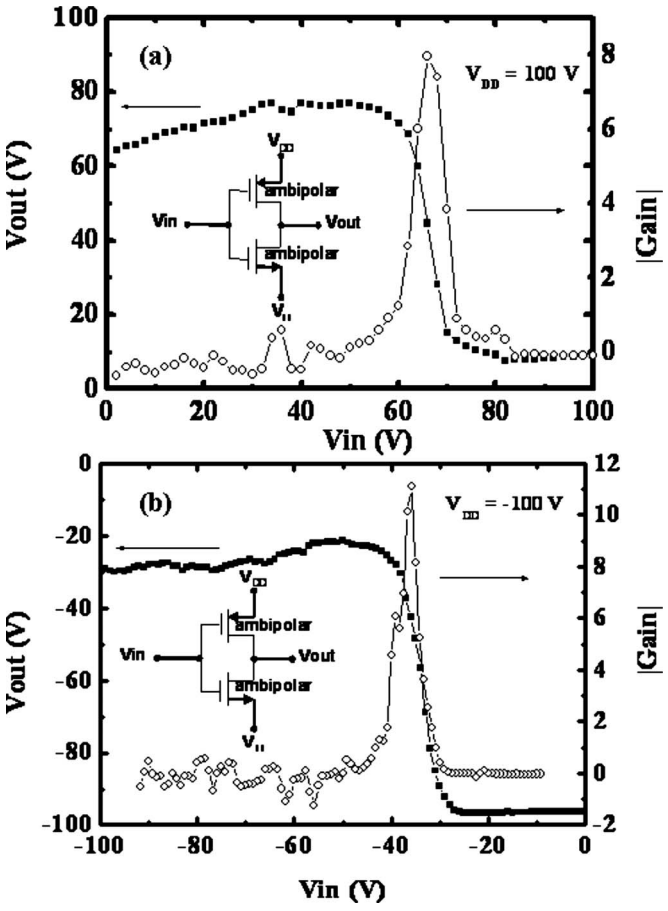

FIG. 8. Transfer characteristics of complementary meta-oxide semiconductor (CMOS)-like ambipolar pentacene inverter (a) in the first and (b) third quadrants with their corresponding gains. The insets show the scheme of the inverter circuit.

ACKNOWLEDGMENTS

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[1] C. D. Dimitrakopoulos and P. R. L. Malenfant, Adv. Mater. (Weinheim, Ger.) **14**, 99 (2002).
[2] E. J. Meijer, D. M. de Leeuw, S. Setayesh, E. Van Veenendaal, B. H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf, and T. M. Klapwijk, Nat. Mater. **2**, 678 (2003).
[3] M. Kitamura and Y. Arakawa, Appl. Phys. Lett. **91**, 053505 (2007).
[4] J. Shi, H. Wang, D. Song, H. Tian, Y. Geng, and D. Yan, Adv. Funct. Mater. **17**, 397 (2007).
[5] S. Cho, J. Yuen, J. Y. Kim, K. Lee, and A. J. Heeger, Appl. Phys. Lett. **89**, 153505 (2006).
[6] H. Klauk, M. Halik, U. Zschieschang, F. Eder, D. Rohde, G. Schmid, and C. Dehm, IEEE Trans. Electron Devices **52**, 618 (2005).
[7] D. J. Gundlach, K. P. Pernstich, G. Wilckens, M. Grüter, S. Haas, and B. Batlogg, J. Appl. Phys. **98**, 064502 (2005).
[8] T. D. Anthopoulos, D. M. de Leeuw, E. Cantatore, S. Setayesh, E. J. Meijer, C. Tanase, J. C. Hummelen, and P. W. M. Blom, Appl. Phys. Lett. **85**, 4205 (2004).
[9] T. B. Singh, P. Senkarabacak, N. S. Sariciftci, A. Tanda, C. Lackner, R. Hagelauer, and G. Horowitz, Appl. Phys. Lett. **89**, 033512 (2006).
[10] H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y. Y. Lin, and A. Dodabalapur, Nature (London) **404**, 478 (2000).
[11] R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard, and R. M. Fleming, Appl. Phys. Lett. **67**, 121 (1995).
[12] T. F. Guo, Z. J. Tsai, S. Y. Chen, T. C. Wen, and C. T. Chung, J. Appl. Phys. **101**, 124505 (2007).
[13] T. B. Singh, F. Meghdadi, S. Günes, N. Marjanovic, G. Horowitz, P. Lang, S. Bauer, and N. S. Sariciftci, Adv. Mater. (Weinheim, Ger.) **17**, 2315 (2005).
[14] N. Benson, M. Schidleja, and C. Melzer, Appl. Phys. Lett. **89**, 182105 (2006).
[15] M. Ahles, R. Schmechel, and H. von Seggern, Appl. Phys. Lett. **85**, 4499 (2004).
[16] L. L. Chua, J. Zaumseil, J. F. Chang, E. C. W. Ou, P. K. H. Ho, H. Sirringhaus, and R. H. Friend, Nature (London) **434**, 194 (2005).
[17] C. Rost, D. J. Gundlach, S. Karg, and W. Rieß, J. Appl. Phys. **95**, 5782 (2004).

[18]T. D. Anthopoulos, S. Setayesh, E. Smits, M. Cölle, E. Cantatore, B. de Boer, P. W. M. Blom, and D. M. de Leeuw, Adv. Mater. (Weinheim, Ger.) **18**, 1900 (2006).
[19]T. D. Anthopoulos, G. C. Anyfantis, G. C. Papavassiliou, and D. M. de Leeuw, Appl. Phys. Lett. **90**, 122105 (2007).
[20]H. Wang, J. Wang, X. Yan, J. Shi, H. Tian, Y. Geng, and D. Yan, Appl. Phys. Lett. **88**, 133508 (2006).
[21]E. C. P. Smits, S. Setayesh, T. D. Anthopoulos, M. Buechel, W. Nijssen, R. Coehoorn, P. W. M. Blom, B. de Boer, and D. M. de Leeuw, Adv. Mater. (Weinheim, Ger.) **19**, 734 (2007).
[22]T. S. Huang, Y. K. Su, and P. C. Wang, Appl. Phys. Lett. **91**, 092116 (2007).
[23]J. Puigdollers, C. Voz, A. Orpella, R. Quidant, I. Martin, M. Vetter, and R. Alcubilla, Org. Electron. **5**, 67 (2004).
[24]W. Y. Chou, C. W. Kuo, H. L. Cheng, and Y. R. Chen, Appl. Phys. Lett. **89**, 112126 (2006).
[25]C. R. Kagan and P. Andry, *Thin-Film Transistors* (Dekker, New York, 2003), p. 87.
[26]X. Yan, J. Wang, H. Wang, H. Wang, and D. Yan, Appl. Phys. Lett. **89**, 053510 (2006).