# 行政院國家科學委員會專題研究計畫成果報告
# 深次微米 T 型閘極金氧半電晶體之研製
# Development and Characterization of a Novel Method for Fabricating deep-micron Si MOSFET's with T-Shaped Gate

計畫編號：NSC 88-2215-E-009-030
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一、中文摘要：

在本研究計畫中，我們成功的研製出一新式自我校準之 T 型閘極金氧半電晶體，我們簡稱為 STAIR 製程。製程中使用化學機械研磨平坦化製程，BOE 選擇性蝕刻及多晶矽 sidewall spacer 技術製成 T 型多晶矽閘極結構。自我校準之鈷的矽化金屬已成功的降低閘/源/汲極之寄生電阻並降低了閘極片電阻。此外，元件沈積覆蓋層時，閘極邊牆下方形成的空氣邊襯對於降低閘極寄生電容將深具潛力。故本計畫研製出之 T 型閘極金氧半電晶體，很適用於未來高速元件的製作。

關鍵詞：T 型閘極，化學機械研磨，自我校準的矽化金屬，寄生電阻，空氣邊襯

Abstract:

In this project, we have successfully demonstrated a novel process dubbed STAIR (self-aligned T-shaped gate and Air spacer) for fabricating deep sub-micron Si MOSFETs. This method employs CMP planarization, BOE selective etching and poly-Si sidewall spacer techniques to form the T-shaped poly-Si gate structure. Co salicide process is also used to reduce device's parasitic gate/source/drain resistance. Effectiveness of T-shaped gate in reducing the sheet resistance is clearly demonstrated. An air spacer is formed at gate sidewall after CVD passivation oxide deposition, which can potentially reduce the parasitic capacitance. It is therefore very promising for future high-speed device applications.

Keyword: T-shaped Gate, CMP, Salicide, Parasitic Resistance, Air Spacer

二、緣由與目的：

Self-aligned silicide (salicide) process is extremely important for deep sub-micron manufacturing in order to reduce device's parasitic resistance. As devices' dimensions are scaled down, however, the sheet resistance of narrow silicide lines is known to rise with decreasing line width due to increasing difficulty in phase transition of silicide [1][2], and/or poor thermal stability [3]. Recently, it was shown that the use of T-shaped gate can solve the aforementioned problems [4][5]. This is ascribed to the structural improvement since the effective width of silicide on salicided poly-Si gates increases. In these studies, selective epitaxial growth (SEG) technique was used to form the T-shaped gates. We have also proposed and demonstrated a novel process which does not involve SEG to form T-shaped gate [6]. The results indicated that the gate sheet resistance decreases significantly in deep sub-micron regime while the thermal stability is improved as well. In this study, we extend the process to fabricate Si MOS transistors. Such method is dubbed STAIR since the completed devices feature both self-aligned T-shaped gate and air spacer. This method does not rely on lift-off technique to form T-shaped gate. Additionally, the air spacer can potentially reduce the parasitic sidewall capacitance. It is thus very attracting for Si ULSI manufacturing.

三、研究方法與成果：

N-channel MOS transistors were

fabricated on 6-in. Si wafers. Process flow is illustrated in Fig.1. Briefly, after growth of gate oxide (4 nm) and $n^+$ poly-Si layers (200 nm) gate resist patterns were formed and narrowed by an O, plasma treatment [7], followed by conventional steps to form the gate and S/D regions, as shown in Fig.1(a). TEOS spacer was used in the fabrication for self-aligned separation of the extension and deep S/D regions. An additional 550-nm-thick TEOS was then deposited and planarized using a CMP step to a remaining thickness of around 350 nm (Fig.1(b)). BOE selective etching was then used to further thin down the TEOS to around 100 nm (Fig.1(c)). A 2nd poly-Si layer was deposited and etched with a reactive plasma to form the T-shaped gate (Fig.1(d)). The remaining TEOS was then stripped off by BOE etching (Fig.1(e)). An SEM picture of the T-shaped gate structure after this step is shown in Fig.2.

Wafers were then further split into two groups to receive or skip the salicide treatment. For the salicided split, a Co(10 nm)/TiN(30 nm) stacked layer was deposited by sputtering. Due to the shadowing nature of the T-shaped gate, the metal film is deposited with a form as shown in Fig.3(a) and demonstrated by SEM picture in Fig.3(b). Such film structure can potentially reduce the possibility of bridging since the deposited films are disconnected. Devices with conventional poly-Si gate structure were also fabricated for comparison.

After the T-gate processing, a 550-nm-thick TEOS was deposited and an air spacer is formed, as shown in Fig.4. In this work, both low-pressure chemical vapor deposition(LPCVD) and plasma enhanced chemical vapor deposition(PECVD) were employed for forming the TEOS layer. Both methods successfully show the formation of air spacer, as shown in Figs.4(a) and (b), respectively. These results are ascribed to the fast deposition rate of TEOS as well as the weight of the TEOS film imposing on the T-shaped gate. The weight serves to bow the "wing" of the gate down and help prevent the deposited species from entering the portion underneath the "wing". The leakage between gale and drain for salicided T-shaped gale devices was measured with an edge-intensive test structure and the results are shown in Fig.5, which are comparable to those obtained in former reports [4][5].

The effectiveness of T-shaped gate in reducing the sheet resistance is illustrated in Fig.6, in which the sheet resistance of conventional poly-Si gate, poly-Si T-shaped gate, and salicided T-shaped gate were measured and compared. It is seen that the narrow-line-width effect appears for conventional poly-Si gate and is suppressed with the use of poly-Si T-shaped gate structure. Further improvement is achieved with the implementation of Co salicide.

## 四、結果與討論：

Device performance was characterized with an HP4156 parameter analyzer. Results of the measured threshold voltage ($V_{th}$) for different gate structures are shown in Fig.7 and no significant difference is observed among them. The salicided T-shaped gate devices, however, show superior driving capability than nonsalicided devices. An example is shown in Fig.8 and Fig.9 in which the current-voltage characteristics of 0.25 μm conventional poly-Si gate and salicided T-shaped gate devices are compared. Transconductance (Gm) and drive current as a function of channel length for the three splits are given in Figs.10 and 11, respectively. It is seen that the results of non-salicided devices deviate from the theoretical 1/L behavior as channel length is scaled below 2 μm, indicating that the parasitic source and drain resistances are significantly high to affect the output performance. With the implementation of Co salicide process, significant improvement is observed in the deep sub-micron regime so that the curves shown in the figures roughly follow the 1/L relation.

## 五、計畫成果自評：

In summary, we have successfully

demonstrated a novel process dubbed STAIR for fabricating deep sub-micron Si MOSFETs featuring both T-shaped gate and air spacer, which are highly desirable for reducing the parasitic resistance as well as capacitance. This novel scheme is self-aligned and simple and uses no lift-off step. In addition, it is compatible with salicide process. It is therefore very promising for future high-speed device applications.

Some works have been published on the proceeding of conference [8-9] or journal [6].

六、致謝：

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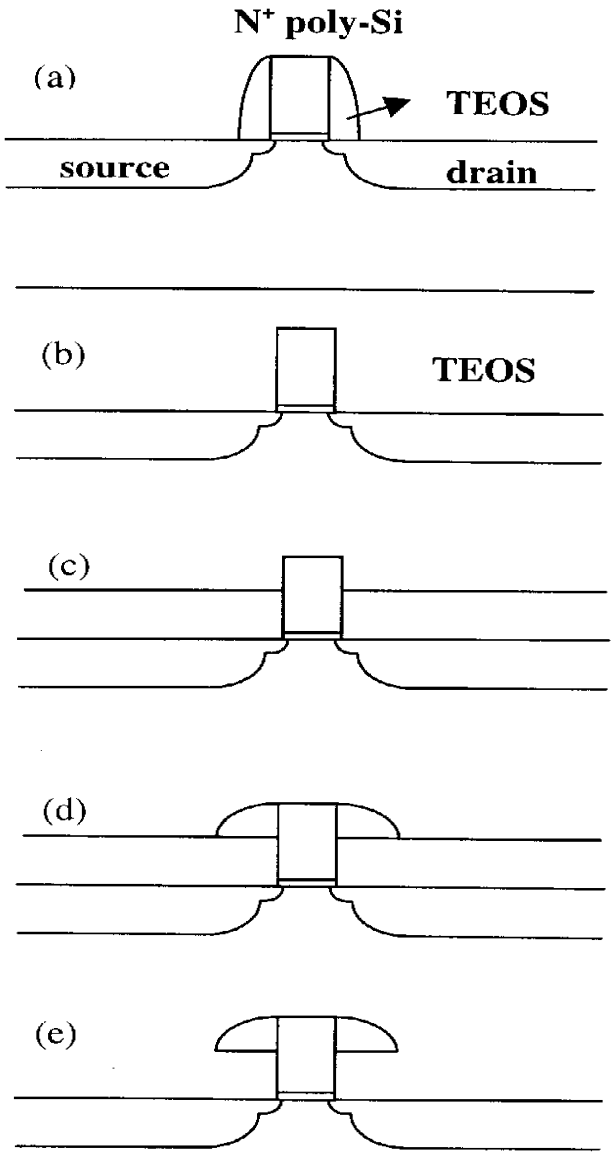


Fig.1 Process flow of the STAIR process.

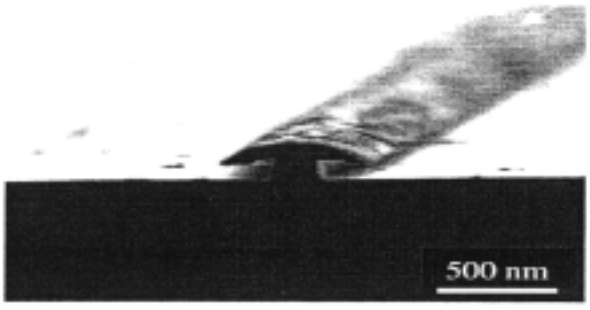


Fig.2 SEM of the T-shaped gate.

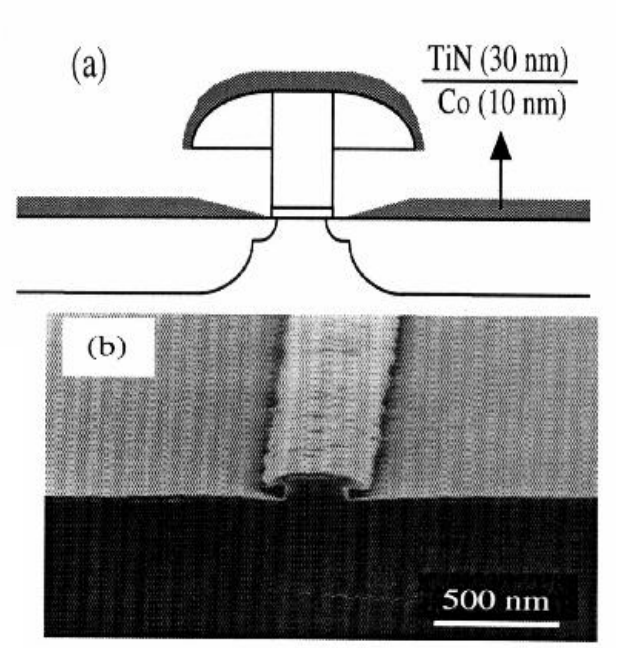


Fig.3 (a) Illustration and (b) SEM picture of the metal film deposited on the T-shaped gate structure.

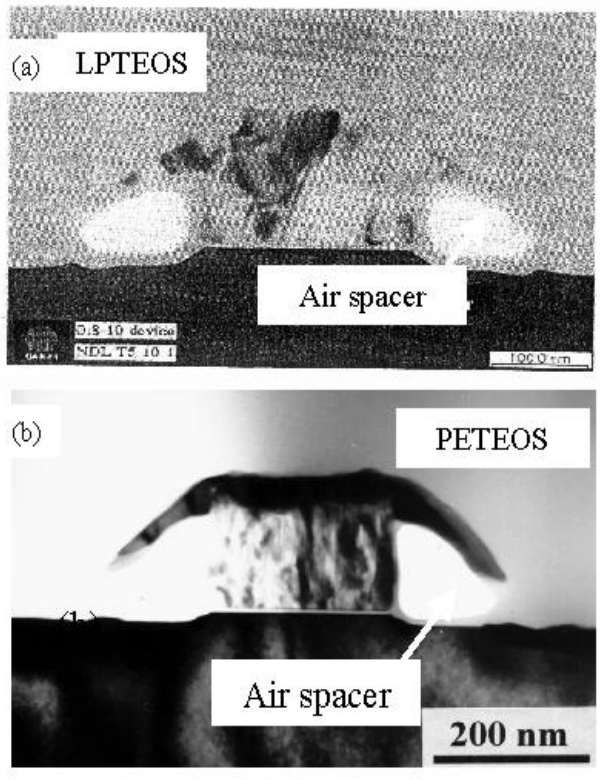


Fig.4 Cross-sectional TEMs of the gate structure showing the T-gate and air-spacer with (a) LPCVD and (b) PECVD TEOS passivation

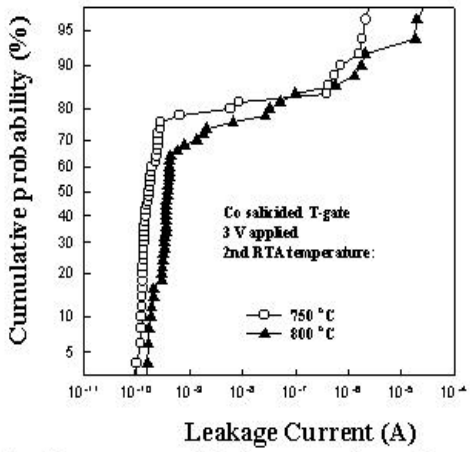


Fig.5 Leakage current between gate and source/drain.

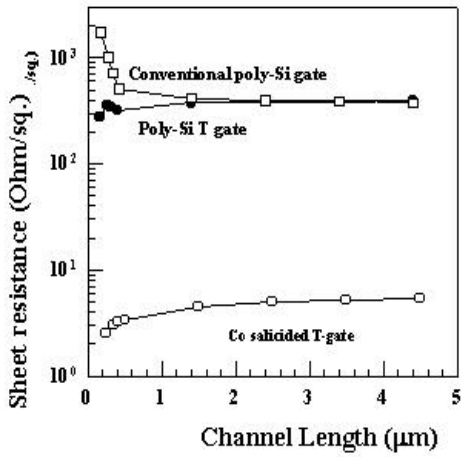


Fig.6 Sheet Resistance of the conventional poly-Si T-gate, and Co salicided T-gate structures as a function of channel length.

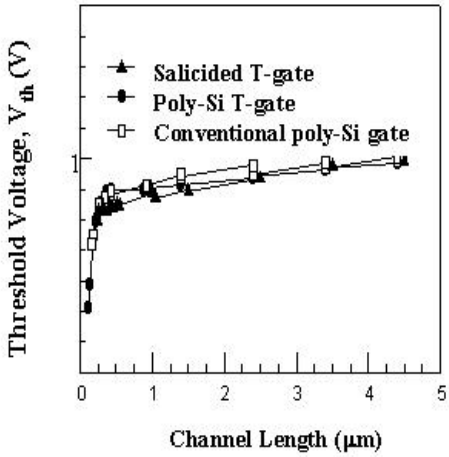


Fig.7 Threshold Voltage as a function of channel length for devices with different gate structures.

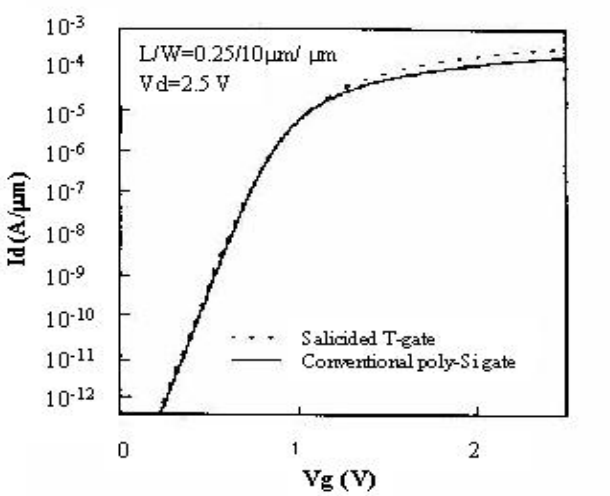


Fig.8 Subthreshold characteristics of 0.25 $\mu$ MOS transistors with conventional poly-Si gate and salicided T-gate.

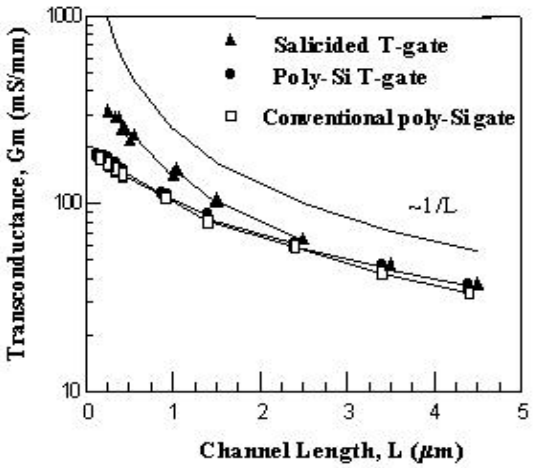


Fig.10 Transconductance as a function of channel length for devices with different gate structures.

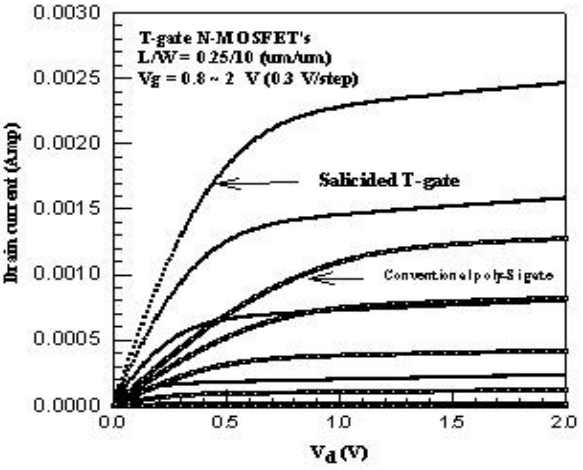


Fig.9 Id-Vd characteristics of 0.25 $\mu$m MOS transistors with conventional poly-Si gate and salicided T-gate.

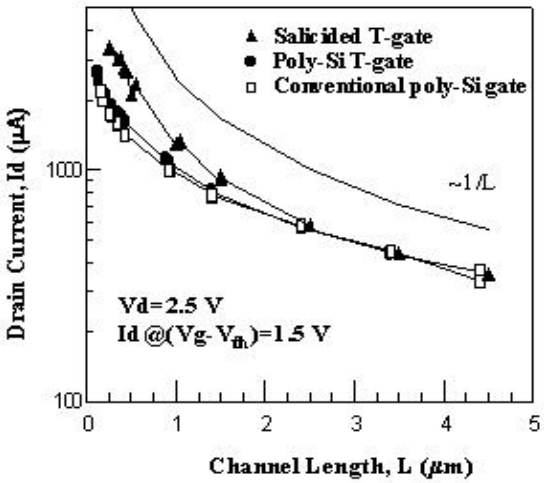


Fig.11 Output Id as a function of channel length for devices with different gate structures.