行政院國家科學委員會 專題研究計畫成果報告

深次微米 MOSFET 穿遂漏電流，鎖定及靜電放電之研究

Tunneling Leakage, Latch-up, and ESD in Deep Submicron MOSFETs

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一、中文摘要

本計劃深入研究深次微米 MOSFET's 可靠性的三項重要課題：穿隧漏電流，靜電放電及電路鎖定，在穿隧漏電流方面，進行（1）建立物理解析式陷井輔助穿隧模式以解釋並重現不同溫度下實驗數據；(2)在 0.18μm/0.25μm/0.35μm 製程將口袋型及反穿透離子佈植最佳化以控制基座穿隧漏電流；（3）利用三維蒙地卡羅模擬軟體亂數產生薄氧化層內部陷井分佈以與穿隧所引致漏電流增加和介電破壞做一連結並重現 0.18μm/0.25μm/0.35μm 實驗結結;及(4)將以往於一 p 通道表面穿隧研究數據做一最終總整理。鎖定和靜電放電方面則（1）建立物理解析模式以重現高溫磊晶式 CMOS 鎖定實驗數據；（2）將靜電放電晶護結構人體及機器模式故障電壓、過高應力電流脈衝故障實驗以及電熱故障模式加以整合做一密切關聯；以及（3）發展 0.18μm/0.25μm/0.35μm 製程過高電應力/靜電放電晶護結構並修正故障模式。

關鍵詞：穿隧漏電流 氧化層崩潰 深次微米 靜電放電 鎖定 超大型積體電路

Abstract

The project will extensively investigate the three important topics concerning the deep submicron MOSFET's reliability : Tunneling Leakage, ESD, and Latch-up. To be performed for the tunneling leakage issue are (1) Construct a physically-based analytic trap-assisted tunneling model in order to explain and reproduce the experimental data at different temperatures;(2)Optimize the pocket and anti-punchthrough implant dosage/energy and angle in processes down to 0.18μm aiming to control the bulk tunneling leakage, (3)Use a three-dimensional Monte-Carlo simulator to generate randomly the trap distribution in ultra -thin oxides and make a linking to the stress induced-leakage current SILC and the dielectric breakdown in processes down to 0.18μm; and (4)Make a final treatment to the p-cell surface tunneling or GIDL data measured before. For the remaining two topics, we will (1)establish a new physically-based model to reproduce the high-temperature latch-up data in epi-CMOS ; (2)make a concise linking between the ESD HBM and MM mode failure voltages, the EOS current pulse failure experiment, and the electro-thermal failure model; and (3)develop a novel EOS/ESD protective structure suitable for the processes down to 0.18μm, and also make a modification on the failure model.

Keywords: Tunneling Leakage, Oxide breakdown, Deep Submicron, ESD, Latch-up, VLSI

二、緣由與目的

我國的半導體工業正穩健的向深次微米之路邁進，現階段已漸次具備 0.25 μm 5 的量產能力，今年底可將技術層次推向預定的 0.18μm 製程，藉著持續不斷的努力，最終我國的半導體工業將能根深蒂固，壯大發展，成就民族工業命脈。然現階段可靠性問題如 Tunneling Leakage 穿隧漏電流，ESD 靜電放電，如 Latch-up 鎖定等嚴重困擾國內半導體工業界，且隨著製程技術的 scaling 無論國內外此問題越來越重來。

三、研究方法與成果

本計劃的主力為博士班四年5 黃煥宗如李煥松二人，前者博士論文主題為 Tunneling Leakage 文者為 EOS/ESD 如 Latch-up。

文 Tunneling Leakage 方面，黃煥宗已文 1998 年四9 IEEE EDL 發表一篇極具極量的 Bulk Tunneling Leakage in Scaled MOSFETs。並完成三維 oxide trap 之 Monte-Carlo 模擬軟體，可與 SILC(Stress induced leakage current) 如 dielectric breakdown 與一 linking，與前已完成一篇論文，為文者 dielectric breakdown 的 linking 並成功應用至 TSMC 0.18至m process。文本計劃中黃煥宗進行的工與重點為：

1. ： 1998 年四9 IEEE EDL bulk tunneling 論文為基礎，積極建建 trap-assisted bulk tunneling 解析模式並完成與實驗比較（我們已測出 bulk tunneling 的溫度變化成分明顯看出低電壓時 trap-assisted 成分之 dominance），並同時與 TSMC 同與 0.18μm/0.25μm/0.35μm process 中如同 optimize pocket 如 anti-punchthrough implant ：控制 bulk tunneling。
2. Ultra-thin oxide 之 tunneling 如其所衍生之 degradation 生為重點之一，首先利用我們自創的三維 Monte-Carlo 模擬軟體 generate randomly tunneling induced trap 之分佈，即能與 SILC as well as dielectric breakdown 即一 linking 並重現實驗數據。與 TSMC 同與生包含了此 linking 如實驗重現。
3. tunneling 了前面的 bulk tunneling 如 oxide tunneling 外，尚有傳統的 Surface tunneling (即 GIDL)。我們文 0.8μm, 0.6μm, 0.35μm 製程6 積大量 GIDL 數據，self-consistent 已6 完成，將與最文總整理，預定產生最少二篇創新論文，題與如下：
   - A Technology-Independent Correlation between GIDL and Electron Current Injection
   - A Model for p-cell GIDL Induced Degradation

文 EOS/ESD 如 Latch-up 方面，李煥松已文 1997 年 4 9 IEEE IRPS 發表一篇 latch-up 論文，並完成了P 溫 latch-up 研究（0.35μm 製程且： 5P 不同 epi P 度如 4P 不同 n-p 間距為參數的 testkey）。最6 漸次完成 EOS/ESD 保護結構之P 電流暫態量測、故障量測如物理機制導出解釋實驗結釋。文本實驗中李煥松進行的工與重點為：

1. ：1997 年 IRPS latch-up 論文為基礎，導出創新型物理解析模式 ：重現P 溫 latch-up 實驗，可應

用於工業如特殊應用電子、CMOS 產子、P 溫P 壓 burn-in、子深次微米 CMOS 晶片因P 速P 密度產生P 功密P 溫度等。

2. 整理 0.6μm 如 0.35μm 等製程的 EOS/ESD 保護結構之大量實驗數據，包密 HBM 如 MM modes 之 ESD 故障電壓、EOS 電流脈密暫態測密如故障測密，：electro-thermal 爲主的故障模式等密： linking 如整同，撰寫數篇極具極量論文。
3. 寫續與 TSMC 同與 0.18μm /0.25μm/0.35μm 製程 EOS/ESD 晶護結構 研究，驗證並修改前述故障模式以因應 scaled process。

四、結論與討論

產出成果重點如下:

1. 至目前為止，已發表三篇 IEEE EDL，一篇 IEEE ED，一篇 IEEE IRPS，一篇 VLSI-TSA，一篇 IEEE IPFA，一篇 SSDM。
2. 一篇 GIDL 論文″New observation and the modeling of gate and drain currents in off-state P-MOSFETs,″ (IEEE ED May 1994)被日本三菱引用(全世界唯一)於 P-type Cell flash memory 之研發生產(1995 及 1996 IEDM)，今年科學園區亦引進 PMC 公司專門研發此新穎產品技術。
3. P-type flash cell 成果已漸次完成 self-consistent study，將撰論文發表。
4. 一系列高溫 epi CMOS 及 ESD 保護結構 Latch-up 之研究成果(包含 1997 IRPS)提至 TSMC 並其 design rules/manuals 建立。
5. 一系列 ESD/EOS characterization 及 modeling 已完成，具世界級貢獻，部分成果已獲 UMC 審核通過申請 ROC 及 USA 專利。
6. 蒙地卡羅模擬已成功解釋並重現超薄氧化層 TDDB 及 SILC。
7. 早期熱載子劣化預警器已在 TSMC 0.25 μm 製程實地驗證成功。

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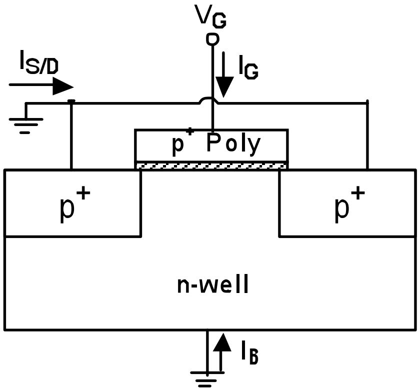

Fig. 1 Schematic illustration of the carrier separa technique. Under negative gate voltage, $I_{S/D}$ originated from either hole tunneling or impact ionization can be distinguished unambiguously through the direction of the current flow.

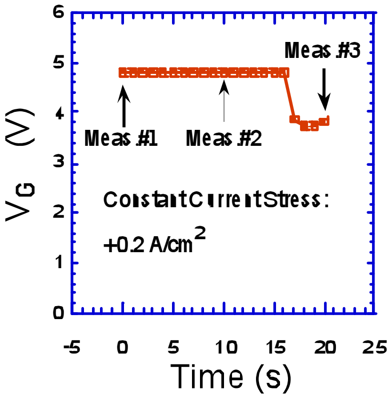

Fig. 2 Gate voltage versus time under constant current stress. A sudden change in gate voltage defines oxide breakdown.

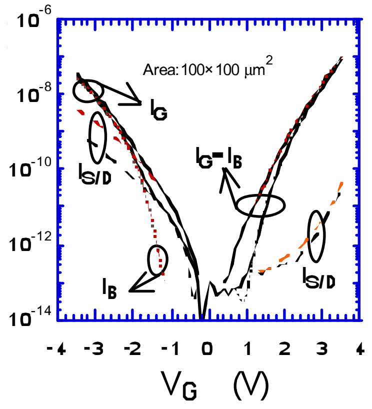

Fig. 3 Terminal current versus gate voltage monitored at two time points labeled Meas #1 & #2 in Fig. 2. Devices measured between +/- 3.5V gate voltage receive no further damages.

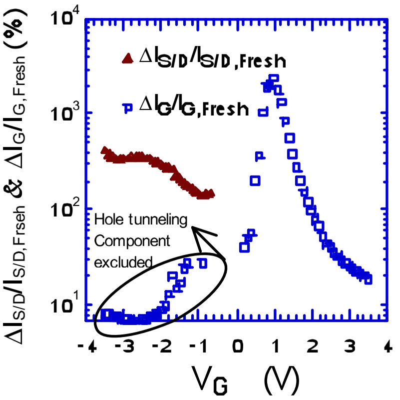

Fig. 4 Increment percentage of the gate and source/drain currents after stress. For $-V_G$, it is clear that the increment of gate current is originated mainly from its hole tunneling component (=S/D current increment).

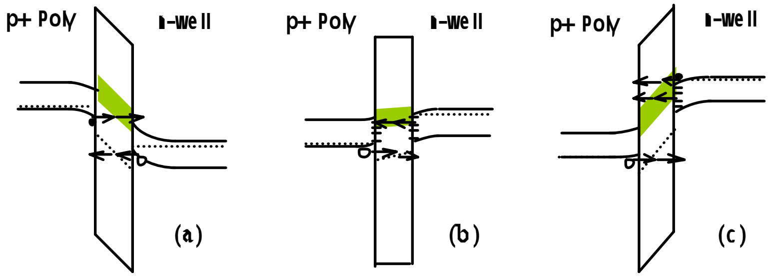

Fig. 5 Band diagrams for p^+ poly/pMOSFET structure (a) in inversion; (b) around flat band voltage; and (c) in accumulation. While in inversion or $-V_G$, the increment of gate current is originated mainly from the source/drain current component, indicating that an even deeper trap level (or band) exists for the enhancement of the hole tunneling. At around flat band voltage, electrons tunnel from the filled interface states to the empty ones on the opposite side [5]. In the mean time, hole density on the p^+ poly varies dramatically from $V_G<V_{FB}$ to $V_G>V_{FB}$; but no matter which, the injected holes into n-well as minority carriers contribute to no separable component. Finally, conduction band electron tunneling dominates the gate current at large positive V_G, and the tunneled holes can only be effectively collected near the

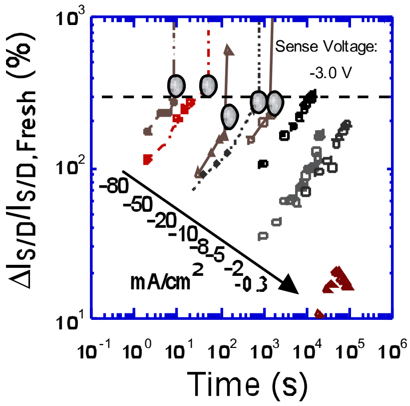

Fig. 6 The evolution of the relative hole trap density percentage in terms of $\Delta I_{S/D}/I_{S/D}$ for a series of constant stress current values. The increment percentage reaches a certain value of around 300%, suggesting a critical hole trap density to trigger catastrophic breakdown.

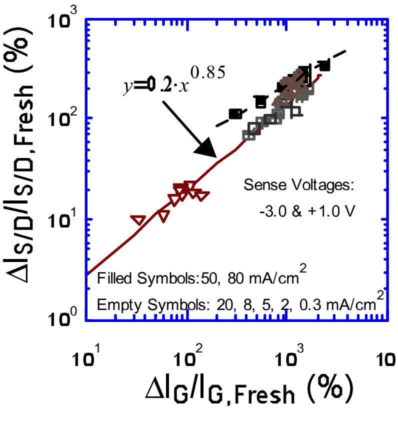

Fig. 7 Scatter plot between the relative hole trap density percentage and the relative interface state density percentage. Significant correlation exists between the two.

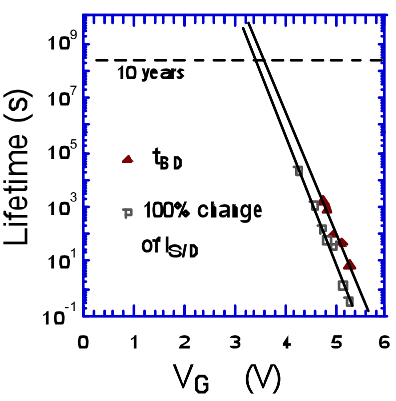

Fig. 8 Lifetime extrapolation according to time-to-breakdown (t_{BD}) and 100% change of $I_{S/D}$. Both show a similar prediction but the latter is more conservative.