# New Test Structure to Monitor Contact-to-Poly Leakage in Sub-90 nm CMOS Technologies

Ming-Chu King and Albert Chin, *Senior Member, IEEE*

***Abstract*—The high leakage or even direct short between contact and gate is a serious problem after the feature sizes are shrunk to 65-nm technology and beyond. However, there is no suitable test structure to effectively monitor the leakage current between them. We have designed a new test structure which can eliminate the drawbacks of existing test structures and effectively monitor the leakage current between contact and gate electrode in state-of-the-art CMOS process technology.**

***Index Terms*—Contact, gate, leakage current, test structure.**

## I. Introduction

THE technology scaling of CMOS process evolves with scaled feature size, thinner gate oxide thickness, and lower operation voltage. The number of transistors per chip has doubled every 18 months. As the feature size is scaled down, there is less tolerance for process control and it is more difficult to process monitor. Therefore, effective process monitoring capability is very critical for the success of process development and manufacturing [1]–[11].

The semiconductor manufacturing process is complicated and involves tight control on every process step. As the feature size is scaled, there is also smaller spacing between gate electrode and contact. The direct short between gate and contact is found to be a common phenomenon while the technology is scaled to 65 nm and beyond. In addition to direct short between contact and gate electrode, the leakage current along with smaller spacing is also a critical concern for 65-nm technology as shown on Fig. 1. The taper profile of contact will have a marginal spacing from the top of the gate. Therefore, better control of dimension and registration is a vital factor for both functional yield and Iddq. However, there is no suitable test structure to effectively monitor the actual leakage current between contact and gate electrodes. To effectively monitor the leakage current between contact and gate electrodes, we have designed a new test structure to eliminate the drawbacks of current test structures. This new test structure is a breakthough in monitoring the leakage current between contact and gate electrodes without suffering the gate leakage and pattern distortion issues on existing test structures. This new test structure is also scalable and can be applied to next-process generations.

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M. C. King is with National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: mingchu_king@hotmail.com).

A. Chin is with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: achin@cc.nctu.edu.tw).

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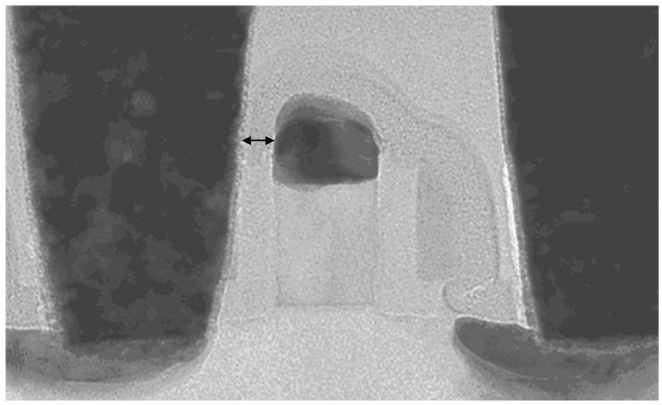

Fig. 1. TEM of marginal spacing between contact and gate electrode. Registration shift or pattern distortion will cause this failure.

## II. Test Structure Design

### A. Conventional Test Structures

There are two kinds of structures which are currently used to monitor the process margin between contact and gate electrodes in state-of-the-art processes. Fig. 2 shows the conventional test structure which is generally used to monitor if there is a direct short between contact and gate electrodes. However, the dominant leakage current of this test structure is the gate leakage current rather than the leakage current between contact and gate electrodes. For conventional CMOS transistors, lightly doped drain (LDD) was introduced to reduce the high electric field at the drain side and improve hot-carrier-injection effect. However, this kind of MOS transistor design will provide a conducting path from drain to the gate edge. The applied voltage between gate and drain will be across the gate oxide. This makes the gate leakage current the dominant leakage current while applying voltage between contact and gate electrodes on this kind of test structure. As the technology scaling keeps going, thinner gate oxide makes this situation even worse.

To resolve this gate leakage issue on conventional test structures, a modified test structure is also used to monitor the leakage current between contact and gate electrodes as shown in Fig. 3. The modified test structure is to put the transistor over the shallow-trench-isolation (STI) region which will not have any leakage issue due to the substrate, even though there is no gate leakage issue by this modified test structure. However, this kind of test structure cannot reflect the real situation. The gate patterning over the STI region will be different from the gate patterning over silicon due to the difference of focal plane and substrate reflectivity. Therefore, the real dimension is different from the actual dimension if the transistor is placed

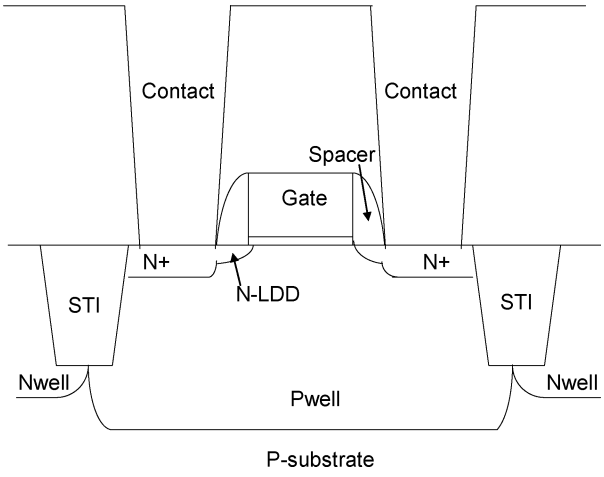


Fig. 2. Conventional test structure used to monitor the direct short and leakage current between contact and gate electrodes.

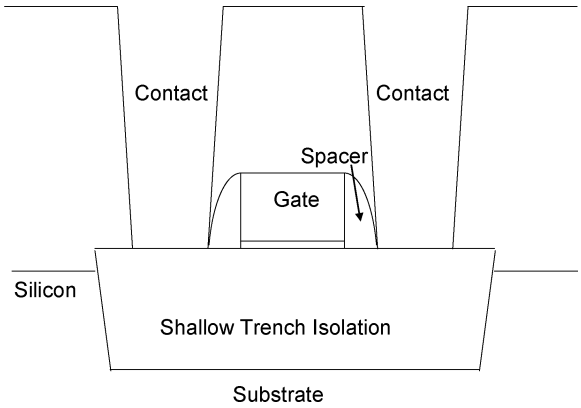


Fig. 3. Modified test structure used to monitor the direct short and leakage current between contact and gate electrodes. The transistor is placed above the shallow-trench-isolation.

over the silicon region. On the other hand, the contact etching will be etching the silicon dioxide rather than silicon. This will also cause different size at the contact bottom. Therefore, this kind of test structure cannot monitor the real situation. The monitored leakage is measured on the distorted patterns of both gate and contact patterning.

The other way to separate gate oxide leakage from contact-to-poly leakage is to design a test structure with relaxed poly-to-poly pitch. By designing a much larger poly-to-poly space for contacts, the possibility of poly-to-contact short will be minimized. However, while this will help to determine the gate leakage component, it will not supply any information about contact to poly leakage.

### *B. New Test Structure*

Fig. 4 shows the new test structure which can prevent the gate leakage issue and pattern distortion of existing test structures. The new test structure has the same physical structure as the real circuit. The difference of the new test structure is to remove the LDD implant in the conventional CMOS transistors. The LDD implant will form an electrical connection between source/drain (S/D) and gate edge. Any voltage applied on the S/D will be

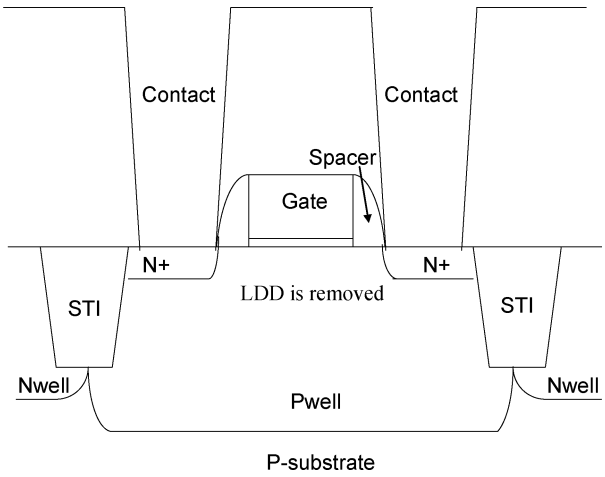


Fig. 4. New test structure designed to monitor the direct short and leakage current between contact and gate electrode. There is no LDD in the new test structure.

electrically connected to the gate edge. This new MOS transistor can be formed by masking the N-LDD lithography layer to block the whole test structure. This layer is the same as the conventional N-LDD implant layer in logic process. Therefore, there is no extra process cost for the proposed test structure.

By removing the LDD implant in the conventional MOS transistor, the applied voltage at the S/D side will cause an extended p-depletion region below the spacer region. Most of the applied voltage at S/D will be supported by the depletion region.

To understand how the new test structure can eliminate the gate leakage issue, we simulated an asymmetric-LDD device by MEDICI as shown in Fig. 5. Fig. 5(a) shows the asymmetric-LDD transistor which blocked LDD implant at the drain side. The Medici-simulated electrical potential (Fig. 5(b)) shows most voltage will be supported by the depletion region under spacer even when the drain is applied 3.3 V. Therefore, our new test structure incorporates a new MOSFET without LDD-implant to cut the leakage path between gate and source/drain regions.

## III. Experimental Results

The new test structure was processed on a 0.16-$\mu$m logic process technology with 0.15 $\mu$m gate length. Fig. 6 shows the top view of the test structure including active region, poly gate, and contacts. After the gate patterning, LDD and halo implants for both NFET and PFET are subsequently implanted following the lithography process. A Boolean operation is specially handled to block the new test structure while making the LDD mask. On the other hand, we also put the same test structure without blocking the LDD implants as a standard group to compare the electrical performance. The contacts are periodically placed on source and drain regions with a minimum rule from the gate. The metal-1 connects all the contacts at active region which will be used to measure the aggregate leakage current between contact and gate. The contacts are symmetrically placed beside the gate electrode. Therefore, the worst leakage current between contact and gate electrode can be detected no matter the registration shift is to the left or to the right side. By rotating the test structure 90°,

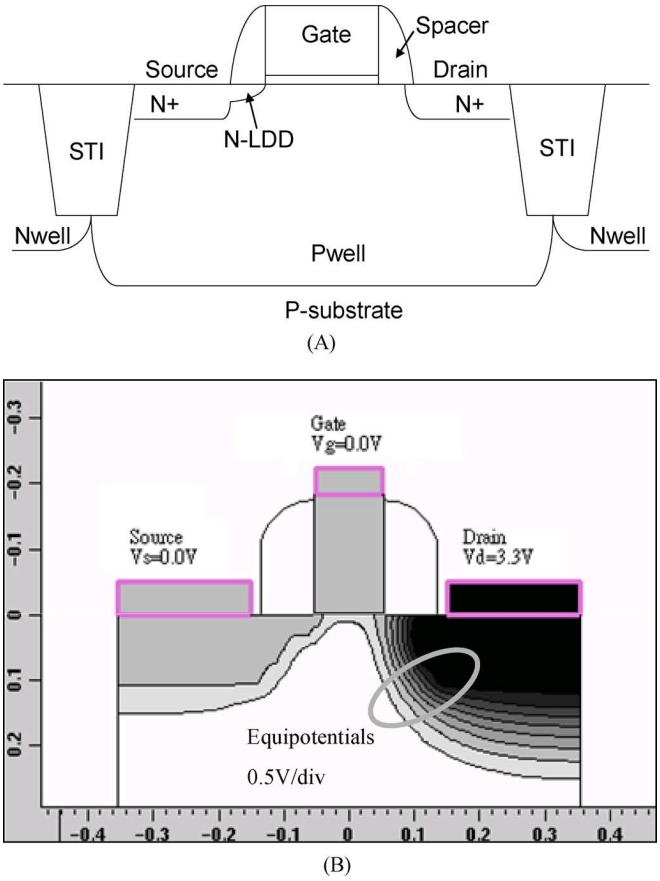


Fig. 5. (a) Asymmetric-LDD transistor. (b) Medici-simulated electrical potential of the transistor shown in (a). The applied voltage at drain side will be supported by the depletion region under spacer.

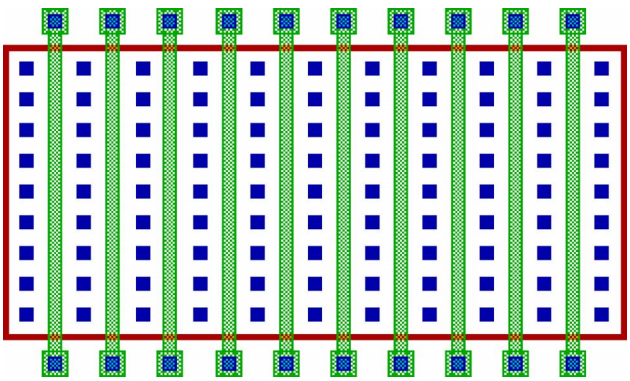

Fig. 6. Top view of the test structure to measure the leakage current of contact to gate electrode. The green lines are poly gate, blue squares are contacts, and the region within the red square is active region.

the new test structure can monitor the registration in a different orientation.

Fig. 7 shows the Ig-Vdg characteristics of a conventional test structure and a new test structure as shown in Fig. 6. The current at the gate node is measured with gate applied 0 V and varying the S/D voltage from $-1.8$ V to 1.8 V. The current at the gate node will be dominated by the gate leakage current as shown by the black square in Fig. 7. Therefore, the conventional structure can not effectively monitor the leakage current between contact and gate electrode. It also cannot distinguish the gate leakage

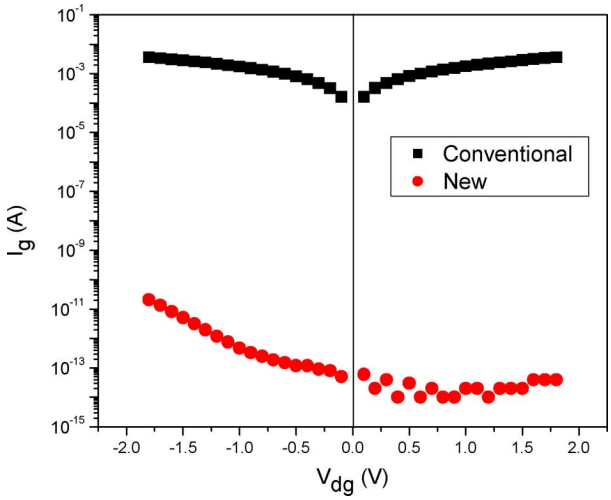


Fig. 7. Ig-Vdg characteristics of a conventional test structure where the leakage between gate and drain is dominated by the gate leakage. The new test structure showed a much lower leakage between gate and drain due to the designed potential barrier between drain and gate.

issue from the direct short between contact and gate electrode. The measured current at the gate node on new test structure is 10 orders lower than what was measured from conventional test structure. One important characteristic of the measured leakage current at the gate electrode is an asymmetric curve while the applied voltage is at the source/drain side. The leakage current is at the level of tenth fA while the source/drain is applied positive voltage. This is because the leakage path of gate leakage is blocked and the leakage current between contact and gate electrode is very small. If there is no abnormal process issue due to registration shift or contact sizing, the leakage current between contact and gate electrode will be close to the nondetectable region by the measurement equipment. The leakage current will increase monotonically while the source/drain side is applied negative voltage. This is because the negative voltage will decrease the depletion region under the spacer region. This decrease of the depletion region will create a shorter path for the gate leakage mechanism. Therefore, the best operation point for the new test structure with NFET is to measure the device with a positive voltage at the source/drain side while gate is grounded.

Our characterization results successfully proved our design. By a proper device design with a potential barrier between source/drain and channel, the dominant gate leakage at conventional test structure can be eliminated. The physical structure of the new test pattern is also the same as real circuit. Therefore, this new test structure does not distort the structure and can reflect the real situation.

The direct short of contact to gate electrodes is frequently observed during the process developing stage at 0.13 $\mu$m, 90 nm, and 65 nm. The presence of contact to poly leakage in additional to the existing gate leakage is an increasing challenge for process development. To make the process viable, contact profile optimization through optical proximity correction (OPC) and lithography/etching recipes are the keys. As technology scales further, smaller feature size requires better process tools with better process control. Our new test structure offers an effective process monitor vehicle to distinguish the dielectric leakage between contact and gate electrodes from

the gate leakage current which could not be achieved before. The experimental results also demonstrate a successful design of our new test structure for monitoring the leakage current of contact to gate electrode.

## IV. Conclusion

We have designed a new test structure to effectively monitor the leakage current between contact and gate electrodes. The new test structure can eliminate the existing issues on conventional test structures such as gate leakage and pattern distortion. A potential barrier between source/drain and channel is designed into the new test structure without extra process steps and added cost. The new test structure is also scalable and is suitable for process monitor in sub-90 nm process technology.

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**Ming-Chu King** received the B.S. degree in physics from National Taiwan University in 1992, the M.S. degree in electrical and computer engineering from the University of California at Santa Barbara in 1995, and the Ph.D. degree in electronics from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2007.

He joined Taiwan Semiconductor Manufacturing Company in 1995. He was a Process Integration Manager to ramp-up 0.18 $\mu$m, 0.15 $\mu$m, and 0.13 $\mu$m logic process technology in TSMC. He also developed 0.14 $\mu$m subnode logic process technology and 0.13 $\mu$m mixed-signal and RF process technology in 2002 and 2003, respectively. He was a Technical Manager for 65-nm process integration in the Logic Technology Division of TSMC R&D during 2004–2005. He is currently a Senior Manager with Qualcomm Communication Technologies, Ltd.

**Albert Chin** (SM'94) received the Ph.D. degree from the Department of Electrical Engineering, University of Michigan, Ann Arbor, in 1989.

He was with AT&T-Bell Labs from 1989 to 1990, General Electric-Electronic Lab from 1990 to 1992, and visited Texas Instruments' Semiconductor Process and Device Center (SPDC) from 1996 to 1997. He is a Professor at National Chiao Tung University, and visiting Professor at Si Nano Device Lab, National University of Singapore. He has published more than 300 technical papers and presentations. His research interests include Si VLSI, RF, and III-V devices. He is a pioneer in high-$\kappa$ gate dielectric and metal-gate research ($Al_2O_3$, $La_2O_3$, $LaAlO_3$ and HfLaON with NiGe, $YbSi_2$, and $Ir_3Si$ metal gates) for low dc power consumption CMOS. He invented the Ge-On-insulator (GOI) CMOS to enhance the mobility, 3-D IC to solve the ac power consumption and able to extend the VLSI scaling, resonant cavity photo-detector for high gain-bandwidth product, and high mobility strain-compensated HEMT. He is also the pioneer in high-$\kappa$ deep-energy trapping layer research [Al(Ga)N and HfON] for MONOS nonvolatile memory, where 100 $\mu$s fast program/erase speed, large memory window, and good retention are simultaneously achieved at record low $< \pm 5$ V write for SoC. The high-$\kappa$ TiTaO and STO MIM he developed with $k = 45 \sim 150$ can meet ITRS requirement of analog capacitor to year 2018. He also developed the ion implantation method to convert VLSI-standard Si substrate into semi-insulating, where much-improved RF device performance close to GaAs has been realized up to 100 GHz. He is currently working on quantum-trap nano MONOS memory, solar cells, high density MIM DRAM capacitor, metal-gate/high-$\kappa$ nano-CMOS, and RF Si technologies.

Dr. Chin has given invited talks at IEDM and other conferences in the U.S., Europe, Japan, Korea, etc. He also served as a committee member in IEDM.