電漿製程天線效應對超薄閘氧化層電晶體特性影響之研究

Study of Plasma Antenna Effect in Ultrathin Gate Oxides

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主持人: 林鴻志 毫微米元件實驗室 研究員

Email: hclin@ndl.gov.tw

中文摘要(關鍵詞: 電漿損害效應，超薄氧化層，崩潰電荷量)

本文研究探討電漿製程的充電損害效應對於氧化層厚度範圍由 87 埃到 25 埃元件的影響。當閘極氧化層 (gate oxide)厚度小於 4 0 埃後，傳統常用來偵測天線效應程度的電晶體參數，如臨界電壓 (threshold voltage，Vth)、互導 (transconductance，Gm)，及次臨界擺幅 (subthreshold swing，SS)等，都已不再適用。同時崩潰電荷量 (charge-to-breakdown，Qbd) 對於電應力之電流密度 (current density)，極性(polarity)及溫度(temperature)變得相當敏感。實驗結果顯示，當閘氧化層薄到 26 埃時，仍有嚴重的電漿損害發生。而負極性的電漿充電及高溫製程是造成損害的主要原因。

ABSTRACT

Charging damage induced in oxides with thickness ranging from 8.7 to 2.5 nm is investigated. Results of charge-to-breakdown (Qbd) measurements performed on control devices indicate that the polarity dependence increases with decreasing oxide thickness at room temperature and elevated temperature (180 ℃) conditions. As the oxide thickness is thinned down below 3 nm, the Qbd becomes very sensitive to the stressing current density and temperature. Experimental results show that severe antenna effect would occur during plasma ashing treatment in devices with gate oxides as thin as 2.6 nm. It is concluded that the negative plasma charging and high process temperature are the key factors responsible for the damage.

INTRODUCTION

Plasma charging effect, which may lead to severe oxide degradation during processing, has become one of major reliability concerns in ULSI manufacturing since the late 80's [1]~[7]. This can be ascribed to several reasons: (1) Oxide becomes very susceptible to charging damage as its thickness (Tox) is scaled below 10 nm. (2) Number of plasma steps employed in a chip fabrication increases significantly as the chip functionality and complexity advance. (3) In order to promote the throughput or to meet the critical requirements of deep-submicron manufacturing, process tools with high plasma current density, such as high current implantor and high-density plasma (HDP) reactors for etching and deposition applications, are increasingly used. These process steps may potentially aggravate the extent of charging.

When entering sub-quarter micron era (Tox < 6 nm), the oxide thickness dependence of plasma charging damage presents an important and controversial topic. Park and Hu studied the damage induced in oxides (2.2 nm < Tox < 7.7 nm) during metal and contact etching processes and indicated that thinner oxide has superior immunity [3]. Alavi *et al.* showed that, as oxide is thinned down, the damage increases up to a point (~4 nm), and then decreases due to direct tunneling [4]. Similar results were also found by Noguchi *et al.* in investigating the electron shading effect [5]. On the other hand, the results of Bayoumi *et al.* [ref. 6, Tox range: 8 ~ 4 nm], Krishinan *et al.* [ref.7, Tox range: 6 ~ 3.5 nm] and Chien *et al.* [ref. 8, Tox range: 8 ~ 4 nm] showed that susceptibility of oxide to damage increases with decreasing oxide thickness. More recently, Krishinan *et al.* further indicated that severe damage could be induced in gate oxide as thin as 2.1 nm under certain ICP metal etch process conditions [9]. These different findings are understandable since the process conditions and equipment configurations can be very different from one study to another. Meanwhile, degradation characteristics of oxide under high field stressing may change significantly as Tox is thinned down and, thus, different kinds of indicators, e.g., charge-to-breakdown (Qbd), breakdown field, threshold voltage (Vth), etc., used to characterize the damage may lead to a very different outcome.

This study is intent to make the picture of Tox-dependent charging damage more clear. Important factors including stress polarity, temperature, and stress current level are investigated. Device parameter measurements were also performed on n-channel transistors with Tox ranging from 8.7 to 2.5 nm. Charging damage induced during photoresist (PR) removal step in a down-stream reactor is also studied and analyzed.

DEVICE FABRICATION

N-channel transistors with n^+ poly-Si gate were fabricated on 6 in. Si wafers. The oxides were grown in O_2/N_2 (1/6) furnace ambient at temperature ranging from 800 ~ 900 ℃. Oxide thickness ranging from 2.5 to 8.7 nm was determined by the ellipsometry and TEM methods on the monitor wafers. Figure 1 shows a TEM example of a 2.5 nm-thick oxide. The oxide thickness was also checked by the F-N I-V fitting (Fig.2) [10] [11] method, which takes the poly-depletion effect into account, on the fabricated devices. Typical examples are shown in Fig.2. Consistent results are obtained among these methods.

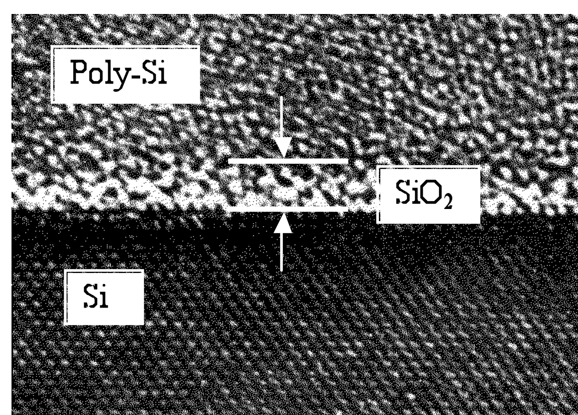

Fig.1 TEM photo of a 2.5 nm-thick oxide layer.

Metal pads with various surface areas are connected to the poly-Si gate electrode of these n-channel transistors and act as the antenna. These metal patterns were defined with wet processing and then the PR layers were stripped off with the O_2 plasma in a down-stream asher. The process temperature is 200 ℃ during ashing. Charging

damage could be induced in this treatment and is analyzed by use of antenna devices. The antenna area ratio (AAR) is defined as the area ratio between the metal pad and the active region. In this study, the "control devices" are referred to those with small AAR values (e.g., AAR < 20), assuming the induced damage is negligible in these samples.

Fig.2 Typical current-voltage characteristics of ultrathin oxides and the F-N current fitting curves.

Tox DEPENDENCE ON Qbd CHARACTERIZATION

Constant current stressing was employed in this work to explore the time-dependent-dielectric breakdown (TDDB) characteristics of ultrathin oxides. This method is appropriate for characterizing the charging damage since it has been pointed out that the plasma charging may more likely act as a non-ideal current source [12]. It is noted that, as oxide is thinner than 5 nm, soft breakdown is induced predominantly instead of hard breakdown [13][14]. During this study, it is further found that the failure events after stressing were entirely soft breakdown as oxide is thinned down below 4 nm, consistent with the results of a recent report [15].

Figure 3 shows the effect of stress polarity on the Qbd results measured at 25 and 180 ℃, respectively. The magnitude of stressing current density is fixed at 1 A/cm^2. The polarity dependence means the difference in Qbd values between that obtained by gate injection (Vg < 0) and substrate injection (Vg > 0). It has been well documented in previous reports [16][17] that the polarity dependence increases with decreasing Tox for oxides thicker than 4 nm, and is ascribed to the different properties between the poly-Si/oxide and oxide/Si interfaces. In this study, we observe that, as oxide is further scaled down, the polarity dependence becomes even stronger at both 25 and 180 ℃, as shown in Fig.3. This is mainly due to the rise in Qbd under substrate injection condition as oxide is thinned down, while the Qbd under gate injection stressing remains relatively unchanged.

Fig.4 shows the effects of stress current density and temperature on Qbd under gate injection stressing. It is found that, Qbd of 2.6 nm-thick oxides is about three orders higher in magnitude than those of thicker oxides under current density of -0.2 A/cm^2 (Vox ~ 2.9V for Tox = 2.6 nm) at room temperature, indicating the higher tolerance to high field under DT process. However, when temperature is raised from room temperature to 180 ℃, Qbd of

Fig.3 50% charge-to-breakdown measured at 25 and 180 ^{0}C as a function of stress polarity and oxide thickness. AAR of the test samples is 4.

Fig.4 50% charge-to-breakdown measured at 25 and 180 ℃ under gate injection of -0.2 and -1 A/cm^2, respectively, as a function of oxide thickness. AAR of the test samples is 16.

2.6 nm-thick oxides (J = -0.2 A/cm^2) is only about one order higher in magnitude than that of thicker oxides. This implies that the temperature acceleration effect is very significant for ultrathin oxides under direct tunneling (DT) stressing. Such effect is not clearly understood, and could be possibly related to the properties of oxide/Si interface, since it has been pointed out that the injected electrons may release energy at the interface [18].

By increasing the current density to - 1 A/cm^2 (Vox~3.4 V) the thickness dependence on Qbd shown in Fig.3 is not significant at room temperature while a drop in Qbd is observed at 180 ℃ as Tox is scaled down. This means that, under the F-N stressing, thinner oxides may suffer more damage as temperature is raised. In addition, current density dependence of Qbd is also reduced at high temperature. For oxide thinner than 3 nm, although not as strong as that in in DT stressing, the temperature

acceleration effect is also very significant. The temperature effect has been reported previously[19][20]. In this study, however, we find that its role would be even more important as oxide is scaled below 4 nm, thus more attention should be paid in this aspect.

Fig.5 Wafer maps of (a) negative and (b) positive potential values recorded by CHARM-2 sensors.

CHARGING DAMAGE INDUCED DURING ASHING

In this work, we characterized the charging damage induced in oxides during a photoresist (PR) stripping step in an RF down-stream O_2 plasma asher. Previously, we have investigated this system and found that severe antenna effect could occur at the wafer center[8][21]. The cause of damage is presumably due to the non-uniform plasma generation resulted from the gas injection mode of the asher[22]. This is supported by results of CHARM-2 monitor wafers. As can be seen in Figs.5(a) and (b), the CHARM-2 sensors recorded high positive and negative potential values at the wafer edge and center, respectively. In the experiments, however, no significant damage is found in devices located at the wafer edge where positive charging is incurred. This can be ascribed to the strong polarity dependence shown in Fig.3.

Fig.6 shows the Qbd as a function of device location and antenna area ratio for oxides with thickness ranging from 4 to 8.7 nm. Each datum represents the average result of several measurement sites with identical distance-from-center. Constant current stressing was performed with -0.2 A/cm^2. It is noted that the Qbd of devices with small AAR of 16 is essentially independent of position and, therefore, can be regarded as a damage-free reference, confirming our assumption made in previous section. For devices with large AAR (10K), significant damage begins to appear at the wafer center as oxides is scaled below 6 nm and, for 4 nm-thick oxides, oxide breakdown is induced at the wafer center.

Charge-to-Breakdown (C/cm^2)

Distance-from-center (cm)

Fig.6 Position dependence of charge-to-breakdown as a function of oxide thickness (4 ~ 8 nm) and antenna area ratio. (solid circle : AAR = 10 K; open circle : AAR = 16)

Characteristics of Qbd for oxides with thickness ranging from 4 to 2.6 nm are shown in Fig.7. For efficient characterization, these devices were stressed either to breakdown or to a value of 5000 C/cm^2 if the oxides are not failed with stress current density of -0.2 A/cm^2. Stressing with -1 A/cm^2 is also performed on the devices with 2.6 nm-thick oxide. It is observed in this figure that oxide breakdown occurs in large antenna devices at the wafer center regardless of oxide thickness. As oxide is thinned down to 2.6 nm, Qbd higher than 5000 C/cm^2 is observed for samples with small AAR of 16 (not shown) and for samples with AAR of 10 K but away from the center region under - 0.2 A/cm^2 stress condition. In these devices, the abrupt increase in Qbd as compared to that obtained under -1 A/cm^2 stress condition is explained by the higher tolerance to tunneling current stressing in DT (-0.2 A/cm^2) process. Nevertheless, the results shown in Fig.7(c) clearly indicate that severe antenna effect is induced at the wafer center.

Charge-to-Breakdown (C/cm^2)

Fig.8 Charge-to-breakdown results of antenna devices as a function of oxide thickness. The test cells where the large antenna devices (AAR = 10 K) are located are shown in the top portion of the figure. Each datum represents the average result of several measurements.

Fig.7 Position dependence of charge-to-breakdown as a function of oxide thickness (4 ~ 8 nm) and antenna area ratio. (solid circle: AAR = 10 K; open circle: AAR = 16)

Oxide thickness dependence on Qbd is illustrated in Fig8, in which the average results obtained from control and damaged (AAR = 10000) samples are shown and compared. The damaged samples are located in the nine cells (shown in this figure) at the wafer center. Constant current stressing of -0.2 A/cm^2 current density is performed on these devices. It is seen that, for oxides thicker than 3 nm, Qbd of control samples is relatively independent of Tox, while that of damage samples decreases with decreasing Tox. When Tox is thinned down to 2.6 nm, Qbd of control devices rises significantly due to the transition of stress condition from FN (Tox $\geq$ 3nm) to DT process, as mentioned earlier. Nevertheless, the remaining Qbd measured from the damage samples is much smaller. From the

Fig.9 Threshold voltage, subthreshold swing, and transconductance as a function of cell position. Antenna area ratio of the devices is 20 K. Oxide thickness is 2.5 nm.

results shown in Figs.3 and 4, it is understood that the damage characteristics of thinner oxides are very sensitive to stress polarity, current density (or oxide field), and temperature. The antenna effect shown in Figs. 6 ~ 8 can thus be mainly ascribed to the strong negative plasma charging (supported by the results of CHARM-2 monitors shown in Fig.5), and elevated process temperature (200 ℃). The latter factor could be even more important since the associated acceleration effect is very significant under both FN and DT charging stress conditions.

The above analysis is mainly based on the Qbd characterization. When other indicators are used, the feature of outcome might be different. This is shown in Fig.9, in which the Vth, subthreshold swing (SS), and transconductance (Gm) of transistors with Tox of 2.5 nm and AAR of 20 K are shown as a function of device location. There seems to be no degradation in this plot. However, when Qbd is used to characterize these devices, as shown in Fig.10, significant antenna effect is identified. Such finding is ascribed to the significant decrease in the rates of trap creation and interface state generation under high-field stressing as oxide is scaled down[17]. It is noted that the breakdown events found in the measurements of Fig.10 all belong to the soft-breakdown type, consistent with the findings shown previously [15] and in previous section. Typical Vg-t curves during constant current stressing are illustrated in Fig.11. It is seen that soft breakdown with noisy characteristics [15] appears for large antenna device from the beginning of stressing. Interestingly, subthreshold characteristics of a transistor with such thin oxide depict little changes even after the charge-to-breakdown test. An example is shown in Fig.12, in which the Vth, SS, and Gm remain almost unchanged after oxide is stressed to soft-breakdown. Similar results were also reported recently [15][23]. The only important factors in ULSI manufacturing when gate oxide is scaled parameter that depicts significant change shown in the figures is the gate leakage (Ig), which increases significantly after oxide breakdown. This could explain the different outcomes between Figs.9 and 10 in monitoring the antenna effect.

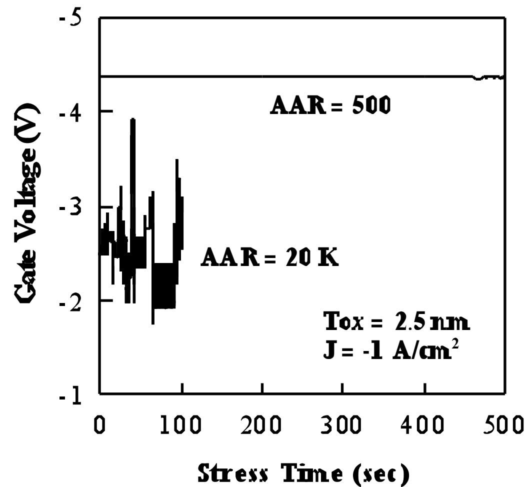

Fig.11 Gate voltage variation during constant current stressing for devices located at the wafer center with small (AAR= 500) and large (AAR = 20 K) antenna.

Fig.10 Charge-to-breakdown values as a function of cell position Channel length and width of the measured transistor are 1.2 and 10 μm, respectively.

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Fig.12 Drain and gate current as a function of gate voltage measured (a) before and (b) after charge-to-breakdown test. Channel length and width of the measured transistor are 12 and 10 μm, respectively.

CONCLUSIONS

In this study we have investigated effects of stress polarity, temperature, and current density on the charge-to-breakdown characteristics of oxides with thickness ranging from 2.5 to 8.7. It is shown that the stress polarity dependence increases with decreasing oxide thickness at both 25 and 180 ℃. This indicates that negative plasma charging may produce far more severe damage than positive plasma charging as oxide is thinned down below 4 nm, as is evidenced by the experimental results. The acceleration effect of temperature is also found to be very significant as oxide is scaled down. Severe damage could thus be induced in ultra-thin oxides at elevated process temperature condition even under DT stressing condition. Based on the experiment findings, we conclude that the plasma uniformity and process temperature are the two most down. It is believed that more attention should be paid on the plasma steps which are operated at raised temperature, such as ashing or other CVD steps, when the gate oxide is scaled below 3 nm.

We have also compared the usefulness of several indicators in revealing the antenna effect. It is found that traditional methods of monitoring transistor parameters, including Vth, SS, and Gm, may not be appropriate for detecting the charging damage in ultrathin gate oxides. Consequently, some destructive methods, such as the charge-to-breakdown measurement, or the noise characterization techniques [9][15], are necessary to evaluate plasma damage in the ultrathin oxides.

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