5 GHz quadrature voltage-controlled oscillator using trifilar transformers

J.-S. Syu, C. Meng, K.-C. Tsung and G.-W. Huang

A 0.18 μm CMOS 5 GHz quadrature voltage-controlled oscillator (QVCO) is demonstrated by using trifilar transformer coupling. The trifilar transformers composed of one primary coil and two secondary coils are used to separate the gate and drain bias for output voltage swing optimisation and also replace a conventional transistor-coupling method for quadrature output generation simultaneously. As a result, the trifilar-coupling QVCO achieves 180.1 dBc/Hz figure of merit (FOM) at the supply voltage of 1.2 V. The on-chip passive single sideband upconversion mixer is also demonstrated to fairly measure the quadrature accuracy of the QVCO. Thus, a 33.7 dB sideband rejection ratio is achieved.

Introduction: A higher inductor quality factor results in better phase noise performance for an LC voltage-controlled oscillator (VCO). The transformers consisting of two inductors with strong mutual coupling can provide a higher quality factor for each inductor. Moreover, the VCOs with transformers [1] at drains and gates of the cross-coupled differential pairs can separate each DC bias for an output voltage swing optimisation.

Transistor-coupling methods (including the parallel coupling topology [2] and series coupling topology [3]) are commonly used for a quadrature voltage-controlled oscillator (QVCO) design but with extra undesirable effects (including parasitic capacitance, device noise, and extra power consumption). The transformer-coupling method [4, 5] is applied to avoid these undesirable effects and is suitable for low supply voltage applications. Furthermore, the trifilar transformer [6] consisting of three coils (one primary coil and two secondary coils) is utilised in this work to merge the above advantages. The QVCOs with trifilar transformer couplings at drains, gates and sources are demonstrated for the first time, to the best of our knowledge.

Circuit design: The schematic of the QVCO based on trifilar coupling is shown in Fig. 1. The trifilar-coupling QVCO consists of two cross-coupled differential VCOs ($DVCO_I$ and $DVCO_Q$) and two trifilar transformers (TF_1 and TF_2). Each trifilar transformer is composed of three centre-tapped symmetric inductors (one primary coil P and two secondary coils S_1 and S_2) which provide balanced input/output signals. The demonstrated trifilar transformer is designed and simulated by Sonnet EM simulation.

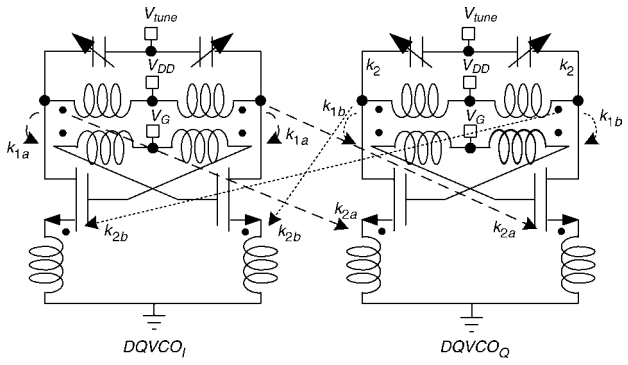

Fig. 1 *Schematic of trifilar-coupling QVCO*

Mutual coupling for one trifilar transformer depicted by dashed line; the other trifilar transformer depicted by dotted line

The primary coil (P) of the trifilar transformer TF_1/TF_2 is used as a centre-tapped symmetric inductor load while one of the secondary coils (S_1) of TF_1/TF_2 is connected to the gates of each $DVCO_I/DVCO_Q$ for gate and drain bias separation. The other secondary coil (S_2) of the TF_1/TF_2 is in-phase/anti-phase connected to sources of $DVCO_Q/DVCO_I$, respectively. All the DC bias of the drains, gates, and sources is fed from the centre-tap node of each inductor of the trifilar transformer. The start-up time of the QVCO is about 3 ns by ADS transient simulation.

To fairly measure the quadrature accuracy at high frequencies of the proposed trifilar-coupling QVCO, the on-chip passive single-sideband (SSB) upconverter is implemented [2]. The IF differential quadrature inputs are generated by the off-chip quadrature coupler and the on-chip active balun (balance to unbalance transformer). The photograph of the trifilar-coupling QVCO using TSMC 0.18 μm CMOS technology is shown in Fig. 2. The die size is 1.2×1.31 mm^2. The symmetric layout is necessary for better performance.

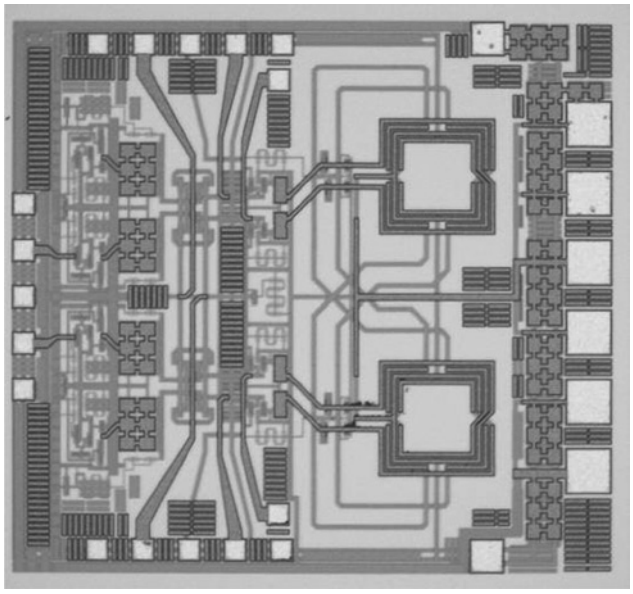

Fig. 2 *Photograph of trifilar-coupling QVCO with SSB upconverter*

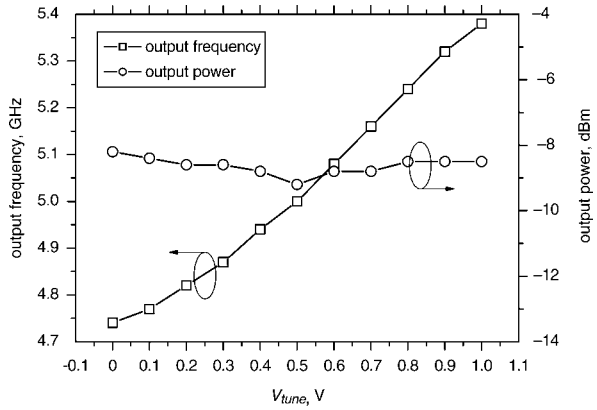

Fig. 3 *Output frequency and power of trifilar-coupling QVCO with respect to tuning voltage*

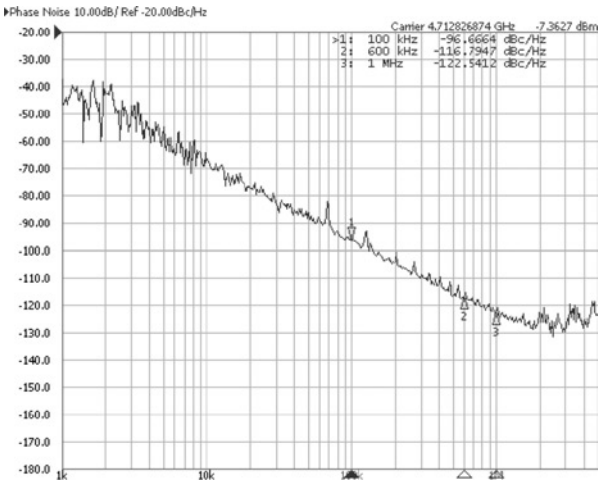

Fig. 4 *Phase noise spectrum of trifilar-coupling QVCO*

Measurement results: The output frequency and power with respect to the tuning voltage of the trifilar-coupling QVCO is shown in Fig. 3. The VCO output power is around −8 dBm and the output frequency

changes from 4.74 to 5.38 GHz for the tuning voltage from 0 to 1 V with the KVCO of 640 MHz. The core current consumption is 35 mA at the 1.2 V supply. The phase noise spectrum of the trifilar-coupling QVCO is shown in Fig. 4; the phase noise is −122.5 dBc/Hz at 1 MHz offset frequency. The phase noise figure of merit (FOM) is 180.1 dBc/Hz. The measured sideband rejection ratio is 33.7 dB after the SSB upconverter with the quadrature IF = 119 MHz and the sideband rejection ratio is equivalent to about 2.3°quadrature phase error.

Conclusion: The trifilar-coupling QVCO achieves gate and drain bias separation for optimal output swing and in-phase/anti-phase quadrature coupling instead of transistor-coupling simultaneously. The trifilar-coupling QVCO is demonstrated by using TSMC 0.18 μm CMOS technology.

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