行政院國家科學委員會研究計畫成果報告

計畫題目: 次兆分之一秒響應之研究

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主持人：荊鳳德教授　執行單位：交通大學電子工程系　學生：梁竹欣

一、　中文摘要

我們利用次兆分之一秒暫態反射率量測法來測量在矽晶片上的載子生存期之兆分之一秒的光反應.其中離子佈植最高濃度必須至少$10^{16}$$cm^{-2}$.在這種濃度下,分別經由砷離子佈植及 400℃ 退火的載子生存期可以量到0.9和1.4兆分之一秒.經過退火的晶片,載子生存期之所以會增加可以解釋為捕捉中心濃度降低,表面電阻亦顯示出與退火的溫度有密切相關.而我們也發現降低表面電阻（大約一百倍）亦可以降低跳躍式傳導,其中我們主要利用較低的離子濃度來達到較低的表面電阻值.

關鍵詞：兆分之一秒載子光反應,載子生存期

Abstract

Picosecond photoresponse of carriers in Si ion-implanted Si samples has been measured using femtosecond transient reflectivity measurement. A threshold peak implant dose of 10~6 cm^{-2} is required to achieve picosecond carrier lifetime. At this dosage, carrier lifetimes of 0.9 and 1.4 ps are measured for the as-implanted and 400°C annealed Si substrates, respectively. The increase in carrier lifetime upon annealing is attributed to the reduction in the concentration of trap and recombination centers. Sheet resistance also shows a strong dependence on the annealing temperature. An eightfold increase in sheet resistance is obtained for annealed samples, and a reduction in hopping conduction, manifested by the $e^{-1/T}$ temperature dependence, may be responsible for the increase in resistance. Further evidence of decreasing hopping conduction can be also observed from the more than two orders of magnitude in reduction of sheet resistance as the peak dosage decreases from 10^{16} to 10^{14} cm^{-2}. **This paper was published at Appl. Phys. Lett.**

keywords : picosecond photoresponse of carrier, carrier lifetime

二、　緣由與目的

There has been a considerable interest in the development of semiconductor materials[1-6] that are suitable for ultrafast electronics and optoelectronics,[7] and to date, devices with speed near terahertz[8] have also been demonstrated. The basic requirement in the material development to achieve ultrafast response is having created a high concentration of defects, deep levels, and recombination centers[1-6] that can effectively reduce the carrier lifetime. III-V materials grown at low temperature (LT) by molecular beam epitaxy technique have been studied extensively for this application.[1-4,6] The as-grown LT-GaAs is nonstoichiometric and highly defective, with excess As and a large concentration of point defects formed during growth.[9,10] Postgrowth annealing reduces the concentration of point defects and As precipitates form. Ultrafast photoresponse of both as-grown and, subsequently, annealed LT-GaAs has been reported,[11,12] where the increased carrier lifetime upon annealing is attributed to the reduced concentration of defects and the formation of arsenic (As) precipitates. Another method to generate excess As in GaAs is by implanting As into GaAs[13] and As precipitates also form after annealing. A very fast photoresponse of 220 fs was obtained in the As ion implanted GaAs,[14] which is close to that measured in the LT-grown GaAs.

In addition to the fast photoresponse, hopping conduction as determined by the resistivity measurement has been observed in the As-implanted GaAs.[15] Obviously, implant-induced defects play a role in both reducing carrier lifetime and altering the electrical conduction mechanism. Since developing a Si-based material having fast photoresponse is attractive in realizing a monolithic integrated high-speed optoelectronic receiver on the Si substrate, research on implanted Si is of great interest. In this letter, we report the study of carriers in Si implanted with Si ions by the photoresponse technique and resistivity measurement.

三、 實驗方法

Since there is no semi-insulating Si available, P-type [100] Si was used for this study. Multiple Si ion implants with different ion energies are used to achieve a uniform profile of ~0.5um by computer simulation.[16] To generate different concentrations of defects, three sets of implant dosages are used: (1) 3×10^{15}, 5×10^{15}, and 10^{16} cm^{-2} for the highest dose, (2) 3×10^{14}, 5×10^{14}, and 10^{15} cm^{-2} for the middle dose, and (3) 3×10^{13}, 5×10^{13}, and 10^{14} cm^{-2} for the lowest dose, for ion energies of 80, 160, and 300 keV, respectively. At high implanted doses, it is generally shown that the Si substrate may become amorphous and the solid-phase recrystallization occurs at annealing temperatures between 500 and 600°C.[17] Therefore, we have chosen in this work annealing temperatures at 400, 600, and 800°C, which are below, equal, and above the temperature of starting recrystallization, to evaluate the optimum temperature as far as carrier lifetime is concerned. Harmon *et al.*[6] in a similar work, have shown that carrier lifetime in LT-GaAs exhibits a strong dependence on the annealing temperature. Our samples are generally annealed in a nitrogen ambient for I h, and the transmission line model (TLM) is applied to measure the sheet resistance. The interspacing distances of the TLM patterns are 2.5, 5, IO, 20, and 50 ,um. Prior to the deposition of ohmic metals for the contact pads, samples are cleaned with a H2SO4/H2O2 cleaning solution and, subsequently, followed by a 1:5 HF/H2O dip. The final HF dip serves another important purpose, to passivate the Si surface by HF atoms and to avoid the formation of a thick native oxide. A thick layer of native oxide is undesired for the formation of ohmic contact that will then require either higher temperature or longer sintering time. Either one should be kept to its minimum because the distribution of implantation induced defect is very sensitive to any postimplant annealing. For that we have applied a low sintering temperature of 400°C and a short time of 10 min to form the ohmic contacts.

The photoresponse of implanted Si is measured using fs time-resolved photoreflectance. The measurement setup is similar to the previously published study of ion implantation in Si on sapphire [18] A 100 fs mode locked Ti:sapphire laser provided the excitation pulses. A sampling pulse train was derived from the excitation pulse with a variable delay for the external optical probe. The probe beam is polarized perpendicular to the pump beam in order to eliminate coherent diffraction effects. The reflectance of the probe beam is measured by a Si photodiode with a locking amplifier. Transient photoresponse of carriers were calculated from the 1/e fall time of the photoresponse. The setup has been calibrated by measuring the photoresponse of a LT-GaAs grown at 220°C. The measured 1/e fall time of 0.4 ps is comparable to the published results.4 A more detailed description of the pump-probe experiment will be published elsewhere. In order to make a meaningful comparison among the experimental data, all samples were measured in successive runs under as identical measurement conditions as possible.

四、 結論與討論

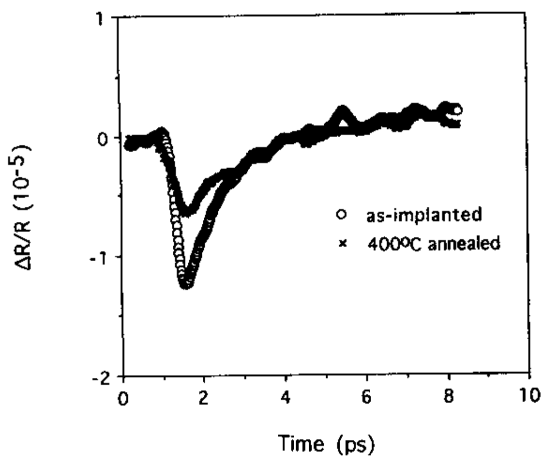

FIG.1. Femtosecond response of as-mplanted and 400°C annealed si. There is no photoresponse relaxation up to 1 ns for annealing temperatures above 600°C. The implanted doses are 3×10^{15}, 5×10^{15} and 10^{16} cm^{-2} at energies of 80, 160, and 300 kev, respectively.

Result

Figure I shows femtosecond transient photoreflectivity for the as-implanted and 400°C annealed Si at a peak implant dose of 1016 cm 2. Carrier lifetimes of 0.9 and 1.4 ps are measured for the as-implanted and 400°C annealed Si, respectively. The 0.9 ps carrier lifetime in the as-implanted Si is of the same order to the measured 0.4 ps in our LT-GaAs reference. A similar increase in carrier lifetime upon annealing is also observed in LT-GaAs, which is attributed to the formation of As precipitates and the reduced concentration of defects and trap centers.[6] The small but abovebaseline photoreflectance relaxation at long decay times may be due to the lattice heating by trapped carriers [14,19] The small increase is also observed in photoreflectance studies of LT materials.[1,6]

The relative intensity of photoresponse of ion-implanted Si decreases by a factor of 2 after 400°C annealing, and it decreases further to the noise level for samples annealed at above 600°C. We have also conducted the experiments on samples implanted at peak dosages of 10^{14} and 10^{15} cm^{-2}. However, no measurable photoresponses are detected. The threshold peak implant dose of 10^{16} cm^{-2} is, thus, determined to be required to achieve a ps carrier lifetime.

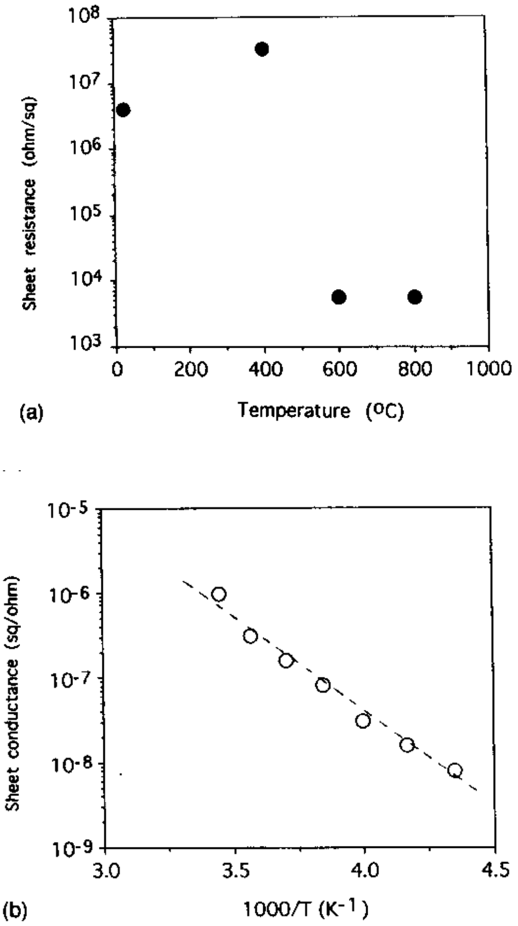

FIG. 2. (a) measured sheet resistance of as-implanted, 400,600, and 800 °C annealed Si, and (b) The Arrhenius plot of sheet conductance.

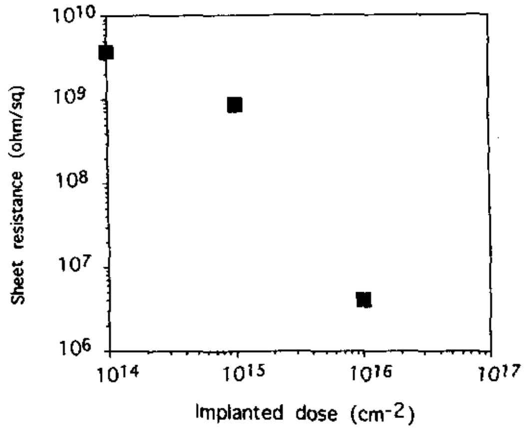

FIG 3. Measured sheet resistance as the function of peak implanted dosage.

We have also measured the sheet resistance to further understand the relationship among the photoresponse, annealing temperature, and implant dose. Figure 2(a) shows the dependence of sheet resistance on annealing temperature at a peak implant dose of 10^{16} cm^{-2}. The resistance reduces from 4x 10^{16} Q/sq for the as-implanted to 5000Q/sq for samples annealed at temperatures above 600°C. The reduction of sheet resistance may be due to the solid phase regrowth that occurs at temperatures above 600°C for Si implanted with high doses. It is suggested that this measured resistivity in annealed samples is very close to that from the substrate, indicating that the implanted Si layer has recrystallized. It is, therefore, proposed that no measurable photoresponse relaxation on these particular samples may be due to the solid phase regrowth after annealing at temperatures above 600°C In general, the typical carrier lifetime of indirect Si is ~us, which is beyond the capacity of the photoresponse measurement system. In contrast, an eightfold increase in sheet resistance is observed after 400°C annealing. Such unusual dependence of sheet resistance on the annealing temperature cannot be explained by the normal conduction mechanism of carrier transport in metal-semiconductor junctions. We have, therefore, measured the temperaturedependent sheet conductance on the as-implanted sample to study the conduction mechanism. Figure 2(b) shows the Arrhenius plot of sheet conductance. An exp($-\Delta E/KT$) dependence has been found, and an activation energy ΔE of 0.45 eV is measured that indicates the carrier transport is dominated by the fixed-range hopping conduction.[155,20] Hopping conduction is commonly observed in highly defective as grown Lt-GaAs and As ion-implanted GaAs, and depends strongly on the concentration of defects. Therefore, the increase in sheet resistance when annealed at 400°C in this study is attributed to a reduction in implant-induced defects that decrease the hopping conduction.[21,22]

The dependence of the implanted dose on sheet resistance is further investigated. Figure 3 shows the measured sheet resistance on the peak implant dosage. A decrease in sheet resistance of more than two orders is observed as the peak implant dose increases from 10^{14} to 10^{16} cm^{-2} The unusual dependence can be again explained by incorporating the hopping conduction mechanism as the concentration of defects and traps increases and the resistance decreases with the increasing implant dose. Consequently, an increase in defects and traps also reduces the carrier lifetime.

Conclusion

In summary, we have studied the ps photoresponse of carriers in Si ion-implanted with Si. A minimum dose of 10^{16} cm^{-2} is required to achieve ps photoresponse. The measured carrier lifetime as well as the sheet resistance depend strongly on the annealing temperature. The increase in carrier lifetime after annealing at 400°C is attributed to the reduced concentration of defects and traps that in turn reduces the contribution by hopping conduction leading to an increase of sheet resistance

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