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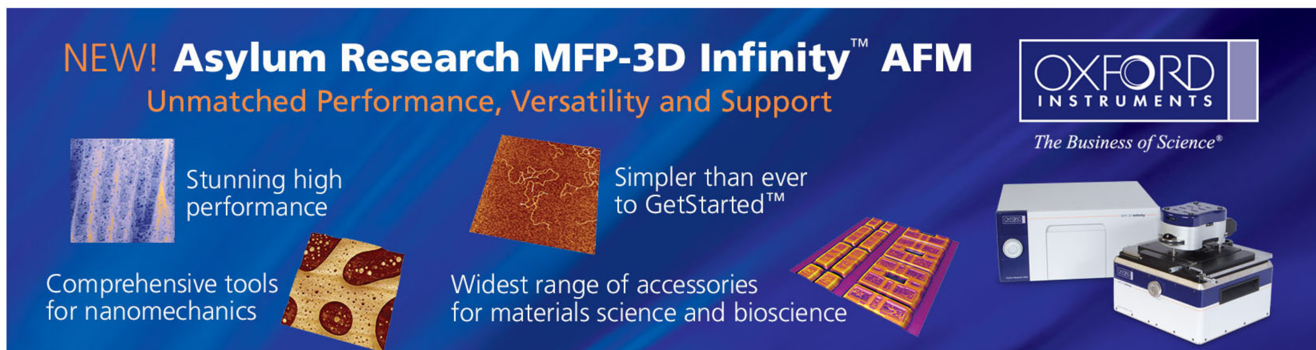

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Reliability characteristics of NiSi nanocrystals embedded in oxide and nitride layers for nonvolatile memory application

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The authors provided the reliability characteristics of nonvolatile nickel-silicide nanocrystal memories embedded in oxide and nitride layers for next-generation nonvolatile memory application. The charge trapping layer was deposited by sputtering a commixed target in the argon and oxygen/nitrogen ambiances, and then using a low temperature rapid thermal annealing to form nanocrystals. Transmission electron microscope clearly shows the sharpness and the density of nanocrystals. These proposed memory structures were compared for the charge storage ability, retention, and endurance. In addition, we used a simple simulation of electric field for nonvolatile nanocrystals memory to explain the advantages by using the high-k dielectric. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2905812]

Nonvolatile nanocrystal (NC) memories have been promising candidates to substitute for the conventional nonvolatile floating gate memory because the discrete traps served as the charge storage media have effectively improved the data retention for the scaling down process.[1,2] Among various NCs for the nonvolatile memory technology, the metallic NCs were extensively investigated over semiconductor NCs because of several benefits such as enhanced gate control ability (i.e., stronger coupling with the conduction channel), higher density of states, smaller energy disturbance, and larger work function.[3,4] However, the surrounding dielectric with NCs cannot be ignored because of its importance in terms of density of NCs, retention, and endurance. By the previous studies, the high-k materials can be used to increase the density of NCs due to the nucleated site effect and to achieve the better retention.[5–7]

In this letter, we presented the nonvolatile nickel-silicide (NiSi) NC memories embedded in oxide and nitride layers, respectively. These proposed memory structures were compared for the reliability test, and then, we also proposed a simple simulation of electric field to explain the advantages by using high-k dielectric surrounded with NCs.

These nonvolatile NC memories were fabricated on a 4 in. p-type silicon (100) wafer, with which the resistivity was about 20 Ω cm. After a standard RCA process, which removed native oxide and microparticles, a 3-nm-thick tunnel oxide was grown by using a dry oxidation process in an atmospheric pressure chemical vapor deposition. Afterward, a 10-nm-thick oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer was deposited by sputtering of $Ni_{0.3}Si_{0.7}$ commixed target in Ar [24 SCCM (SCCM denotes cubiccentimeter per minute at STP)] and O_2 (2 SCCM) environments at room temperature. The dc sputtering power and pressure were set to 80 W and 7.6 mtorr. Next, the rapid thermal annealing (RTA) process was performed in N_2 ambient and the annealing conditions were settled at 600 °C for 100 s. In addition, we changed the charge trapping layer from the oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer to the nitrogen (10 SCCM) incorporated $Ni_{0.3}Si_{0.7}$ layer, and the formation flow was used with the same recipes including the deposition and annealing conditions. Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition for the above-mentioned devices. Al electrodes on the back and front sides of the sample were finally deposited and patterned. Moreover, the electrical characteristics including the capacitance-voltage (C-V) hysteresis and reliability test were performed, in which they were measured by Keithley 4200 and HP4284 Precision *LCR* meter.

Figure 1 shows the cross-sectional transmission electron microscopy (TEM) image relative to the C-V characteristics of NiSi NCs embedded in the oxide [Figs. 1(a) and 1(c)] and nitride [Figs. 1(b) and 1(d)] layers. In the comparison of TEM, it is found that the shape and density of NCs in Fig. 1(b) are superior to that of Fig. 1(a) because the incomplete silicon nitride (SiN_x) layer could keep the thermal energy to enhance the self-assembled ability of NCs, and the dangling bonds of nitride also increased the nucleated sites to obtain high density of NC during the RTA process.[7] Hence, the memory window of NiSi NCs embedded in the nitride layer (4.5 V) was larger than NiSi NCs embedded in the oxide layer (2.0 V) under ±10 V gate voltage operation.

To further investigate the reliability of NiSi NCs embedded in oxide and nitride layers, the retention tests are shown in Fig. 2. We used the same programing (+10 V for 5 s) and erasing (−10 V for 5 s) conditions to treat these nonvolatile memories. The shift of flatband voltage (V_{FB}) as a function of time is obtained by comparing the C-V curves of charging state and quasistate. According to the previous research, the memory window has the saturation phenomenon under the state of fixed charging voltage with long charging duration and all of the trapped states (including shallow and deep states) are filled with storage carriers.[8] Moreover, if the charges are trapped in the same stored sites, the escaping probability of storage charges will be increased by the Coulomb blockade effect under the retention test. In our work, Fig. 2(b) with NiSi NC embedded in nitride layer has better

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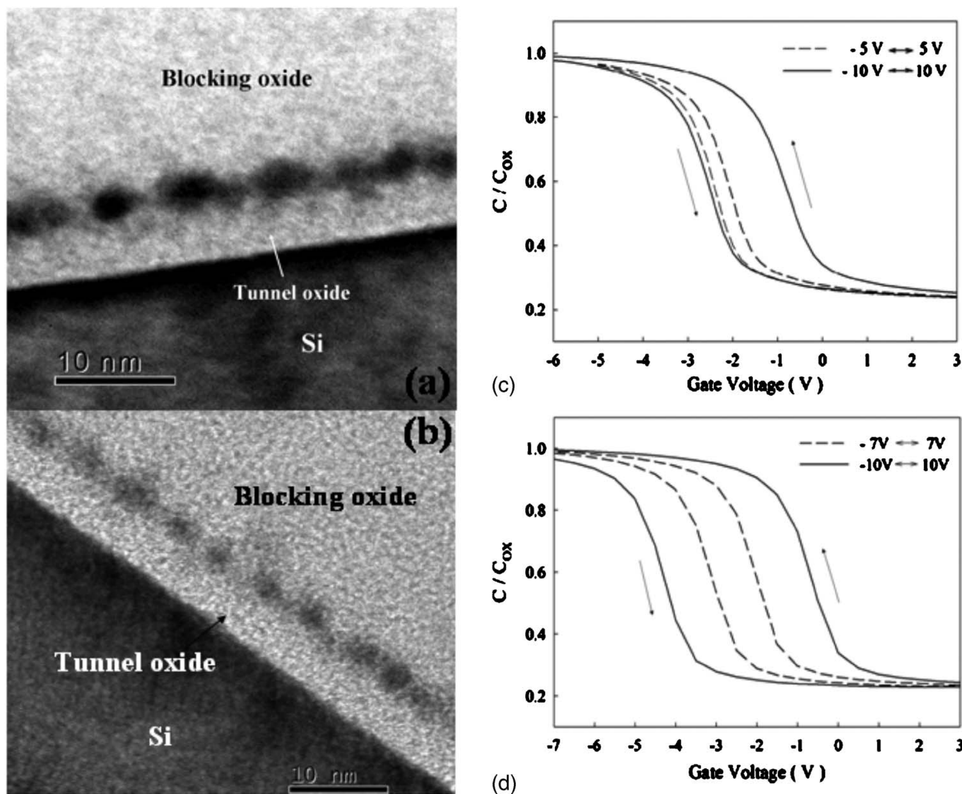

FIG. 1. Cross-sectional TEM analysis of (a) NiSi NCs embedded in oxide layer, and (b) NiSi NCs embedded in nitride layer. *C-V* hysteresis of memory structure with (c) NiSi NCs embedded in oxide layer and (d) NiSi NCs embedded in nitride layer. The memory windows of (c) 2.0 and (d) 4.5 V can be obtained under ± 10 gate voltage operation, respectively.

charge holding rate (66%) than that of Fig. 2(a) with NiSi NC embedded in oxide layer (50%) after 10 yr. This result consider that the charges are only stored in the NCs for the NiSi NC embedded in oxide layer structure, but the nitride had the trapping states to trap charges and dispersed the distribution of storage charge resulting in a lower Coulomb repulsive force in the charge trapping layer.

Figures 3(a) and 3(b) present the endurance characteristics of NiSi NC embedded in oxide and nitride under the pulse conditions of $V_G - V_{FB} = \pm 5$ V for 0.1 ms. From the data trend of Fig. 3(a), it is found that the variation of the memory window is serious after 10^6 P/E cycles. Nevertheless, the NiSi NC embedded in nitride reveals more stable memory window for the endurance test, as shown in Fig. 3(b). In order to clarify the influence of surrounding dielectric (oxide and nitride) and NCs on the behavior of the endurance process, we provided a simple simulation of electric field distribution for the NCs surrounded with the dielectric structures to explain the above-mentioned degradation phenomenon, as shown in Fig. 4. The simulation conditions of NC structures corresponded with the TEM image (as shown in Fig. 1) and the gate voltage was settled at the inversion state. Here, we used the ISE (Integrated Systems Engineering) TCAD software to build the NC structure and model. The simulation NC structure conditions of tunnel oxide thickness, metal NC diameter, blocking oxide thickness, and the distance between NCs and tunnel oxide/blocking oxide are set to 3, 5, 30, and 2 nm. In addition, the dielectric constants of SiO_2 and SiN were given to be 3.9 and 7.5, respectively.

Figure 4(a) shows the electric field distribution of metal NCs embedded in the oxide layer and the red line (black line) of the inset is a distribution of vertical electric field across a single NC (without any NCs). To compare the range of maximum electric field (E_{max}) between the substrate and NC, it is clearly found that the average E_{max} of the red line

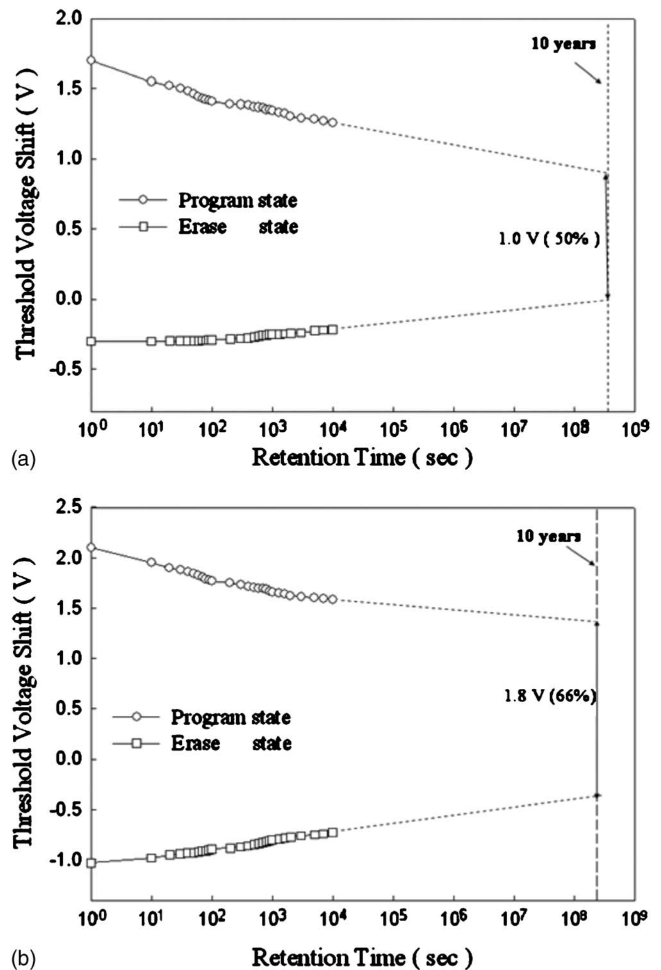

FIG. 2. Retention of the NC memory structure embedded in (a) oxide (charge holding rate: 50%) and (b) nitride layers (charge holding rate: 66%). The dotted line is the extrapolated value of retention data after 100 s, which this range is a steady state.

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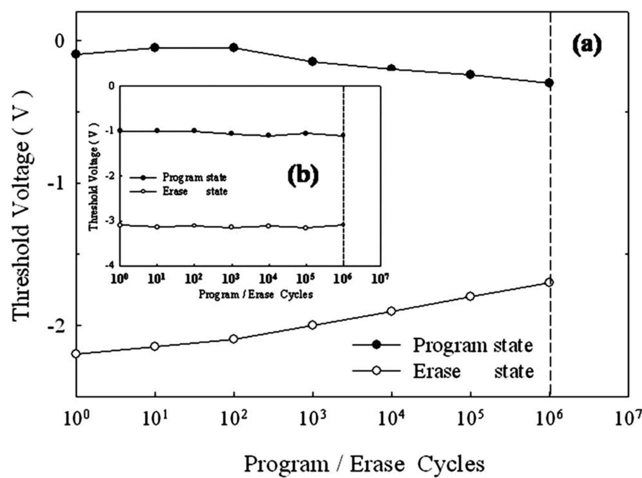

FIG. 3. Endurance characteristics of the NC memory structure embedded in (a) oxide and (b) nitride layers. Pulses condition of $V_G - V_{FB} = \pm 5$ V for 0.1 ms.

(9 MV/cm) are larger than the average E_{max} of the black line (6 MV/cm) for the distance of 3–5 nm from the substrate because of the stronger coupling effect of metal NCs than oxide. On the contrary, in Fig. 4(b), the diversity of average E_{max} of red (with NC) and black (without NCs) lines among the NC and Si substrate is less than that of NCs embedded in oxide. In other words, the distribution of electric field for metal NCs embedded in nitride layer was more uniform by the simulation analysis. Considering the influence of electric

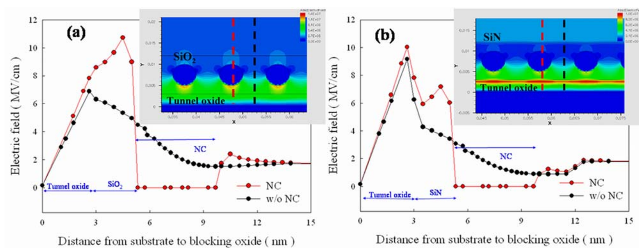

FIG. 4. (Color online) Simulation of electric field distribution of NiSi NCs embedded in (a) oxide and (b) nitride layers. The red line/black line of the inset is a distribution of vertical electric field across a single NC/without any NCs. The dielectric constants of SiO_2 and SiN were given to be 3.9 and 7.5, respectively.

field distribution for the metal NCs embedded in oxide layer structure, the charges have large tunneling probability in the tunnel oxide under the metal NCs, but the tunneling probability was almost the same in the tunnel oxide for the metal NCs embedded in nitride layer structure. Hence, the tunnel oxide below the NCs surrounded with the oxide layer would be seriously degraded under the P/E cycling operation because a large number of storage charges would cause the defects in the tunnel oxide during charge transportation process resulting in a memory window narrowing effect [as shown in Fig. 3(a)]. In addition, the nitride has trapping centers to store the charges and the NCs surrounded with the nitride layer have a uniform tunneling probability[9]. Therefore, the degradation result would be alleviated due to the distributed charge injection mode.

Nonvolatile NiSi NCs embedded in oxide and nitride layer memories using the low thermal budget were fabricated. These memory structures also exhibited enough memory windows to define the data information. However, nonvolatile NiSi NCs embedded in nitride layer memory have better reliability than nonvolatile NiSi NCs embedded in oxide memory. Moreover, the simulation of electric field distribution was enough to explain the divergence in the endurance test.

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