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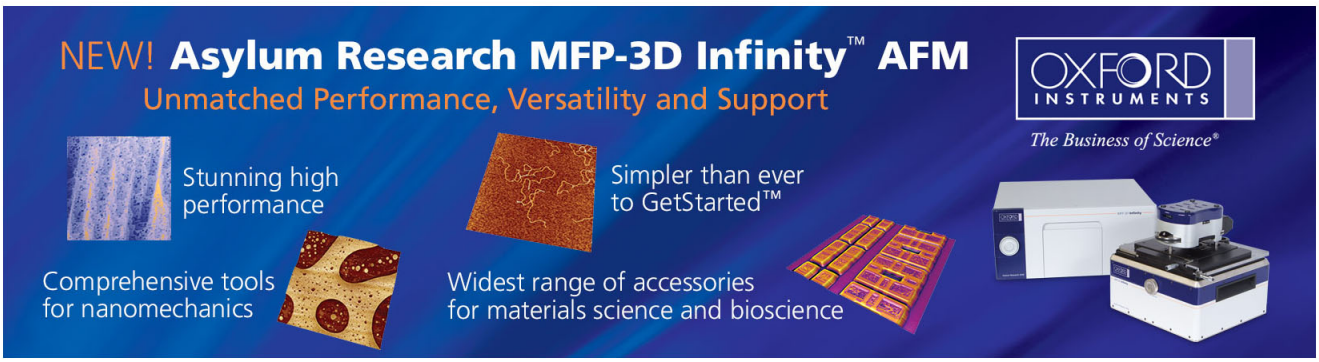

Formation of cobalt-silicide nanocrystals in Ge-doped dielectric layer for the application on nonvolatile memory

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In this work, Ge-doped cobalt-silicon thin film was synthesized using a cosputter system (Co and $Si_{0.5}Ge_{0.5}$). The deposited film was annealed in oxygen ambient at 650 °C to form cobalt-silicide nanocrystals. The formation of isolated silicide nanocrystals was confirmed by transmission electron microscopy and x-ray photoelectron spectroscopy analysis. In metal-oxide-insulator-oxide-silicon structure, a significant electrical hysteresis is observed and attributed by the presence of the cobalt-silicide nanocrystals and the oxidized Ge elements. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2908916]

Recently, floating-gate (FG) structure devices are the mainstream technology for the nonvolatile memory. It was invented by Kahng and Sze at Bell Labs in 1967.[1] However, the conventional FG devices have some drawbacks for the demand of scaling down devices hereafter.[2] With scaling down, tunneling oxide thinning will bring the storage to easily lose charge as there is leakage path existing in the tunneling oxide. The structure with distributed storage elements is considered the solution for this issue. Therefore, Tiwari *et al.* presented using Si nanocrystals (NCs) instead of conventional FG continuous storage layer.[3] To date, several methods and materials have been widely studied on the formation of NCs for the nonvolatile memory application.[4–6] Among several kinds of NC devices, the metal and metal silicide NCs are considered to be beneficial in its variable work function, higher density of states around the Fermi level.[7–9] In addition, the dielectric layer that NCs embedded in can also contribute the charge storage sites by defects or traps created in the interfaces between different materials.[10,11] In this letter, the formation of cobalt-silicide NCs was investigated by adding Ge elements into the cobalt-silicide film using cosputtered Co and $Si_{0.5}Ge_{0.5}$ targets on tunnel oxide. After thermal oxidation process, the cobalt-silicide NCs are formed and the additional Ge elements are oxidized. Furthermore, the oxidized Ge elements contribute extra charge trap sites.

Figure 1 exhibits the process flow in this work. First, a 5-nm-thick thermal oxide was grown as the tunneling oxide on *p*-type Si substrate by dry oxidation in atmospheric pressure chemical vapor deposition furnace. Subsequently, a 10-nm-thick Ge-doped cobalt-silicon thin film was deposited by sputtering the Co and $Si_{0.5}Ge_{0.5}$ targets simultaneously. The dc sputter power of cobalt and $Si_{0.5}Ge_{0.5}$ are 50 and 75 W, respectively. The process pressure was set at 7.6 mTorr, which yielded the deposition rate of 0.03 nm/s. Then a 20-nm-thick capped oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) before rapid thermal oxidation (RTO) process. After RTO at 650 °C for 30 s, the cobalt-silicide NCs nucleated in the dielectric layer. Afterwards, a 30-nm-thick blocking oxide (SiO_2) was capped by PECVD system. Finally, Al gate electrode was patterned and annealed. In addition, the electrical characteristics were performed in terms of capacitance-voltage (*C-V*) and current-voltage (*J-V*). Transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS) reveal the material composition and formation of NCs after thermal oxidation process.

Figure 2 shows (a) the cross-sectional and (b) the plane-view TEM image of the fabricated device sample. It can be found that the average diameter of cobalt-silicide NCs is around 8–10 nm from the cross-sectional TEM image and the area density of NCs is estimated to be about 1.03×10^{11} cm^{-2} from the plane-view TEM image. According the reported paper, the Ge elements tend to segregate at interface during the formation of the NCs.[12] With the segregation of Ge elements, the component of NCs is nearly cobalt silicide. Moreover, according to the thermodynamic analysis, the Si and Ge elements are prior to be oxidized in the mixed film.[13] Therefore, the cobalt-silicide NCs nucleate in the thin dielectric film mixed with silicon oxide and oxidized Ge elements.

Figure 3(a) shows the *C-V* hysteresis after bidirectional sweeps, which implies the electron charging and discharging

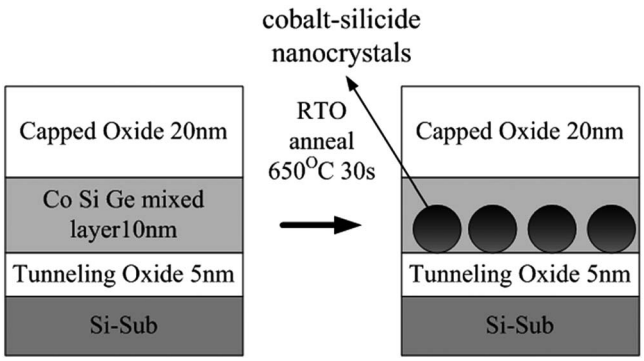

FIG. 1. The process flow proposed in this work.

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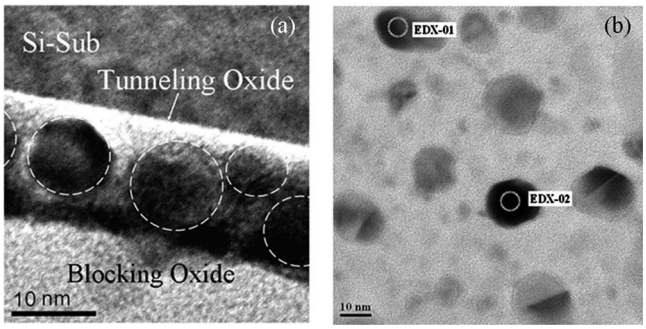


FIG. 2. The cross-sectional TEM micrographs of the MOIOS structure using thermal oxidized Ge-doped cobalt-silicon layer as trapping layer. The size of cobalt-silicide NCs are about 8–10 nm and the density of the nanocrystals is estimated to be about 1.03×10^{11} cm^{-2}.

effects of the metal-oxide-insulator-oxide-silicon (MOIOS) structure with cobalt-silicide NCs embedded in dielectric layer. The bidirectional *C-V* sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited a threshold voltage shift (ΔV_t), indicating carriers charging effect. In Fig. 3(a), it is found that the memory window of 5.5 V is observed under ±10 V gate voltage operation. As the swept voltage is increased to ±15 V, a more pronounced *C-V* shift is observed. The charge storage ability of Ge-doped cobalt-silicon memory devices is attributed to the presence of cobalt-silicide NCs and the oxidized Ge elements, which provide extra charge trap sites. Moreover, the

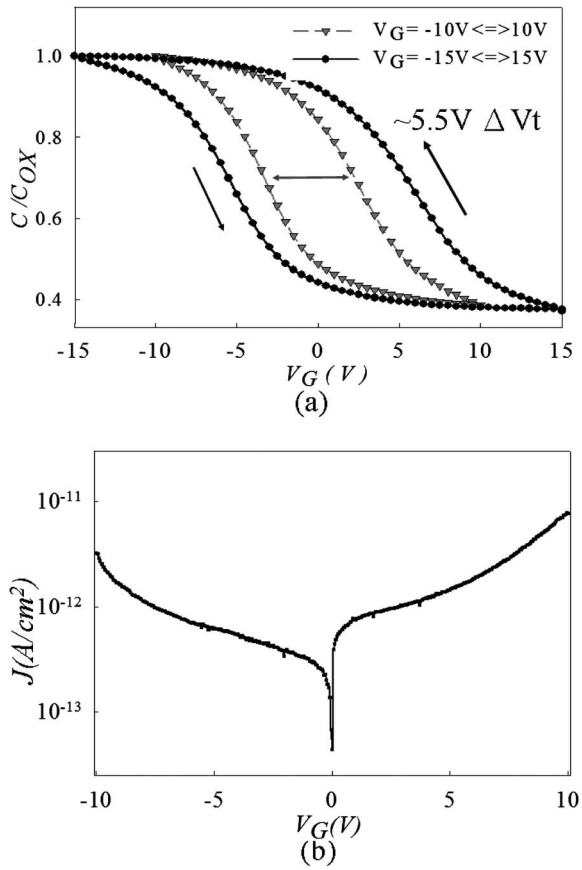
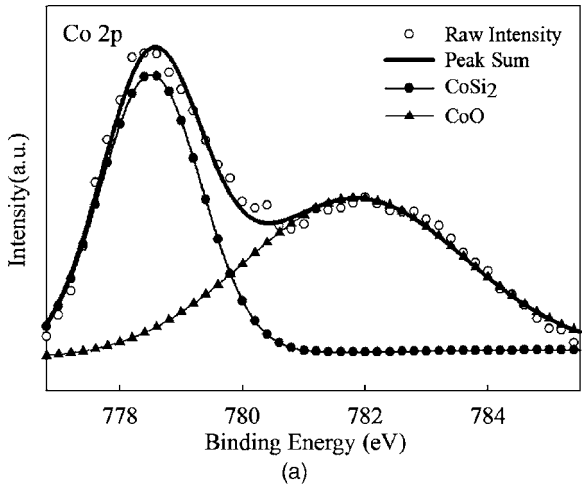


FIG. 3. (a) Memory effect obtained from *C-V* characterization of the MOIOS structure. The electrical *C-V* measurements are performed by bidirectional voltage sweeping (1) from 10 to−10 V and −10 to 10 V; (2) from 15 to−15 V and −15 to 15 V. (b)The current density measurement by voltage sweeping from (1) 0 to 10 V and (2) 0 to−10 V.



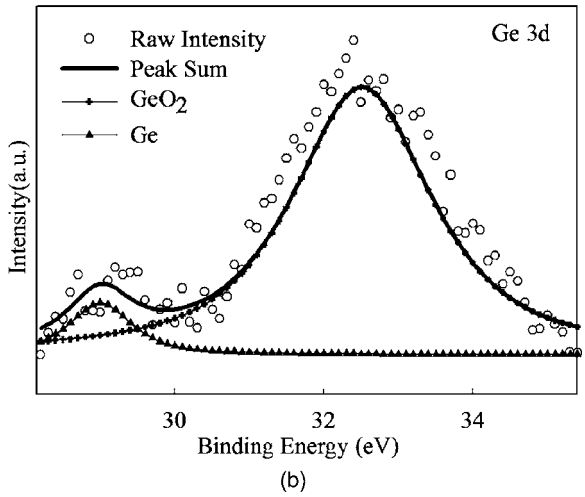


FIG. 4. (a) Co 2*p* XPS spectrum of the charge trapping layer after 650 °C thermal oxidation process. The main peak can be composed into two components which center at ~778.5 and ~782 eV corresponding to cobalt-silicide and cobalt oxide. (b) Ge 3*d* XPS spectrum of the charge trapping layer. The main peak at 32.5 eV can be assigned to the oxidation of Ge elements.

leakage current in the MOIOS structure is shown in Fig. 3(b). The lower leakage current could avoid the stored charge leaking into gate through the blocking oxide for the MOIOS structure. According to the reported paper, the asymmetry of *J-V* characteristics in the figure is because when the applied voltage is swept from 0 to+10 V, some negative charges are trapped in the defects of the dielectric layer, leading to an increase of the injection barrier height and, therefore, to a decrease of the oxide conductivity.[14]

Figure 4 demonstrates the results of XPS analysis for Ge-doped cobalt-silicon thin film after thermal oxidation process. In Fig. 4(a), it can be found that the Co 2*p* XPS spectrum shows two peaks corresponding to cobalt silicide and cobalt oxide at ~778.5 and ~782 eV, respectively.[15] The result indicates that cobalt-silicide NCs are formed and partly cobalt elements are oxidized to cobalt oxide during thermal oxidation process. Furthermore, the Ge 3*d* XPS spectrum is displayed in Fig. 4(b) which clearly indicates the peak at ~32.5 eV.[16] It is believed that the thermal oxidation process causes the formation of cobalt-silicide NCs and the oxidation of Ge elements.

In conclusion, we demonstrate the formation of the cobalt-silicide NCs by cosputtering Co and $Si_{0.5}Ge_{0.5}$ targets

simultaneously. A significant *C-V* hysteresis of 5.5 V is observed under ±10 V gate voltage operation for the MOIOS structure. The obvious memory window is attributed to both the cobalt-silicide NCs and the trap-rich oxidized Ge elements. In addition, this formation method of cobalt-silicide NCs with distributed storage elements is easy and compatible with the current manufacturing technology of semiconductor industry.

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