高性能混合訊號積體電路與系統之設計與研製(三)
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The Design and Applications of Low-Voltage CMOS RF Transceiver Chips

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Abstract — This project describes and designs three building block for radio frequency transceiver front-end integrated circuits. (1) A 3V 1.9GHz CMOS low-distortion direct-conversion quadrature modulator with a RF amplifier is described[1]. The circuit is implemented using 0.5 m DPDM CMOS technology and dissipates only 95mW (include power dissipation of RF amplifier) under 3V power supply voltage. The unwnated lower sideband is below –80dBc when the 0dB normalized desired upper sideband is set at 1.9GHz, corresponding to a small signal path mismatch. Moreover, the LO feedthrough and the second-order intermodulation are less than –80dB. The third-order intermodulation of –60dB is obtained. A current reuse technique is employed to save the power dissipation of RF amplifier that the current in the negative resistor is reused in the gain stage. The gain of RF amplifier is 23dB at 1.9GHz center frequency. The power dissipation of RF amplifier is only 9mW and smaller than resent publication.

(2) A 2.4GHz low-noise low-power single-to-differential bandpass amplifier is implemented in 0.5μm CMOS process. In this bandpass amplifier, the compact tunable positive-feedback circuit is connected to the integrated spiral inductor to enhance its Q value. The simple diode varactor circuit is adopted for center frequency tuning[2]. Two parallel spiral inductors are used to reduce the effective inductance and raise the center frequency. HSPICE simulation has been performed to verify the performance of the designed bandpass amplifier. It has been shown that the amplifier has a gain of 15dB at Q=45 under 2V power supply with 39mW power dissipation. The noise figure is 4.36dB in the passband. The tunable frequency range is between 2.369GHz and 2.422GHz. The gain difference and phase difference between the two differential output nodes are 0.0011905dB and 179.932° respectively, at 2.4GHz.

(3) A new CMOS fully differential bandpass amplifier (BPA) based on the structure of transresistance (Rm) amplifier and capacitor is proposed and analyzed. In this design, the Rm amplifier is realized by a simple inverter with tunable shunt-shunt feedback MOS resistor and tunable negative resistance realized by the cross-coupled MOS transistors in parallel with a current source. The capacitor is in series with the input of Rm amplifier, which realize the filter function and block the dc voltage. Under a 2-V supply voltage, the post-tuning capability of the gain can be as high as 90 dB whereas the tunable frequency range is between 41MHz and 178MHz. The power consumption is 11 mw and the dynamic range (DR) is 50 dB. The differential-mode gain is 20 dB and the common-mode gain is –25 dB so that the CMRR is 45 dB. Simple structure, good frequency response, and low power dissipation make the proposed bandpass amplifier quite feasible in the applications of IF stage for RF receivers.

中文摘要

本計畫描述並設計三個射頻前端積體電路的基本方塊，(1)本計劃首先設計一個 1.9GHz 行動通訊系統中之 IQ 調變器（IQ Modulator）和一內建射頻放大器(RF Amplifier)，採用標準的 0.5 微米雙層 poly 雙層金屬金氧半場效電晶體技術(0.5um DPTM CMOS technology），IQ 調變器採用組

合器的架構，功率消耗為 90mW，當 upper sideband 輸出為 1.9GHz 且正規化至 0dBm 時，lower sideband 為-80dB，相當於訊號的 mismatch 相當的小，第三互調訊號小於 -60dB，其他不想要的訊號都小於-80dB。在射頻放大器方面，我們將電流在電路架構中重複的使用，亦即負電阻的偏壓電流和轉導放大器的偏壓電流是相同的，功率消耗因此降低了。射頻放大器的電壓增益為 23dB，中心頻率為 1.9GHz，功率消耗比目前所發表的電路小很多，為 9mW。

（2）這是一個一個採用 0.5μm CMOS 製程來實現的 2.4GHz 單端轉雙端低雜訊低功率消耗的帶通濾波器，在此濾波器中包含了可調的正回授電路來增加 Q 值及可調電容來調整中心頻率，並使用兩個並聯螺旋電感提高中心頻率，而模擬部份則是以 HSPICE 來完成。由模擬結果可以看到: 在 2V 的電壓及 Q=45 情況下，增益為 15dB，功率消耗 39mW，雜音指數為 4.36dB，中心頻率調整範圍 2.369GHz ~ 2.422GHz 輸出兩端的增益及相位差分別為 0.0011905dB 及 179.932°。

（3）最後，提出一個完全由 CMOS 製程製作、電源工作電壓在 2V、操作在 80MHz 的新型帶通放大器，用以取代接收機前端的壓控放大器和離散式高 Q 值的 image 濾波器。此線路的頻率的控制範圍介於 41 至 178MHz，其增益的變化可高達 90dB，CMRR=45，功率消耗僅有 11mw，証明了用 CMOS 製程製作高頻接收機前端的可行性。

2. Introduction

In recent years, the rapid growth of mobile radio systems has led to an increasing demand of low-cost high-performance communication integrated circuits (ICs). The operational frequency bands of the modern mobile systems such as advance mobile phone service (AMPS) and Pan European Group special mobile (GSM) are 900 MHz, and 1.9 GHz for the personal communication networks (PNC) and digital European cordless telephone (DECT) [3]. To implement such a high frequency system, a multi-technology scheme which uses bipolar or BiCMOS ICs as the radio-frequency/intermediate-frequency (RF/IF) sections [3] and CMOS ICs as the baseband section [4] is often employed. This multi-technology scheme contains many ICs and discrete components. Thus the disadvantages of high cost and large size are inevitable. As to the consumers' demand for smaller-size lower-weight handheld equipment, a single technology scheme is preferred for the maximum integration level. To realize this scheme, low-cost high-integration all-CMOS implementation is one of the most attractive solutions.

Generally, an RF system can be divided into three functional blocks, namely, receiver, transmitter, and baseband processor. The receiver performs amplification, downconversion, and demodulation on the received signals. The transmitter performs modulation, upconversion, and transmission on the transmitted signals. The baseband processor performs both baseband signals processing and human-machine-interface processing. The key factor to obtain a high integration all-CMOS communication system is the availability of high performance receiver, transmitter, and baseband processor.

3. Results and Discussions

3.1 Quadrature Modulator and RF Amplifier

The HSPICE simulation of the proposed low-distortion direct-conversion quadrature modulator using 0.5 m DPDM CMOS technology is performed. Fig. 1 shows the circuit diagram of the quadrature modulator. Fig. 2 shows the circuit diagram of the RF amplifier. The over-all circuits are simulated under 3V batteries supply voltage. The amplitude of modulated signal is 400mV when 100mV baseband and 400mV LO are applied.

The frequency of baseband signal is 20MHz. The unwanted lower sideband and other spurious components include LO feedthrough, second-order intermodulation are less than –80dB when the desired upper

sideband is tuned at 1.9GHz. The third-order intermodulation are small than –60dB. The current drain including that in the RF amplifier is 31.7mA under 3V supply. The voltage gain of 23dB is achieved in the RF amplifier, whereas the quality factor is about 78.

The chip of the proposed circuit is now under fabrication. In the experimental chip, all of the function blocks including quadurture modulator, quadrature VCO, RF amplifier and output buffer are integrated on the same chip for test consideration.

3.2 Bandpass Amplifier

The HSPICE simulation on the designed bandpass amplifier is performed by using the transistor parameters of 0.5μm double-poly-double-metal CMOS technology. The supply voltage is 2V. Fig. 3 shows the overall circuit. The simulated results of the bandpass amplifier are summarized in Table I. It can be seen that S_{11} and S_{22} are below –10dB around the passband as required. The simulated noise figure of bandpass amplifier tuned at Q=45 is 4.36dB. The overall gain variations in the temperature range of 0 ~ 80 °C is 19dB. The third-order intercept points IP_3 is about 0dB.

A 2V 2.4GHz low-noise low-power single-to-differential bandpass amplifier has been proposed and analyzed. It is quite feasible to apply the designed bandpass amplifier in a RF CMOS receiver IC.

3.3 IF Bandpass Amplifier

Fig. 4 shows the basic circuit, the fully differential IF BPA can be realized by direcly cascading 3 stages of the biquadratic BPAs. Fig. 5 shows the HSPICE simulated frequency responses of the fully differential 6^{th}-order of Rm-C IF BPA with $V_{CP}=0.1V$, $V_{CN}=1.85V$, and $V_Q=0.1V$, and the supply voltage $V_{DD}=2V$. The differential-mode gain is 20 dB whereas the common-mode gain is –25 dB so that the CMRR is 45 dB. It has an out-of-band signal suppression comparable to the ideal 6^{th}-order BPF. When the IF BPA is applied to a dual-conversion RF receiver, the mirror signal suppression of 20dB can be obtained.

Thus the control voltage V_Q may be used to perform the automatic gain control (AGC). In the tuning of the IF BPA, the initial values of the controlled voltages are $V_{CP}=0.1V$, $V_{CN}=1.85V$, and $V_Q=0.75V$. After finding the optimal values, one of the controlled voltages can be kept constant while the other is adjusted to perform the fine tune. The simulated center frequency of the BPA varies from 41 MHz to 178 MHz whereas there is no gain variation in the passband. Under the condition of $V_{CP}=0.1V$, $V_{CN}=1.79\sim 2V$, and $V_Q=0.1\sim 1.2V$, the tunability of the center frequency is 137 MHz.

4. 計畫成果自評

在計畫執行期間，共完成了 1.9GHz 直接轉換正交調變器和內建射頻放大器、2.4GHz 低雜迅帶通慮波器、及 80MHz 中頻低雜訊帶通放大器。在 1.9GHz 直接轉換正交調變器和內建射頻放大器，非但架構創新，且其性能皆優於傳統的方法。最大的遺撼就是還沒將四相位電壓控制振盪器整合於單一晶片上，未來改進的方法為將測試電路與鎖相回路做在同一晶片上，用以降低寄生負載，增加準確性。此電路已發表論文並刊於 1999 ICECS conference。在低雜訊放大器方面，由於加上了正回授電路及可調電容，使得晶片在製作完成以後，仍可做增益及中心頻率的調整，而不受限於製程的變化產生性能上的改變，由結果看出，此放大器在 2.4GHz 的操作頻率下，性能可符合要求。此電路已發表論文並刊載於 1999 ICECS。在中頻 80MHz 帶通放大器方面，許多方面多加以修改，以得到更好的特性。最重要的為此線路的頻率控制範圍為 41 至 178MHz，而其增益的變化高達 90dB，CMRR=45，功率消耗僅有 11mw。未來的研究方向為將其與其它線路整合在單一晶片上，完成整個收發機系統的設計。此電路已投搞於 2000 ISCAS conference。

Reference

[1] Shuo-Yuan Hsiao and Chung-Yu Wu, “A parallel structure for CMOS four-quadrant

analog multipliers and its application to 2GHz RF downconversion mixer," IEEE J. Solid-State Circuits, vol. 33, no. 6, pp. 859-869, June 1998.

[2] Chung-Yu Wu and Yu Cheng, "The Design of 2V 1GHz CMOS Low-Noise Bandpass Amplifier with Good Temperature Stability and Low Power Dissipation,"ICECS 98, vol 3, pp.153-156, Sep., 1998.

[3] P. H. Lu, C. Y. Wu, and M. K. Tsai, "Design techniques for VHF/UHF high Q tunable bandpass filters using simple CMOS inverter-based transresistance amplifiers," IEEE J. Solid-State Circuits, vol.31, pp.719-725, May 1996.

[4] A. Rofougaran et al., "A 1GHz CMOS RF front-end IC for a direct-conversion wireless receiver,"IEEE J. Solid-State Circuits, vol. 31, pp. 880-889, July 1996.

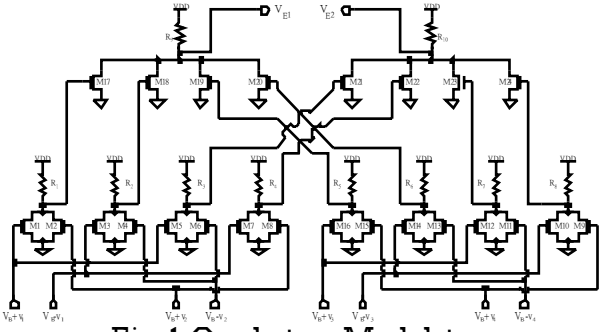


Fig. 1 Quadrature Modulator

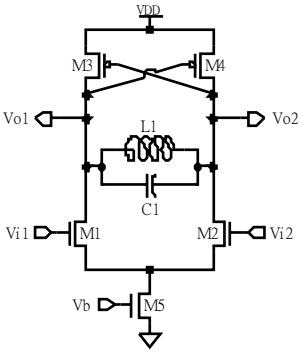


Fig. 2 RF Amplifier

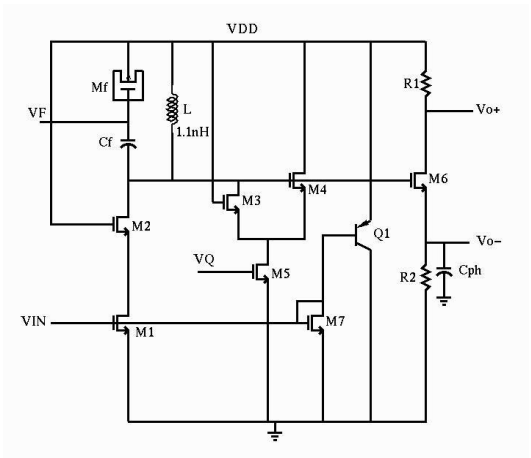
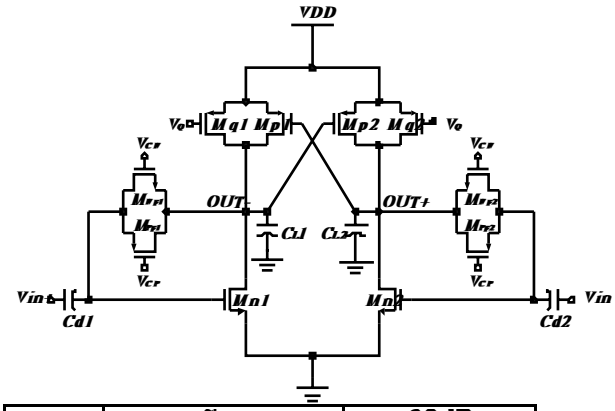


Fig. 3 The complete circuit diagram

PARAMETERS		VALUE
Q		45
SUPPLY VOLTAGE		2V
	Power Gain	15dB
	Center Frequency	2.4GHz
	Noise Figure	4.36dB
	IIP_3	0dB



	S_{11}	-30dB
	S_{22}	-34dB
	DC Power	39mw
	Gain Variation	19dB

TableI Simulation results of the bandpass amplifier

Fig. 4. The circuit diagram of Rm-C IF biquadratic BPA

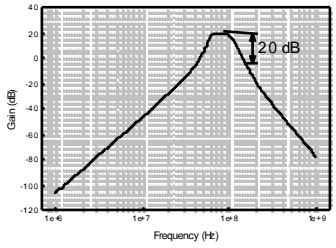


Fig. 5. The HSPICE simulated frequency response of the fully differential 6th-order Rm-C IF BPA when V_{DD}=2V, V_{CN}=1.75V, V_{CP}=0.1V, and V_Q=0.75V