Multimode G_m–C Channel Selection Filter for Mobile Applications in 1-V Supply Voltage

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***Abstract*—A CMOS transconductor for multimode channel selection filter is presented. The transconductor includes a voltage-to-current converter and a current multiplier. Voltage-to-current conversion employs linear region MOS transistors, and the conversion features high linearity over a wide input swing range. The current multiplier which operates in the weak inversion region provides a wide transconductance tuning range without degrading the linearity. A third-order Butterworth low-pass filter implemented with the transconductors was designed by TSMC 0.18-μm CMOS process. The measurement results show that the filter can operate with the cutoff frequency of 135 kHz to 2.2 MHz. The tuning range and the linearity performance would be suitable for the wireless specifications of GSM, Bluetooth, cdma2000, and wide-band CDMA. In the design, the maximum power consumption at the highest cutoff frequency is 2 mW under a 1-V supply voltage.**

***Index Terms*—Channel-selection filter, linear current multiplier, low voltage, mobile application, transconductor, wide tuning range.**

I. Introduction

RECENT trends to portable solutions is to include multiple applications in a high-integration system. Therefore, cost efficiency of VLSI implementations has been greatly enhanced with the emergence of multimode technology. This work presents a CMOS implementation of a channel selection filter for multimode mobile applications. The channel-selection filter is an important component for direct conversion receiver in wireless applications. Fig. 1 shows the structure of the direct conversion receiver [1]. The low-pass filter is used to select the required information under desired channel bandwidth. It acts between the variable gain amplifier and the baseband detection block. A large tuning range of the low-pass filter would be required for various wireless applications.

To meet different specifications for the desired channel in multimode technology, new basic analog building blocks should be re-designed. The transconductor, which performs the voltage-to-current conversion, is a basic building block in the G_m–C continuous-time filters [2]–[6]. For the multimode applications, the transconductor requires a wide tuning range of the transconductance while the linearity is well maintained.

In the paper, a high-performance linear transconductor is designed by the combination of a voltage-to-current converter and a current multiplier. The basic block diagram is shown in Fig. 2. Linear region MOS transistors are used to perform the voltage-to-current conversion and the third-order harmonic distortion term can be minimized by providing suitable bias conditions. The current multiplier makes use of weak inversion region MOS transistors to achieve high linearity. Then, the transconductor is used to design a third-order Butterworth low-pass G_m–C filter, where the filter order is suitable for the desired applications. In the paper, Section II develops the proposed high-linearity transconductor. The G_m–C filter which meets the specifications of GSM, Bluetooth, cdma2000, and wide-band CDMA is developed with the measurement results in Section III. Finally, conclusions are presented in Section IV.

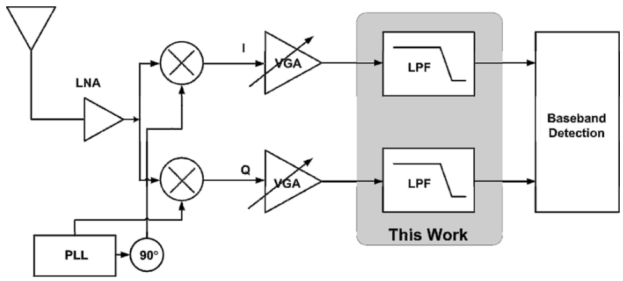

Fig. 1. Basic diagram of the direct-conversion receiver.

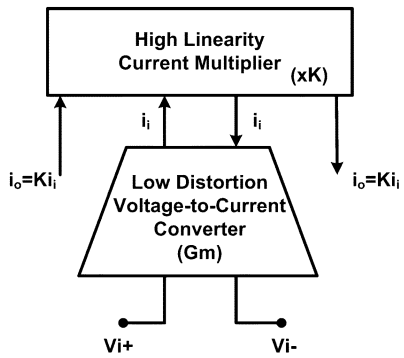

Fig. 2. Basic diagram of the transconductor.

II. Proposed Transconductor Circuit

A. Triode Region MOS Characteristic

The transconductor is designed with a differential input pair operating in the triode region. The drain current of a MOS transistor in the linear region can be expressed as

$$I_D = K_{\text{lin}}\left[(V_{\text{GS}} - V_{\text{th}})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{1}$$

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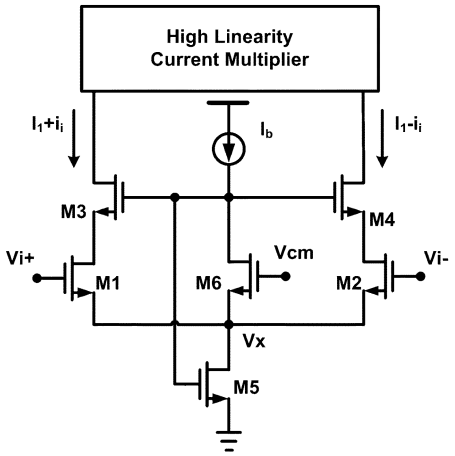

Fig. 3. Voltage-to-current cell.

where $K_{\rm lin}$ is the device parameter, $V_{\rm GS}$ is the gate-to-source voltage of the MOS transistor, V_{DS} is the drain-to-source voltage of the MOS transistor, and $V_{\rm th}$ is the threshold voltage. Thus, the output current would have a linear relationship with the applied input gate-to-source voltage under a constant drain-to-source voltage. The transconductance can be obtained by the derivative of the current-to-voltage characteristic and expressed as

$$G_m = \frac{\partial I_D}{\partial V_{\rm GS}} = K_{\rm lin} V_{DS} \tag{2}$$

The above equation is obtained by assuming that the V_{DS} would not change with the variation of $V_{\rm GS}$. However, efforts should be made to maintain the independence in realistic circuit implementation. Previous research [7] used the cascode structure to decrease the variation of drain voltage, but the circuit required BiCMOS technology and the voltage variation at the source terminal degraded the linearity. Regulated cascode structures have been used with the expense of increased complexity and power consumption [8]. Besides, the pseudodifferential structure was introduced with the need of the common-mode feedforward (CMFF) circuit [9] to solve the problem caused by input common-mode variation. Therefore, to design the transconductor based on the triode region input transistors, we need to keep the linearity without large power consumption, and the common-mode problem should be solved.

The transconductance is proportional to the V_{DS} from (2), so the transconductance tuning can be achieved. However, if a large tuning range is required, the MOS transistor operation would shift from the triode region to the saturation region owing to the increased V_{DS} and thus the linearity performance would be degraded.

B. Transconductor Implementation

Fig. 3 shows the proposed voltage-to-current circuit. The circuit is designed based on the flipped voltage follower (FVF) [10], which is composed by transistors M5 and M6. The main voltage-to-current conversion is provided by transistors M1 and M2. The gate voltage of transistor M5 is used to provide a bias voltage for transistors M3 and M4, and ensure the linear region operation of transistors M1 and M2. Thus, the drain voltage of transistors M1 and M2 would be kept to a constant value. In the circuit, the input transistors operate in the linear region, rather the saturation region proposed in [10]. Besides, the source of transistors M1 and M2 is fixed to a constant value owing to the FVF feedback loop. From analysis, it is shown that the low impedance can be obtained at the source of transistor M6. The structure suppresses the variation at the source of transistors M1 and M2, and thus the circuit would operate under a class-AB fashion.

To obtain the voltage-to-current characteristic of our proposed circuit, the input differential voltages at the gate of transistors M1 and M2 can be written as $V_{\rm i+} = V_{\rm cm} + (\mathrm{v_d}/2)$ and $V_{\rm i-} = V_{\rm cm} - (\mathrm{v_d}/2)$, where $V_{\rm cm}$ is the input common-mode voltage and v_d is the input differential-mode voltage. The currents which flow through transistors M1, M2, and M6 are expressed by

$$I_{D1} = K_1 \left[\left(V_{\rm cm} + \frac{v_d}{2} - V_{\rm th} - V_X \right) \times (V_{D1} - V_X) - \frac{1}{2}(V_{D1} - V_X)^2 \right] \tag{3}$$

$$I_{D2} = K_2 \left[\left(V_{\rm cm} - \frac{v_d}{2} - V_{\rm th} - V_X \right) \times (V_{D2} - V_X) - \frac{1}{2}(V_{D2} - V_X)^2 \right] \tag{4}$$

$$I_b = \frac{1}{2}[K_6(V_{\rm cm} - V_X - V_{\rm th})^2] \tag{5}$$

where V_{D1} and V_{D2} are the drain voltages of transistors M1 and M2, respectively, M_i and V_x is the source voltage of transistor M6. The aspect ratio of transistors M1, M2, and M6 are set to the same value. Note that $V_{D1} = V_{\rm GS5} - V_{\rm GS3}$ and $V_{D2} = V_{\rm GS5} - V_{\rm GS4}$. We assume that $V_{\rm GS5}$ would be very close to $V_{\rm GS6}$ since transistors M1 and M2 work in the linear region and a small drain current is produced. Moreover, a slightly larger aspect ratio of transistor M5 can be designed to support this assumption. $V_{\rm GS3}$ and $V_{\rm GS4}$ could be obtained by using the square law equation of saturated transistors. Thus, by inserting (5) in (3) and (4), the output currents I_{D1} and I_{D2} would be a function of input differential voltage. To analyze the linearity of the output current against the input voltage under the differential structure, a Taylor series expansion is used and then the relationship would be expressed by

$$i_{\rm out} = a_{1,\rm out} v_d + a_{2,\rm out} v_d^2 + a_{3,\rm out} v_d^3 + a_{4,\rm out} v_d^4 + \cdots \tag{6}$$

$$a_{1,\rm out} = G_m = \frac{1}{2} K \left(\alpha - \frac{\beta^2 - 3\beta\alpha + \alpha^2}{\sqrt{\alpha^2 + 2\beta\alpha - \beta^2}} \right) \tag{7}$$

$$a_{3,\rm out} = -\frac{3(\beta - 2\alpha)^3 \alpha}{2(\beta - \alpha)(\beta^2 - 2\alpha\beta - \alpha^2)^3} \tag{8}$$

where

$$K_1 = K_2 = K, \qquad \alpha = \sqrt{\frac{2I_b}{K_6}}; \quad \beta = V_{\rm cm} - V_{\rm th}$$

In (6), the output current can be seen to be a nonlinear function of the input differential voltage. Since the even-order harmonic terms could be cancelled out by the differential structure, the third-order harmonic distortion would become the dominant component. We can find that to minimize the third-order distortion term, the following equation should be satisfied:

$$\sqrt{\frac{2I_b}{K_6}} = \frac{V_{\rm cm} - V_{\rm th}}{2} \tag{9}$$

If the above condition is held, only the fifth or higher order distortion terms are left in (6) and these nonlinear terms have very low contribution to the proposed circuit. Moreover, to model the nonlinearity with respect to the gate source voltage of a MOSFET, the function of the squared $V_{\rm GS}$ in [11] is included. We can assume β_1 in [11] is small for large length of input transistors, where β_1 is process-dependent parameter. The calculation results show that we can multiply a factor of $(1+\beta_1)$ to (7) and a factor of $(1+\beta_1)^3$ to (8) through the approximation, and thus the condition in (9) hold as well.

For the proposed transconductor circuit, it does not require the CMFF circuit. This is because the input common-mode voltage is directly sensed at the gate terminal of transistor M6. If the input common-mode voltage is changed, the variation would appear at the source node of transistor M6, that is, the source nodes of transistors M1 and M2. Therefore, the common-mode current would not be changed since the gate and source voltage of transistors M1 and M2 vary in the same direction simultaneously, and thus the common-mode gain is minimized.

C. High-Linearity Current Multiplier

Low distortion voltage-to-current conversion is obtained under the defined bias conditions, and furthermore, the transconductance tuning ability could be added with the high-linearity current multiplier circuit, as illustrated in Fig. 4. The transistors would operate in the weak inversion region while proper sizing is required. For a MOSFET operating in the weak inversion region with V_{DS} larger than a few times of thermal voltage U_T, its current exhibits an exponential dependence of $V_{\rm GS}$ and can be expressed as

$$I_D = I_{D0}\frac{W}{L}\exp\left(\frac{V_{\rm GS}}{nU_T}\right) \tag{10}$$

where W and L are the width and the length of the transistor, respectively, I_{D0} is the reverse saturation current, n is the subthreshold slope factor, and U_T is the thermal voltage. From the above equation, we can find that

$$V_{\rm SG7} = nU_T \ln\left(\frac{I_{D7}}{I_{D0}}\frac{L_7}{W_7}\right) \tag{11}$$

$$V_{\rm SG8} = nU_T \ln\left(\frac{I_{D8}}{I_{D0}}\frac{L_8}{W_8}\right) \tag{12}$$

The device sizes of transistors M7 and M8 are set to the same. We can obtain from the linear voltage-to-current conversion circuit, $I_{D7} = I_1 + i_i$ and $I_{D8} = I_1 - i_i$. Therefore

$$\begin{aligned}\Delta V &= V_{\rm SG7} - V_{\rm SG8} \\ &= V_{\rm GS9} - V_{\rm GS10} \\ &= nU_T \ln\left(\frac{I_1 + i_i}{I_1 - i_i}\right)\end{aligned} \tag{13}$$

The subthreshold slope factor n is equal to $(C_{\rm ox} + C_{\rm depl})/C_{\rm ox}$ [12], where $C_{\rm ox}$ and $C_{\rm depl}$ are the gate and depletion capacitance per unit area, respectively. We can find that the factor $C_{\rm ox}$ is almost equal for nMOS and pMOS devices from the process device model. Besides, $C_{\rm depl}$ would be changed according to the size of MOSFET, and we can design specified ratio of nMOS and pMOS to obtain the same capacitance. The current output

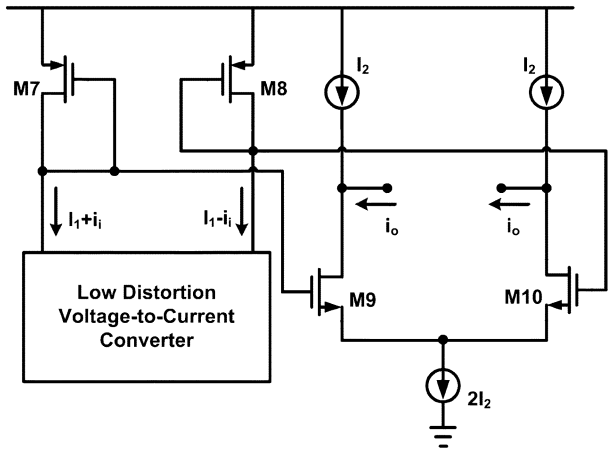

Fig. 4. High-linearity current multiplier.

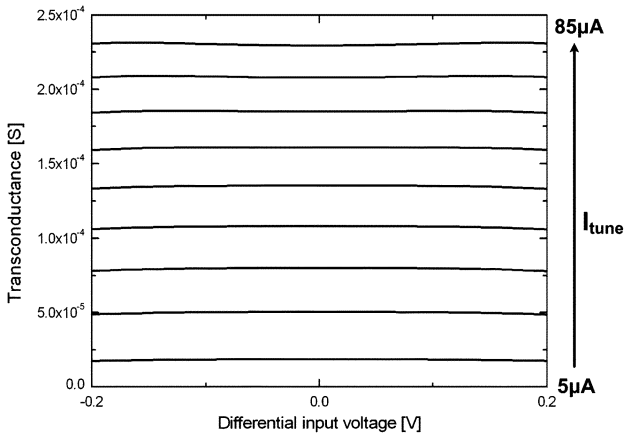

Fig. 5. Simulated G_m range of the proposed transconductor.

from the differential pair of transistors M9 and M10 can be expressed by

$$I_{D9} = \frac{2I_2}{1+e^{\frac{\Delta V}{nU_T}}} = \frac{2I_2}{1+\left(\frac{I_1+i_i}{I_1-i_i}\right)} = I_2 - \frac{I_2}{I_1}i_i \tag{14}$$

$$I_{D10} = \frac{2I_2}{1+e^{\frac{-\Delta V}{nU_T}}} = \frac{2I_2}{1+\left(\frac{I_1-i_i}{I_1+i_i}\right)} = I_2 + \frac{I_2}{I_1}i_i. \tag{15}$$

Finally, the output current $i_{\rm o}$ is given by

$$i_o = I_{D10} - I_2 = I_2 - I_{D9} = \frac{I_2}{I_1}i_i. \tag{16}$$

With the weak inversion characteristic, the input voltage should be logarithmically determined at first and through the exponential function, the output current would have a linear relationship. In other words, the output current is equal to a scaled version of the input current where the scaling factor is determined by the ratio of two bias currents. In our proposed circuit, the output current can be tuned by tuning the bias current I_2 at the output stage. The high-linearity characteristic can be also maintained when the circuit operates from the weak inversion region to the moderate inversion region, and thus the tuning range could be further extended. Fig. 5 shows the large signal simulation of the transconductance with respect to the function of applied differential input voltage. With the

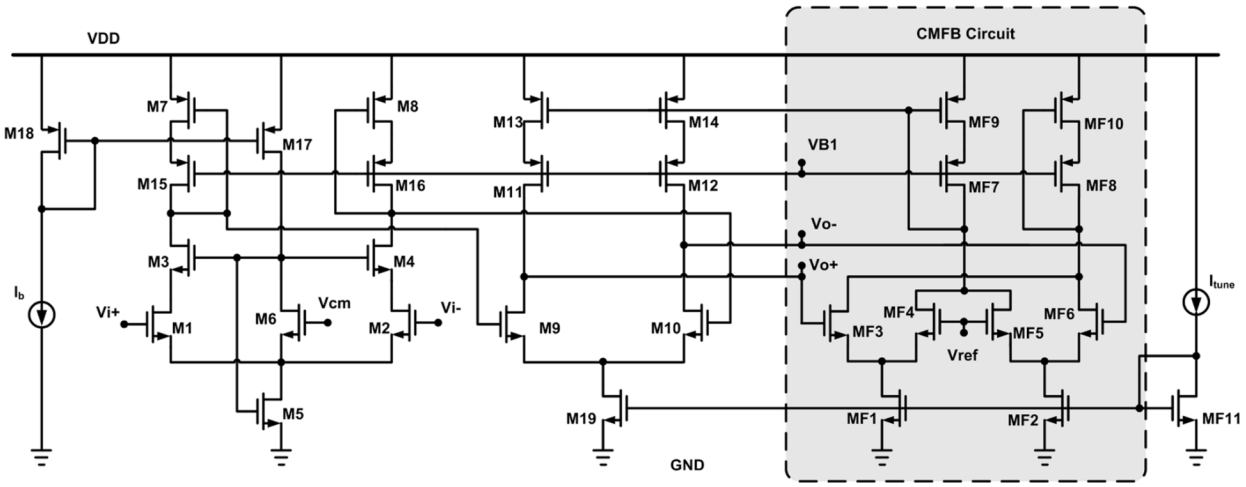

Fig. 6. The final implementation of the proposed transconductor with the CMFB circuit.

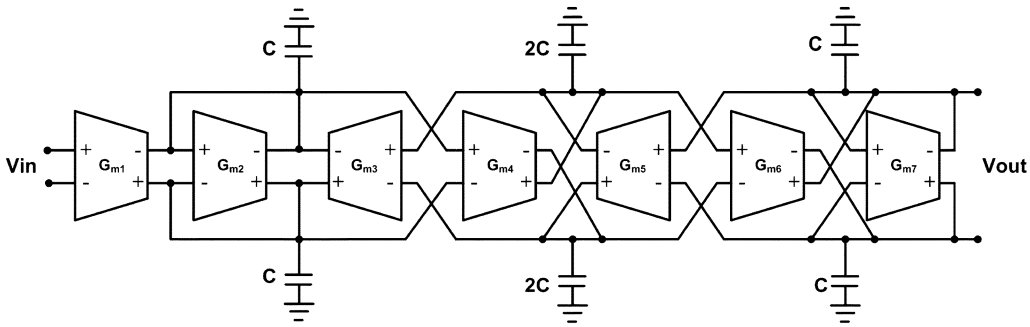

Fig. 7. G_m–C realiazation of the third-order Butterworth filter.

scalable tuning current, the tuning range of 10 to 230 μS can be obtained.

D. CMFB Circuit

As the transconductor is designed under the differential structure, a common-mode feedback (CMFB) circuit is required to control the output common-mode voltage. The final circuit implementation, which includes the CMFB circuit, is shown in Fig. 6. The cascaded transistors are used to enhance the gain of the transconductor since a sufficient gain performance would lead to accurate filter transfer function. $I_{\rm b}$ is an external source which feeds to the current mirror M17 and M18. For the CMFB circuit [13], the output voltage of the transconductor is sensed by transistor MF3 and MF6, and then compared with a reference voltage. The reference voltage is usually equal to the input common-mode voltage owing to the cascade design of the filter structure. If the output common-mode voltage is not equal to the reference voltage, a corrected current would be mirrored by transistor MF9 to the load of the transconductor, and then the output common-mode voltage is adjusted to the desired voltage. The aspect ratio of transistor M19 would be twice the value of transistors MF1 and MF2.

III. Filter Architecture and Measurement Results

From the demonstration of the passive ladder prototype, the third-order Butterworth low-pass G_m–C filter, which consists of seven identical transconductors, is chosen as shown in Fig. 7. G_{m1} is operated as a voltage- to-current converter to perform the current mode operation. The output nodes of G_{m2} and G_{m7} are connected to their input nodes, respectively, to perform as equivalent resistors. G_{m3} to G_{m6} operate as a gyrator to perform the equivalent inductor operation. In the G_m–C prototype, the cutoff frequency of the filter is proportional to G_m/C, where G_m is the transconductance and C is the loading capacitance. In the circuit implementation, transconductors G_{m2} to G_{m7} would be set to the same transconductance, and the input transconductor G_{m1} has twice transconductance than others. We should note that the filter does not need seven CMFB circuits for each transconductor. Actually, only three CMFB circuits are introduced because of the sharing of the same connection nodes. The filter stability can be simulated by applying a pulse current signal at output node to find the settling performance with the loading capacitor of 5 pF. The frequency tuning is achieved from a single source, $I_{\rm tune}$.

The transconductor and the filter were designed in the TSMC 0.18-μm deep n-well CMOS process. The device sizes of transistors M1, M2 and M6 are 8 μm/2 μm, the subthreshold transistors M7 and M8 are 80 μm/1 μm, and transistors M9 and M10 are 100 μm/1 μm. The output buffer is composed by the conventional source follower. The chip micrograph is shown in Fig. 8 with the active area less than 0.5 mm^2. The third-order inter-modulation (IM3) distortion measured with two sinusoidal tones of 400-m$V_{\rm pp}$ amplitude is obtained. The IM3 is shown to be less than $-$ 68.5 dB at the frequency of 2 MHz. Fig. 9 illustrates the filter frequency responses at 1-V supply voltage. We should note that the magnitude is normalized owing to the use of the output buffer. The cutoff frequency can be tuned from 135 kHz to 2.2 MHz, and the range covers the specifications of

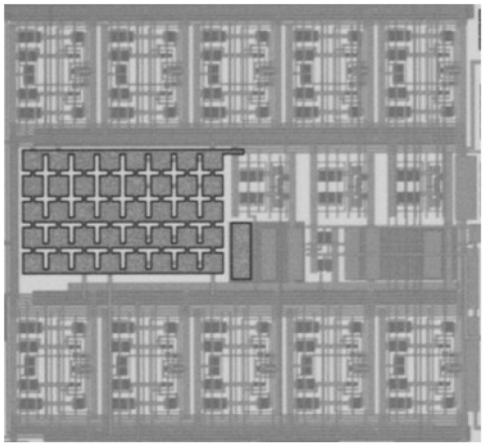

Fig. 8. Chip micrograph.

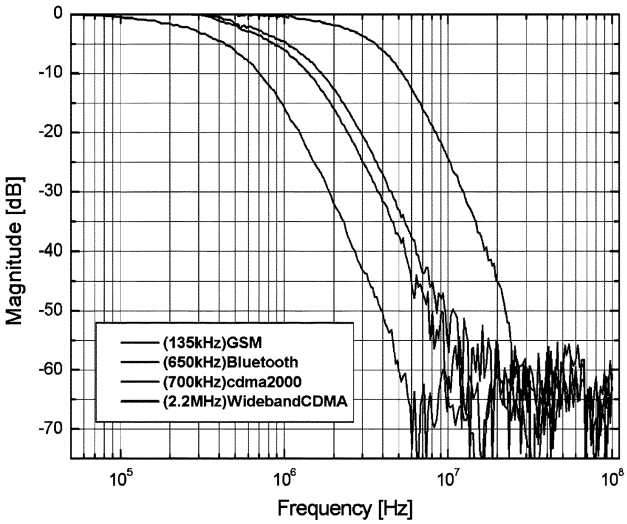

Fig. 9. Measured frequency responses of the proposed multimode filter.

GSM, Bluetooth, cdma2000, and wide-band CDMA. The linearity is maintained by holding the condition of (9), and the $V_{\rm cm}$ is set to 0.6 V. The IIP3 is measured by applying a signal with two sinusoid tones near the selected cutoff frequency. The linearity performance of 23.1 to 19.3 dBm for different specification is obtained. Owing to the weak inversion operation, the small power consumption of 1.57 to 1.92 mW at different cutoff frequency is measured for the proposed filter. The measured CMRR of 47 dB is obtained at 50 kHz. Table I summarizes the measurement results of this work and thus we can conclude a high-performance result of the circuit.

IV. Conclusion

A CMOS implementation of a third-order Butterworth low-pass G_m–C filter for multimode mobile applications is presented. A high-performance transconductor is designed while third-order harmonic term is minimized by applying suitable designing parameters. Through the use of the transconductor as a building block, the cutoff frequency of the channel selection filter can be tuned from 135 kHz to 2.2 MHz, which meets the specifications of several mobile applications. The theoretical analysis of the high-performance operation of the proposed circuit and a complete set of measurement results are provided to demonstrate the validity of the filter.

TABLE I
Performance Summary of This Work

Technology	0.18-μm CMOS	
Supply	1-V	
Active Area	<0.5 mm^2	
Tuning rang	135 kHz – 2.2 MHz	
IIP3	GSM	23.1 dBm
	Bluetooth	21.2 dBm
	cdma2000	21.0 dBm
	Wideband CDMA	19.3 dBm
Power consumption	GSM	1.57 mW
	Bluetooth	1.72 mW
	cdma2000	1.73 mW
	Wideband CDMA	1.92 mW
Output Noise density	65 nV/$\sqrt{}$Hz at 1 MHz	

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