Strained CMOS Devices With Shallow-Trench-Isolation Stress Buffer Layers

Yiming Li, *Member, IEEE*, Hung-Ming Chen, Shao-Ming Yu, Jiunn-Ren Hwang, and Fu-Liang Yang

***Abstract*—In this brief, shallow-trench-isolation (STI) stress buffer techniques, including sidewall stress buffer and channel surface buffer layers, are developed to reduce the impact of compressive STI stress on the mobility of advanced n-type MOS (NMOS) devices. Our investigation shows that a 7% driving current gain at an NMOS device has been achieved, whereas no degradation at a p-type MOS (PMOS) device was observed. The same junction leakage at both the NMOS and PMOS devices was maintained. A stress relaxation model with simulation is thus proposed to account for the enhanced transport characteristics.**

***Index Terms*—Channel surface buffer layer, fabrication, measurement, mobility, MOS devices, shallow-trench isolation (STI), sidewall stress buffer layer, simulation, transport characteristics.**

I. Introduction

MOBILITY enhancement techniques have become pervasive in advanced CMOS technologies. Devices incorporated with either uniaxial strain or biaxial strain approaches were widely studied and well modeled [1]–[4]. Among them, process-induced uniaxial strain approaches are recognized to be better than biaxial strain approaches since the uniaxial strain causes a larger band-structure modification and results in smaller carrier-effective mass and/or scattering rates. These uniaxial strain approaches include applying stressors from various regions, such as the shallow-trench isolation (STI), the embedded silicon–germanium (SiGe) source/drain (S/D), or the contact etch stop layer. In general, the impacts of these 3-D stress effects on performance of CMOS devices have different prefer channel directions and polarities (tensile or compressive) for n-type MOS (NMOS) and p-type MOS (PMOS) devices. Selective processes are often necessary to address the contradictory requirements of NMOS and PMOS stressors. For instance, compressive STI stress usually favors PMOS mobility, but not NMOS [5]. Thus, a selective modification of STI stress effect is important for advanced NMOS performance.

In this brief, we develop novel STI stress buffer layers to relax the mediation of an STI stress from an STI edge to the

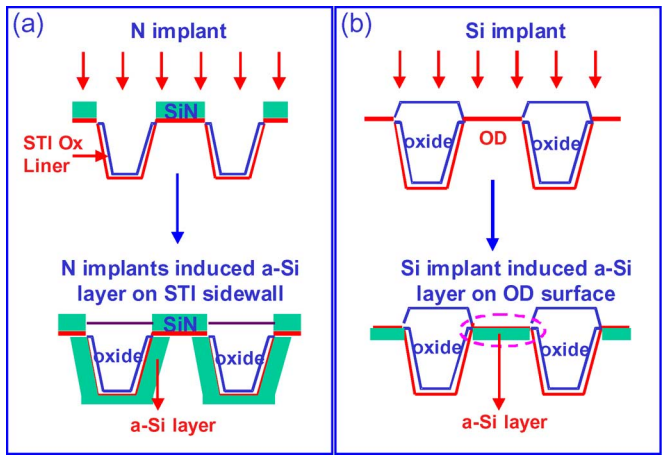

Fig. 1. Schematics of amorphous-silicon buffer layers for STI stress reduction. (a) STI sidewall buffer layer. (b) OD surface buffer layer.

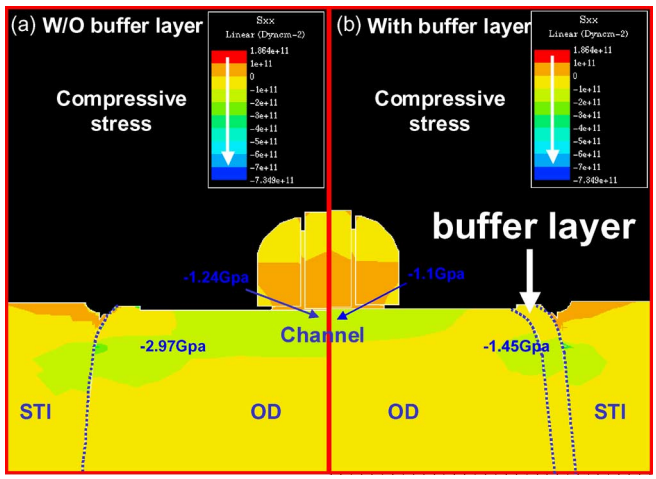

Fig. 2. Channel stress simulation with compressive STI stress. (a) Without STI stress buffer layer. (b) With STI sidewall stress buffer layer. We notice that the peak stresses in the two cases are −2.97 and −1.45 GPa.

Manuscript received July 17, 2007; revised November 28, 2007. This work was supported in part by the Taiwan National Science Council (NSC) under Contract NSC-96-2221-E-009-210 and Contract NSC-96-2752-E-009-003-PAE and in part by the Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C., under a 2006–2008 grant. The review of this brief was arranged by Editor H. S. Momose.

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Digital Object Identifier 10.1109/TED.2008.916708

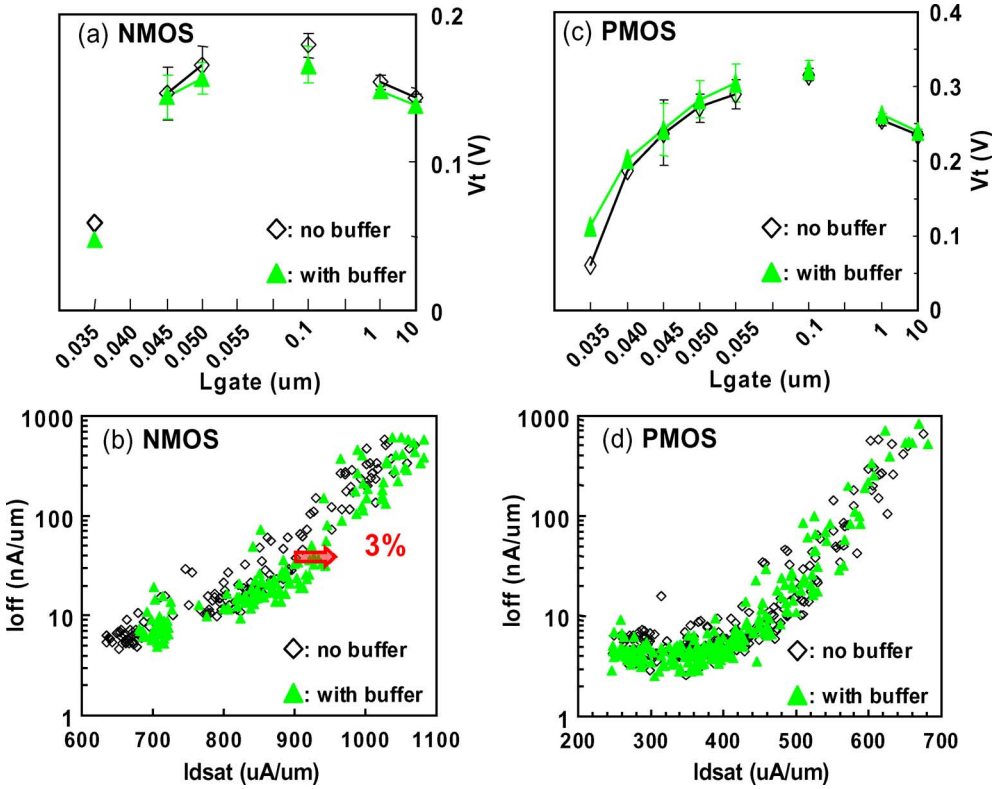


Fig. 3. V_t roll-off characteristics and performance enhancement with an STI sidewall buffer layer for the 1-μm-wide MOS devices. (a) NMOS V_t roll-off. (b) NMOS $I_{d\text{-sat}}$ with 3% enhancement. (c) PMOS V_t roll-off. (d) PMOS $I_{d\text{-sat}}$ without degradation.

channel region. Including sidewall stress buffer and channel surface, buffer layers are fabricated to suppress the effect of compressive STI stress on the mobility of advanced NMOS devices. Performance gain and junction leakage for both NMOS and PMOS devices are further reported. Our investigation shows that a 7% driving current gain at a 1-μm-wide NMOS device has been achieved, whereas no degradation at a PMOS device due to SiGe stress was observed. The same junction leakage at both the NMOS and PMOS devices was maintained. A stress relaxation model with simulation is thus proposed to account for the enhanced transport characteristics. We notice that this STI stress relaxation technique will benefit performance improvement of sub-45-nm CMOS technologies.

This brief is organized as follows. Section II introduces the device fabrication. Section III describes the results illustrating the dependence of the transport characteristics on the explored stress for different CMOS devices. Section IV draws conclusions.

II. Fabrication and Device Structure

The explored CMOS devices with the gate length down to 50 nm are manufactured with a regular STI process. In order to reduce the impact of STI compressive stress, experimental devices with two kinds of STI stress buffer layers, namely, 1) STI sidewall buffer layer and 2) outside diameter (OD) surface buffer layer, are tested and compared with the controlled devices. Fig. 1(a) shows the process steps of the STI sidewall buffer layer. Nitrogen ions are implanted into the sidewall of the STI trench and generate a layer of plastic amorphous silicon. After STI trench refilling and chemical–mechanical polishing, the wafer is then annealed to have this amorphous-silicon layer regrown. Since this amorphous buffer layer is plastic during the STI process, the mediation of STI compressive stress to the channel region is reduced [6], [7]. Simulations of STI stress transferred to the channel region are performed [8], [9] and compared, as shown in Fig. 2(a), without the STI sidewall stress buffer layer, and in Fig. 2(b), with the STI sidewall stress buffer layer. It is clearly shown that STI stress, which extends from STI to the channel region, as shown in Fig. 2(a), is not transferred to the channel region, as shown in Fig. 2(b). We notice that the peak stresses in the two cases are -2.97 and -1.45 GPa, respectively, as shown in Fig. 2.

Fig. 1(b) shows the process steps of the OD surface buffer layer. A standard STI process is deployed until the SiN hard mask is removed. Silicon ions are then implanted into the top surface of the OD region to create an amorphous-silicon layer. Similar to the STI sidewall stress buffer, this plastic OD layer is then annealed and regrown. Compressive STI stress is then relaxed in this top-surface channel layer.

III. Results and Discussion

Fig. 3(a) and (b) shows the threshold voltage (V_t) roll-off characteristics of NMOS devices and the performance enhancement of the ON- and OFF-state current (I_{ON}–I_{OFF}) with an STI sidewall buffer layer for the devices' channel length down to 50 nm, with a 1.05-V bias. In comparison with the control

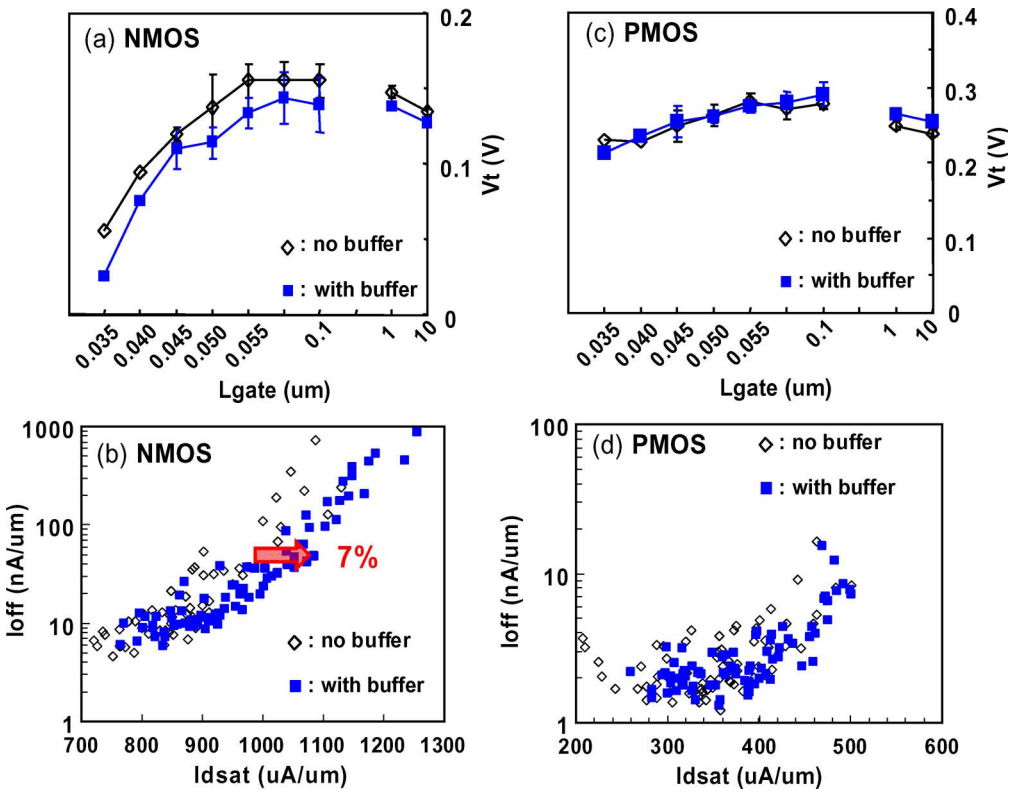
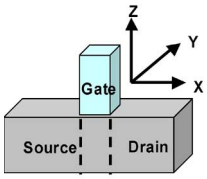


Fig. 4. V_t roll-off characteristics and performance enhancement with an OD surface buffer layer for the 1-μm-wide MOS devices. (a) NMOS V_t roll-off. (b) NMOS $I_{d\text{-sat}}$ with 7% enhancement. (c) PMOS V_t roll-off. (d) PMOS $I_{d\text{-sat}}$ without degradation.

TABLE I
SUMMARY OF THE IMPACT OF THE 3-D STRAIN EFFECTS ON CMOS PERFORMANCE



Decreased Compressive Stress	Drive Current Performance	
	NMOS	PMOS
X direction	Improve	Degrade
Y direction	Improve	Improve
Z direction	Degrade	Improve

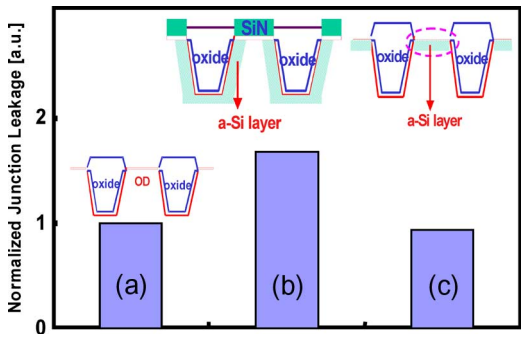


Fig. 5. Comparison of NMOS junction leakage. (a) No STI stress buffer layer. (b) STI sidewall buffer layer. (c) OD surface buffer layer.

devices, NMOS devices with the STI sidewall buffer layer have a similar V_t roll-off and create a 3% gain of saturated drain current ($I_{d\text{-sat}}$) driving current. Fig. 3(c) and (d) shows the V_t roll-off characteristics of an PMOS device and the performance enhancement of I_{ON}–I_{OFF} with an STI sidewall buffer layer. Compared with the control devices, PMOS devices with the STI sidewall buffer layer have a similar V_t roll-off and create no degradation on $I_{d\text{-sat}}$ driving current. Fig. 4(a) and (b) shows the V_t roll-off characteristics of an NMOS device and the performance enhancement of I_{ON}–I_{OFF} with an OD surface buffer layer. In comparison with the control devices, NMOS devices with the OD surface buffer layer have a similar V_t roll-off and create a 7% $I_{d\text{-sat}}$ driving current gain. Fig. 4(c) and (d) shows the V_t roll-off characteristics of an PMOS device and the performance enhancement of I_{ON}–I_{OFF} with an OD surface buffer layer. Compared with the control devices, PMOS devices with the OD surface buffer layer have a similar V_t roll-off and create no degradation on $I_{d\text{-sat}}$ driving current. The PMOS devices adopt the recess silicon process for SiGe on S/D, the SiGe on S/D can provide large compressive stress in the PMOS channel region, and the recess process will reduce buffer layer effect. Therefore, the approach using the stress buffer layer does not affect PMOS device performance. It is noticeable that the OD surface buffer layer, due to its higher efficiency on the relaxation of STI compressive stress along the surface channel, results in a better NMOS driving current gain than that of the STI sidewall buffer layer. Overall, these performance gains of the NMOS devices are consistent with the prediction of strain effects on the enhanced performance of NMOS devices with decreasing compressive stress along both the x- and y-directions, as summarized in Table I. For

the driving current of PMOS devices, the impacts of decreasing compressive stress along the x- and y-directions are cancelled by each other since their responses have reversed polarities.

The qualities of amorphous buffer layers after annealing are evaluated by their impacts on junction leakages. As shown in Fig. 5, the junction leakage of NMOS devices with the STI sidewall buffer layer is increased by $\sim$67% over the controlled devices without the STI stress buffer layer. On the other hand, NMOS devices with the OD surface buffer layer have no junction leakage degradation since this layer is not overlapped with the junction region.

IV. Conclusion

In this brief, we have experimentally achieved a 7% NMOS $I_{d\text{-sat}}$ driving current gain without junction leakage degradation by using an OD surface buffer layer to relax compressive STI stress. In addition, the performance of PMOS devices is not degraded. This technique can be used to reduce the impact of compressive STI process on advanced CMOS devices without additional masks. This STI stress relaxation technique will be useful for the performance improvement of sub-45-nm CMOS devices.

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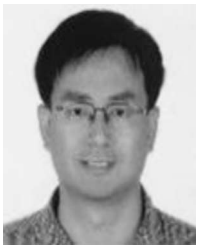

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