行政院國家科學委員會專題研究計畫成果報告

奈米金屬閘 MOS 元件製程技術之研發

Study of Nano Metal Gate MOS Device Technology Fabrication

計畫編號：NSC 90-2215-E-009-097

執行期限：90 年 8 月 1 日至 91 年 7 月 31 日

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一、中文摘要

第一部份我們開發利用選擇性液相沉積方式製作奈米閘極的技術，這個技術包含三個關鍵製程，包括(1)奈米側壁；(2)取代閘極；(3)選擇性液相沉積。首先，奈米尺寸側壁形成做為取代閘極，然後選擇性沉積二氧化矽薄膜於基板上而不沉積於取代閘極，最後移去取代閘極並且填入複晶矽。依靠這個方法，我們成功地製作出 100 奈米的複晶矽閘極。第二部份我們開發高介電常數介電質氧化鋁薄膜之沉積，研究其沉積速率，不同回火條件下的膜組成及其電特性。

關鍵詞：奈米閘極、側壁、選擇性液相沉積、氧化鋁。

Abstract

In the first part we developed a nanometer gate technology by use of selective liquid phase deposition. This technology combined three key processes including (1) nanometer spacer, (2) replacement gate, and (3) selective liquid phase deposition. Firstly, the nanometer dimension spacer was formed as the replacement gate. And then we selectively deposited silicon dioxide on substrate against the replacement gate. Finally, we removed the replacement gate and filled with polycrystalline silicon. By use of this method, we successfully fabricated nanometer polysilicon gate with gate length of 100 nm. In the second part we developed the deposition of high-K dielectric Al_2O_3 film. We investigate its deposition rate, film composition after different annealing conditions and electrical characteristics.

Keywords: Nanometer gate, spacer, replacement gate, selective liquid phase deposition, Al_2O_3.

二、緣由與目的

When CMOS device fabrication technology grows into ULSI generation, the device dimension must scales down to nanometer regime. To achieve the advanced technology, we must spend more on equipment and technology research. The most difficult technology of all is lithography due to its large cost and many unsolved problems. These problems come from the limitation of optical lithography including the light source, proximity effect, mask fabrication and etc. So how to develop a new process compatible with exiting materials and tools shows its importance.

Many new technologies have been developed to achieve nanometer device fabrication, such as phase shift mask [1], vertical transistor [2], replacement gate [3] and so on. These new technologies still have either the cost or the new structure development problem. In this paper, we try combining conventional CMOS technologies and LPD [4] to fabricate nanometer device. And we finally achieve the nanometer polysilicon gate with gate length of 100nm.

When gate oxide scales down to less than 30Å, the large leakage current caused by direct tunneling will generate too much power consumption. To lower the leakage

current, the replacement of high-K dielectric to SiO_2 is inevitable. This study also investigates the properties of high-K dielectric Al_2O_3 film and finds out the optimum deposition condition.

三、實驗

The nanometer polysilicon gate fabrication process flow is shown in Fig. 1. A 6 inches p-type silicon wafer was prepared. After LOCOS formation, SiO_2 was deposited on silicon wafer. Then G-line stepper was used to pattern the SiO_2 layer, and the minimum dimension 0.5 μm of SiO_2 strip was prepared. After oxide RIE and cleaning, Si_3N_4 was conformably deposited on the patterned SiO_2. Then anisotropic RIE was applied to etch the Si_3N_4 and form the nanometer size Si_3N_4 spacer on both side of SiO_2 strip (Fig. 1(a)). The Si_3N_4 spacer will be used as replacement gate. After the removal of SiO_2 strip, the liquid phase deposition (LPD) SiO_2 was selectively deposited on substrate against Si_3N_4 replacement gate (Fig. 1(b)). Then the Si_3N_4 replacement gate was removed by using hot H_3PO_4. Finally, the nanometer size strip-hole was filled with polycrystalline silicon by LPCVD to form the nanometer polysilicon gate (Fig. 1(c)).

The Al_2O_3 film was deposited on Si substrate by sputter. The deposition rate was measured by n&k analyzer. After different annealing conditions, the film composition was analyzed by electron spectroscopy for chemical analysis (ESCA) and X-ray diffraction (XRD). The I-V and C-V measurements of deposited Al_2O_3 film were performed through MOS capacitor.

四、結果與討論

1. 奈米閘極之製作

Figure 2 is the SEM cross-sectional view of Si_3N_4 spacer. Using well-controlled thin film deposition and anisotropic RIE technology, the Si_3N_4 film has been conformably deposited on SiO_2, and nanometer size spacer has also been formed after etching. The replacement gate formation can be affected by the shape and width of spacer. So the etching and the deposition recipe must be accurately controlled to make sure the straightness and nanometer dimension of spacer. Figure 3 shows the SEM pictures of Si_3N_4 replacement gate. After the removal of SiO_2, the replacement gate is found still standing without falling down. From both cross-sectional view (Fig. 3(a)) and top view (Fig. 3(b)), they show the successful formation of replacement gate and accurate size of nanometer dimension. After cleaning, the LPD SiO_2 is selectively deposited on substrate against the replacement gate. Because of the selective property of liquid phase deposition, the SiO_2 will be deposited on silicon substrate instead of Si_3N_4. This phenomenon has been also found in photoresist, lowK material, etc. The strip-hole can also be achieved by CMP planarization process. Because of the damage and the contamination in CMP process, LPD is the only choice to form strip-hole. Then the replacement gate is removed in hot H_3PO_4 solution, and the remained nanometer size strip-hole is filled with polysilicon. Figure 4 shows the SEM pictures of nanometer gate after polysilicon fill. The polysilicon deposition using LPCVD can conformably fill the nanometer size hole without void generation. From Fig. 4, we can see the successful fill of nanometer polysilicon gate with length of 100nm. We had finally achieved the nanometer gate formation by this technology without advance lithography. By using this technology, we can then fabricate nanometer generation CMOS device with existing materials and tools.

2. 高介電常數介電質之開發

The deposition rate of thin Al_2O_3 film is shown in Fig.5. Using n&k analyzer, linear deposition is observed. Figure 6 contains binding energy results and Al and O concentration ratio from ESCA analysis. From Fig. 6(a), the binding energy of Al2p and O1s are ranged from 74.5eV to 75.5eV and 532eV to 533eV, respectively. From Fig.

6(b), the atomic ratio of Al and O is ranged from 0.59 to 0.66. For stoichiometric Al_2O_3 thin film, the ratio between these two atoms should be 0.667. As a result, annealing at 900℃ in oxygen ambient would obtain the most stoichiometric films. However, such higher annealing temperature in oxygen ambient may result in thicker interfacial oxide layer and make device scaling more difficult. The XRD spectra in Fig. 7 are slightly different from other research groups. No obvious crystallization occurs during 1000℃ post-deposition annealing. However, the reason of crystallization peaks observed in 850℃ in nitrogen and 900℃ in oxygen isn't clear known. According to previous ESCA and XRD analysis, 900℃ in nitrogen ambient is chosen as the post-deposition annealing temperature for trade-off between stoichiometry and interfacial layer thickness. Fig. 8 compares leakage currents and capacitances of various deposition conditions temperature and fixed PDA in 900℃. It's clear except for the 100℃ deposition, others have almost the same leakage current and capacitance curves. For these three ones, the effective oxide thickness could be down to 35Å.

五、結論

In conclusion, we successfully fabricated the nanometer polysilicon gate. The nanometer gate was formed by the combination of nanometer spacer, replacement gate and selective liquid phase deposition. From the SEM pictures, we can see the nanometer polysilicon gate and its gate length is 100nm. By using this technology we can next fabricate the nanometer generation CMOS device without advance lithography and new structure.

Besides, we also investigate the high-K dielectric Al_2O_3 film. According to ESCA and XRD analysis, 900℃ in nitrogen ambient is chosen as the post-deposition annealing temperature for trade-off between stoichiometry and interfacial layer thickness and the effective oxide thickness could be down to 35Å.

六、計畫成果自評

本計畫原為三年期之整合型計畫，後經調整為一年期之個別型計畫，依原訂計畫第一年目標，本計畫完成了奈米複晶矽閘極及高介電常數介電質之開發，並已發表相關論文一篇。奈米元件之研究，為目前熱門之研究主題，未來預計依據本計畫研究成果，繼續從事相關主題研究，並發表論文及專利。

七、重要成果

1. EDMS Taiwan'01 Proceeding, December 12-13, 2001, p.423.
2. 2002-奈米科技學術研討會暨國科會成果發表會。

八、參考文獻

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[2] J. M. Hergenrother et al., "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET with Lithography-Independent Gate Length," *IEDM Tech. Dig.*, p.75, 1999.

[3] C. P. Chang et al., "SALVO Process for Sub-50 nm Low-VT Replacement Gate CMOS with KrF Lithography," *IEDM Tech. Dig.*, p.53, 2000.

[4] Ching-Fa Yeh, Chien-Hung Liu, Jwinn-Lein Su, "Novel contact hole fabrication using selective liquid-phase deposition instead of reactive ion etching," *IEEE Electron Device Letters*, vol.20, no.1, p.39, Jan. 1999.

[5] Ching-Fa Yeh, Chih-Wen Hsiao, and Wen-Hsin Chan, "Implementation of nanometer gate using selective liquid phase deposition technology," *EDMS Taiwan'01 Proceeding*, December 12-13, 2001, p.423.

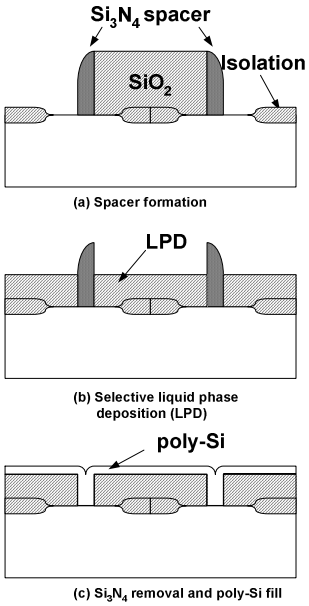


Fig. 1. Fabrication sequence of nanometer gate.

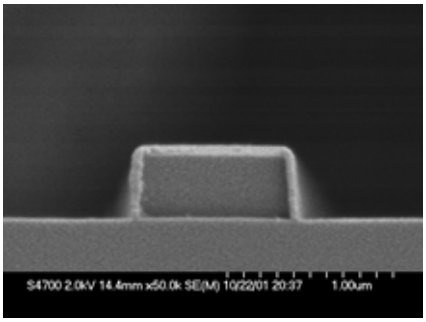
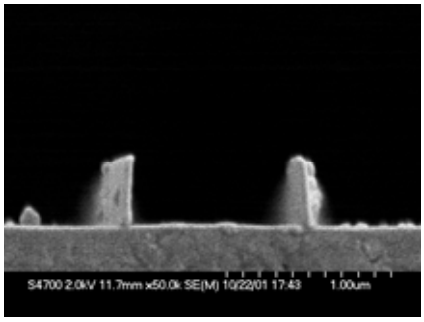
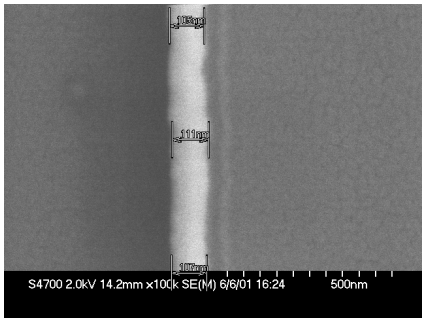


Fig. 2. SEM cross-sectional view of Si_3N_4 spacer.

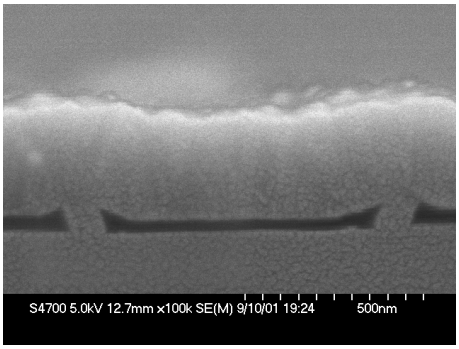


(a) Cross-sectional view

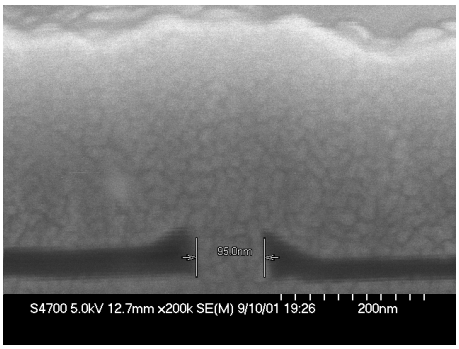


(b) Top view

Fig. 3. Replacement gate: (a) Cross-sectional View and (b) Top view.



(a) Cross-section view



(b) Cross-section view (zoom in)

Fig. 4. Cross-sectional views of poly-Si fill: (a) standard and (b) zoom in.

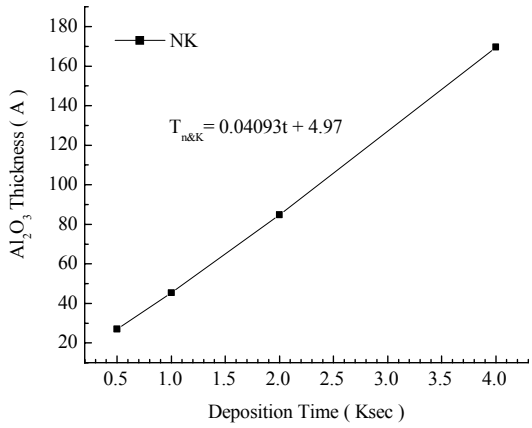
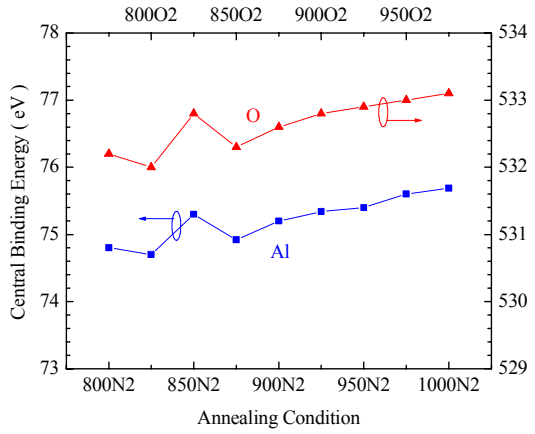
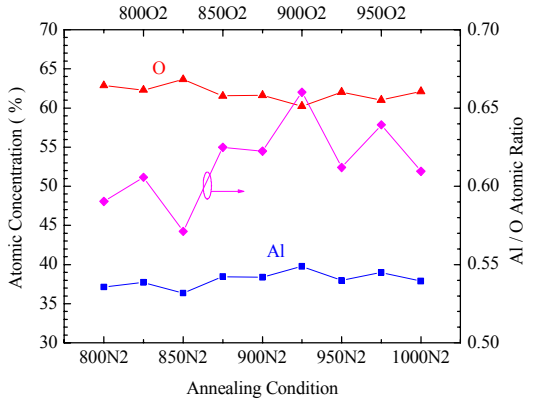


Fig. 5. Deposition rate of thin Al_2O_3 films.

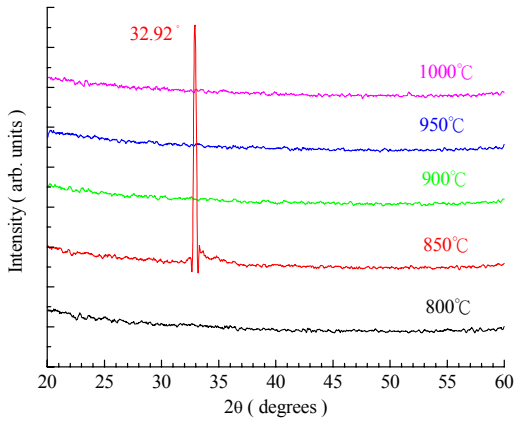


(a)

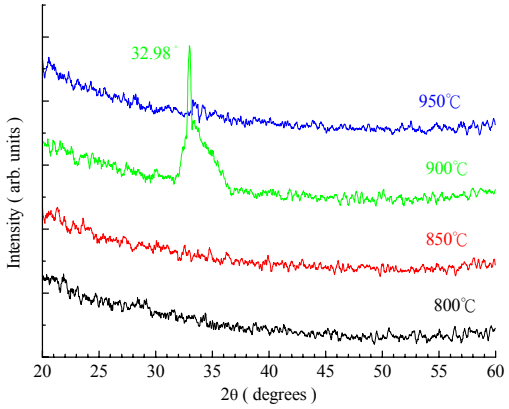


(b)

Fig. 6. (a) Binding energy of Al2p and O1s from ESCA analysis and (b) Al2p and O1s concentration ratio from ESCA analysis.

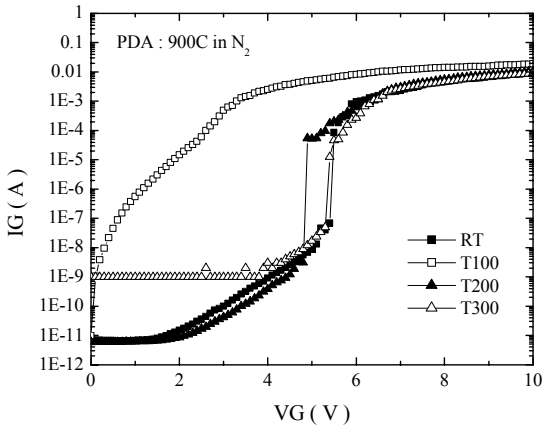


(a)

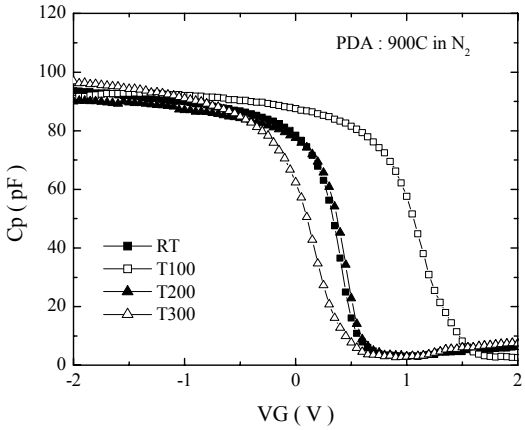


(b)

Fig. 7. XRD spectra of Al_2O_3 thin film annealing in (a) Nitrogen ambient and (b) Oxygen ambient.



(a)



(b)

Fig. 8. (a) I-V curves and (b) C-V curves of Al_2O_3 thin film deposition at various temperature.

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執行單位：交通大學電子工程研究所

中　華　民　國　91 年　10 月　31 日