RF and Logic Performance Improvement of $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ Composite-Channel HEMT Using Gate-Sinking Technology

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***Abstract*—Eighty-nanometer-gate $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite-channel high-electron mobility transistors (HEMTs), which are fabricated using platinum buried gate as the Schottky contact metal, were evaluated for RF and logic application. After gate sinking at 250 °C for 3 min, the device exhibited a high g_m value of 1590 mS/mm at $V_d = 0.5$ V, the current-gain cutoff frequency f_T was increased from 390 to 494 GHz, and the gate-delay time was decreased from 0.83 to 0.78 ps at supply voltage of 0.6 V. This is the highest f_T achieved for 80-nm-gate-length HEMT devices. These superior performances are attributed to the reduction of distance between gate and channel and the reduction of parasitic gate capacitances during the gate-sinking process. Moreover, such superior performances were achieved through a very simple and straightforward fabrication process with optimal epistructure of the device.**

***Index Terms*—High-electron mobility transistors (HEMTs), InAs, InGaAs, platinum (Pt) buried gate.**

I. Introduction

FOR THE advanced wireless communications, InP-based high-electron mobility transistors (HEMTs) have attracted much attention and demonstrated an excellent high-frequency performance because of its superior electronic transport properties and high saturation velocity [1], [2]. Moreover, it is also a potential candidate FET for low-power logic applications beyond Si CMOS technology in a 22-nm node era [3], [4]. InP HEMTs usually use In-rich InGaAs channel or InAs/InGaAs composite channel for good RF performance with large current drivability of the device. Meanwhile, the gate-recess structure also plays a critical role in the high-frequency performance for HEMT devices. In general, the transconductance (g_m) of the device is mainly influenced by the gate-channel distance, and the reduction of the distance can effectively increase the current-gain cutoff frequency (f_T) because of the enhancement of average electron velocity underneath the gate electrode.

Additionally, the shape of the recessed region not only affects the source and drain resistance (R_s and R_d) and the capacitances of gate source and gate drain (C_{gs} and C_{gd}) but also modulates the electric field in the channel. Shinohara *et al.* [5] reported the f_T value of 547 GHz in 30-nm-gate pseudomorphic HEMTs by means of multilayer cap structure to reduce parasitic source and drain resistances. Matsuzaki *et al.* [6] have employed tiered-edge ohmic structure and low-k benzocyclobutene passivation to effectively minimize parasitic gate capacitance and achieve relatively high g_m and f_T values. Although the results seemed rather promising, yet relatively complicated fabrication processes were involved in the reduction of the parasitic elements.

In this letter, the $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite-channel HEMTs were fabricated with platinum (Pt) buried-gate technology. The Pt buried gate was adopted because Pt can diffuse into the barrier layer and the channel can be further recessed [7]–[9]. The diffused gate has lower parasitic capacitance and resistance as compared with that of the recessed gate. Additionally, Pt has a higher metal work function (5.65 eV) than that of titanium (4.1 eV). The measurement results in this letter clearly evidenced that superior device performance can be achieved through a very simple and straightforward gate-sinking fabrication process with optimal epistructure as compared with those proposed in [5] and [6].

II. Device Fabrication

The HEMT structure was grown by molecular beam epitaxy on a 2-in-diameter InP substrate. The schematic of the structure is shown in Fig. 1 and given as follows. A 50-Å InAs channel layer with 20-Å $In_{0.7}Ga_{0.3}As$ upper subchannel and 30-Å $In_{0.7}Ga_{0.3}As$ lower subchannel was grown on top of the 500-nm-thick InAlAs buffer layer. The $In_{0.7}Ga_{0.3}As$

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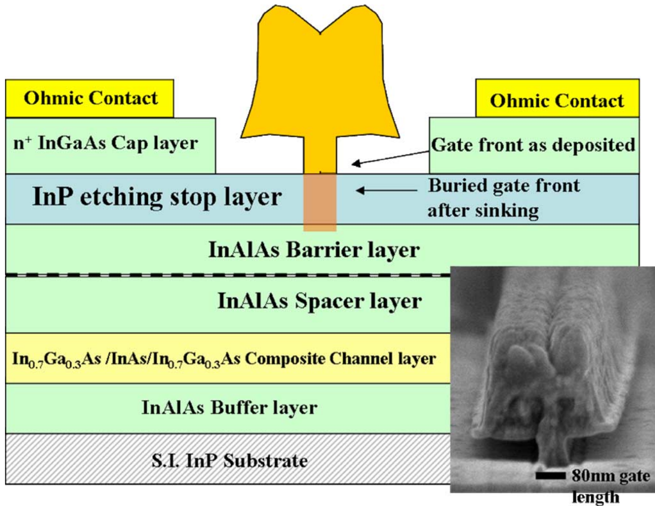

Fig. 1. Schematic view of the device structure. The inserted SEM image is the 80-nm T-shaped gate after recess before silicon nitride passivation.

subchannels were applied to enhance the electron confinement in the thin InAs layer and improve the electron transport properties [10]. A 40-Å-thick InAlAs spacer, a Si-δ-doping with 5×10^{12} cm^{-2}, a 10-nm-thick InAlAs barrier, a 4-nm-thick InP etching stop, and a 35-nm-thick InGaAs cap layer with 2×10^{18} cm^{-3} Si-doping were grown on top of the composite-channel layers.

For the device fabrication, the active area of the device was isolated by wet etch. The ohmic contacts were formed with 3-μm source–drain spacing by evaporating Au/Ge/Ni/Au on heavily doped n-InGaAs cap layer and then alloyed at 250 °C for 25 s to attain low contact resistance (R_c). For the T-shaped gate process, it was performed by the 50-kV JEOL electron beam lithography system (JBX 6000 FS) with trilayer e-beam resist. Succinic acid$/H_2O_2/NH_4$OH solution was used for gate recess, and then, Pt (12 nm)/Ti (60 nm)/Pt (80 nm)/Au (180 nm) were deposited as Schottky gate metal and lifted off by ZDMAC to form an 80-nm T-shaped gate. The inserted SEM image is the unpassivated T-shaped gate formed after recess. A 100-nm-thick silicon nitride was deposited as a passivation layer by plasma-enhanced chemical vapor deposition at 250 °C for 10 min. Finally, thermal annealing at 250 °C for 3 min in forming gas ambient was carried out for gate sinking to further recess the channel. The contact resistance was 0.032 $\Omega \cdot$ mm after gate-sinking process, which remained almost unchanged as compared with that of 0.021 $\Omega \cdot$ mm before annealing.

III. Results and Discussion

Fig. 2(a) shows the dc I–V curve of the device with $2 \times$ 50 μm gate width using gate-sinking technology. The device exhibited a very good pinch-off characteristic and the saturation current of 1418 mA/mm at $V_{\text{ds}} = 1$ V and $V_{\text{gs}} = 0$ V. This very high drain–current density was mainly due to the superior electron mobility in the $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite channel and the nondegrading performance of the ohmic contact during gate annealing. As for the gate–drain breakdown voltage $(V_{\text{DG,BR}})$, the value decreased from 3.6 V for device without sinking to 2.4 V for that with sinking, which is mainly due to the reduction in the Schottky barrier thickness after the gate-sinking process.

The transconductance g_m and the drain–source current plotted as functions of V_{gs} for devices without and with gate annealing are shown in Fig. 2(b). As is observed from the figure, the peak g_m value has increased from 1470 mS/mm for the device without gate sinking to 1590 mS/mm for that with gate sinking, both measured at $V_{\text{ds}} = 0.5$ V. This increase is mainly attributed to the sinking of Pt atoms into the InP etching-stop layer which, in turn, shifted the gate metal front closer to the 2-D electron-gas channel. Meanwhile, the threshold voltage shifted from -0.91 (without gate sinking) to -0.8 V (with gate sinking) when biased at $V_{\text{ds}} = 0.5$ V. The threshold voltage is defined as the V_{gs} when I_{ds} reaches 1 mA/mm. A slight reduction in the gate leakage current from 1.66×10^{-6} A (without gate sinking) to 6.3×10^{-7} A (with gate sinking) was also observed when biased at $V_{\text{ds}} = 0.8$ V and $V_{\text{gs}} = 0$ V, owing to the increase in the thickness of the amorphous layer under gate which diminished the leakage path because of the reduction of the grain boundaries [8], [11].

The S parameters of the 2×50 μm device were measured from 5 to 80 GHz using on-wafer probing system with HP8510XF network analyzer. Fig. 3(a) shows the frequency dependence of the current gain H_{21}, the power gain MAG/MSG, and the Mason's unilateral gain U of the device with gate sinking measured at $V_{\text{ds}} = 0.8$ V and $V_{\text{gs}} = -0.5$ V. The parasitic effects (mainly capacitive) due to the probing pads have been carefully removed from the measured S parameters using the same method as in [12] and the equivalent circuit model in [13]. Since the geometry of the probing pads is relatively large compared with the device itself, the S parameters of the open probing pads have been carefully characterized through full-wave electromagnetic simulations with measurement. The capacitance at the gate–source end was extracted to be 10.2 fF, and the capacitance at the gate–drain end was about 8.6 fF. A very high current-gain cutoff frequency f_T of 494 GHz and the maximum oscillation frequency $f_{\max}$ of 390 GHz were obtained for device with sinking as compared with that of $f_T = 390$ GHz and $f_{\max} = 360$ GHz for the device without sinking. This improvement in the RF performance was due to the increase of g_m and the decrease of the gate-to-source capacitance (C_{gs}) in the applied gate bias range resulting from the gate-sinking process. Similar trend of the reduction in C_{gs} values due to the gate-sinking process has also been observed in [14]. Table I summarizes the extracted intrinsic parameters for devices with and without gate sinking at the same bias conditions. The increase in f_T is mainly caused by the decrease of C_{gs} and the increase of the transconductance.

The effect of gate sinking on the gate-delay performance of the HEMT device is also evaluated. To avoid erroneous and physically meaningless values of logic parameters in characterizing such nonoptimized threshold-voltage device, we have followed the method proposed in [15]. A subthreshold slope of 115 mV/dec and a drain-induced barrier lowering (DIBL) of 200 mV/V after gate sinking were obtained. For device without gate sinking, the subthreshold slope and the DIBL were 115 mV/dec and 178 mV/V, respectively. Fig. 3(b) shows the calculated intrinsic gate delay (CV/I) as a function of

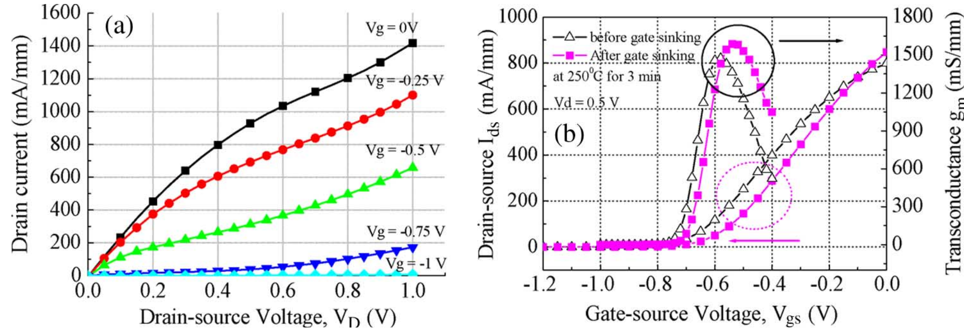

Fig. 2. (a) Drain–source current versus drain–source voltage curve. (b) Transconductance versus gate–source voltage before and after gate sinking at 250 °C for 3 min.

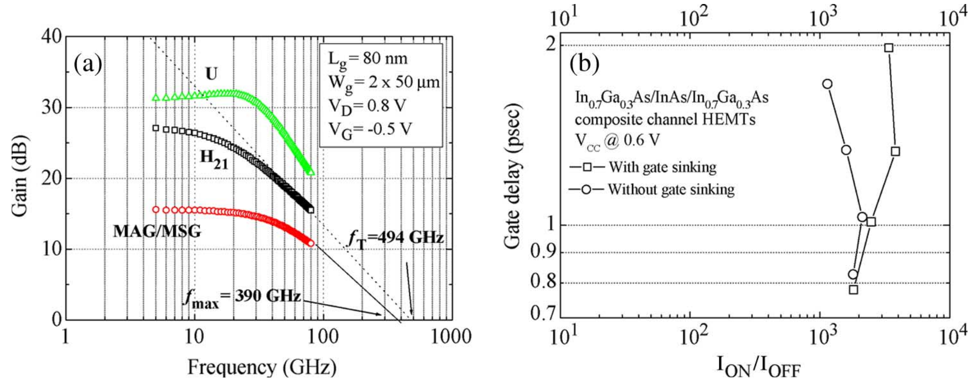

Fig. 3. (a) Frequency dependence of the current gain H_{21}, the power gain MAG/MSG, and the unilateral gain U of the $InAs/In_{0.7}Ga_{0.3}As$ composite-channel HEMTs. The frequency range was from 5 to 80 GHz, and the device was biased at $V_{ds} = 0.8$ V and $V_{gs} = -0.5$ V. (b) Calculated intrinsic gate delay as a function of I_{ON}/I_{OFF} ratio with various choices of the threshold voltage for device with and without sinking.

TABLE I
SUMMARY OF THE HEMT DEVICE PARAMETERS WITH AND WITHOUT GATE SINKING

$InAs/In_{0.7}Ga_{0.3}As$ HEMTs	C_{gs}	C_{gd}	C_{ds}	G_m(RF)	f_T(GHz)	f_{max}(GHz)
Without gate sinking	73.3 fF	16.3 fF	5.3fF	201mS	390 GHz	360 GHz
Gate sinking	60.5 fF	16.6 fF	3.7fF	208mS	494 GHz	390 GHz

I_{ON}/I_{OFF} ratio for the device with and without gate sinking and with various choices of the threshold voltage as defined in [16] at $V_{ds} = 0.6$ V. As is observed from the figure, a low calculated gate delay of 0.78 ps for gate-sinking device with I_{ON}/I_{OFF} ratio maintained on the order of 10^3 was achieved as compared with that of 0.83 ps for the device without gate sinking. The very low intrinsic gate-delay performance is again attributed to the decrease in the C_{gs} after the gate-sinking process. These superior performances have also made such device a potential candidate for future high-speed and low-power logic applications.

IV. CONCLUSION

In this letter, the use of the Pt buried-gate technology for the enhancement of the RF and logic performance of the HEMTs has been demonstrated. The HEMTs exhibit high $I_{ds} = 1418$ mA/mm, high $g_m = 1590$ mS/mm, and an $f_T(f_{max})$ of 494 GHz (390 GHz) after gate sinking. This is believed to be the highest value ever achieved for an 80-nm HEMT devices. Additionally, the logic performance of such device has also been characterized, and a very low intrinsic gate delay (0.78 ps) with an I_{ON}/I_{OFF} ratio in the excess of 10^3 was obtained at $V_{ds} = 0.6$ V. Overall, the performance improvement after gate sinking was mainly attributed to the increase of g_m and the decrease in the corresponding capacitances of the device. The results demonstrate that superior HEMT device performance for high-frequency, high-speed, and low-power logic applications can be achieved through a very simple gate-sinking process with optimal epitaxy structure.

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