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Design and fabrication of MEMS logic gates

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Abstract

This paper presents a novel design of MEMS logic gate that can perform Boolean algebra the same as logic devices that are composed of solid-state transistors. This MEMS logic gate design inherits all the advantages from MEMS switches and thus is expected to have more applications than MEMS switches. One unique feature of this device is that it can perform either NAND gate or NOR gate functions with the same mechanical structure but with different electrical interconnects. In a prototype design, the device is 250 μm long, 100 μm wide and has 1 μm gap. The experimental results show that this device can operate at 10/0 V and achieve the proposed logic functions. The resonant frequency of the device is measured roughly at 30 kHz. Due to no metal-to-metal contact in the current device, the logic functions of the design are verified through observations and video taping.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

MEMS (micro-electro-mechanical system) switches are becoming popular in telecommunication applications because they offer several advantages over their counterparts (FET, PIN diodes, etc), such as low power consumption, high isolation, no leakage currents etc [1–3]. These MEMS switches often work with circuits that are composed of solid-state devices, and are responsible for only a small portion of the circuit functions because they are equipped only with on/off functions. Due to their limited capability, their applications are also limited.

The proposed MEMS logic gates are MEMS devices that can perform Boolean algebra [4]. They can function the same as the logic gates that are composed of solid-state transistors (FET, BJT). With this computation capability, MEMS logic gates are expected to have more applications than the existing MEMS switches. For example, the proposed MEMS logic gates can be used to construct a 'full-mechanical' computer. This mechanical computer can work under severe temperatures and strong ion-radiation environments while conventional solid-state transistors would fail [5]. Another important application would be MEMS SoC (system-on-chip) systems. Lots of MEMS devices require on-chip digital circuitry to complete their functionality [6]. However, the fabrication process integration between IC devices and MEMS devices is always an issue. In that case, the proposed MEMS logic gate design offers the flexibility in making digital circuits and thus reduces the barriers of implementing MEMS SoC systems.

Hirata *et al* [7] demonstrated a design of MEMS logic gate. They used these logic gates to replace MEMS switches in an IC power management system and successfully reduced the silicon area required for the I/O pads. In their design, the 'AND' gate and 'OR' gate had almost the same mechanical structure with different dimensions of actuation pads. Lee *et al* [5] proposed another design for MEMS logic gates and intended to create a gate that has the same mechanical structure but can perform different logic functions. Their design is an NMOS-like mechanical transistor, the same as conventional solid-state transistors, and it needed four transistors to form either a 'NAND' or a 'NOR' gate [4].

This paper presents a novel MEMS logic gate design that can be fabricated by surface micromachining. This device uses exactly the same mechanical structure to perform either 'NAND' or 'NOR' gate function depending on the electrical interconnects. Due to the capability of implementing NAND and NOR gate functions, it is possible to realize entire digital circuits solely from the proposed MEMS logic gates. Therefore, this design is suitable to be a building block for digital circuits [5]. The operation of this design relies on an

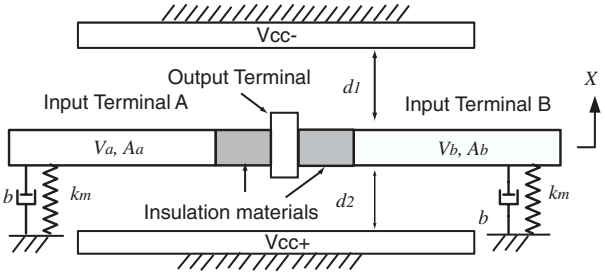


Figure 1. A translational three-layer MEMS logic gate design.

isolation feature in its physical structure, and thus complicates the fabrication process. To demonstrate the logic function of this novel design, a prototype design and the associated fabrication process, which employs polysilicon-to-polysilicon contact [5], are proposed and discussed in detail in this paper.

2. Theory of operation

2.1. A three-layer design

The concept of the proposed MEMS logic gates can be easily understood by the operation of a three-layer, translational, electrostatically-actuated MEMS device. As shown in figure 1, the device consists of one shuttle electrode in the middle and two fixed electrodes on the top and bottom. When the fixed electrodes are biased at the voltages of V_{cc+} and V_{cc-} the shuttle electrode moves either up or down, depending on the voltages applied to it. The probe (output terminal) at the shuttle electrode can connect the top or bottom electrode to export the corresponding output voltage. In short, the logic functions between the input voltage and the output voltage are carried out by the motion of the shuttle electrode.

The motions of the shuttle electrode are determined by the net attractive force from the top (F_{up}) and bottom (F_{down}), and can be described by equations (1),

$$\begin{aligned} m\ddot{x} + b\dot{x} + k_m x &= F_{\text{total}} = F_{\text{up}} - F_{\text{down}} \\ &= \frac{\varepsilon A_a((V_{cc-} - V_a)^2 + (V_{cc-} - V_b)^2)}{2d_1^2} \\ &\quad - \frac{\varepsilon A_a((V_{cc+} - V_a)^2 + (V_{cc+} - V_b)^2)}{2d_2^2}, \end{aligned} \tag{1}$$

where m is the mass of the shuttle electrode; b is the associated damping coefficient; k_m is the spring constant; ε is the permittivity of the air gap; d_1 and d_2 are the gaps between electrodes; V_a and V_b are two input voltages applied to each end of the shuttle electrodes, and A_a and A_b are the respective effective areas for generating the electrostatic force. In this MEMS logic gate design, one gap is designed to be larger than the other ($d_1 > d_2$), and two effective areas are the same ($A_a = A_b$). According to equation (1), altering the magnitudes of the input voltages, V_a and V_b, would affect the shuttle motion and thus the following four situations occur. (1) $V_a = V_{cc+}$, $V_b = V_{cc-}$: in this case, the voltage difference between the top electrode and the shuttle electrode is the same as that between the bottom electrode and the shuttle electrode.

Table 1. Input–output relations of a mechanical NAND gate.

Cases	V_a	V_b	Output
(1)	$V_{cc+}(1)$	$V_{cc-}(0)$	$V_{cc+}(1)$
(2)	$V_{cc+}(1)$	$V_{cc+}(1)$	$V_{cc-}(0)$
(3)	$V_{cc-}(0)$	$V_{cc-}(0)$	$V_{cc+}(1)$
(4)	$V_{cc-}(0)$	$V_{cc+}(1)$	$V_{cc+}(1)$

Because the gap d_1 is larger than d_2, the electrostatic force F_{up} is smaller than F_{down}. The shuttle electrode moves downward and connects the bottom electrode to export the output voltage V_{cc+}. (2) $V_a = V_{cc+}$, $V_b = V_{cc+}$: in this case, F_{down} is zero because there is no voltage drop between the bottom electrode and the shuttle electrode. The shuttle electrode moves upward and connects the top electrode to export the output voltage V_{cc-}. (3) $V_a = V_{cc-}$, $V_b = V_{cc-}$: F_{up} is zero because there is no voltage drop between the top electrode and the shuttle electrode. The shuttle electrode moves downward and connects the bottom electrode to export the output voltage V_{cc+}. (4) $V_a = V_{cc-}$, $V_b = V_{cc+}$: this is the same situation as that in case (1). These four situations are listed in table 1. If the voltage levels of V_{cc+} and V_{cc-} represent the '1' and '0' in digital circuitry, respectively, the input–output relations of this device are the same as the 'NAND' gate that is composed of solid-state transistors.

In addition to the advantage of no leakage current, the proposed design offers two more advantages. (1) The output terminal would connect the fixed electrodes either on the top or bottom in all combinations of input signals. Therefore, this logic device does not have undefined states [4], which is an issue in some logic devices composed of solid-state transistors. (2) When reversing the bias voltages on the top and bottom electrodes, the logic function of this device switches from a NAND gate to a NOR gate. Therefore, with this design, the mechanical 'NOR' gate and 'NAND' gate can have the same mechanical structure with different electrical interconnects.

Due to the three-layer structure, this design is difficult to fabricate by surface micromachining. However, this design can be rotated by 90° and fabricated by bulk micromachining while the resulting actuation voltage is kept as low as 20 V [8].

2.2. A two-layer design

In order to integrate with existing solid-state transistors, a two-layer MEMS logic gate, suitable for surface micromachining, is proposed. According to figure 2, the shuttle electrode does a see-saw motion and connects the output terminal on each end to export the corresponding output voltage. Different from the three-layer design wherein its logic function is facilitated by different voltages and different gaps, the logic function of the two-layer design is facilitated by different voltages and different dimensions of actuation pads (A_l and A_r in figure 2). With careful design of input voltages and device dimensions, this two-layer structure can perform the logic function and have all the advantages discussed in the three-layer design.

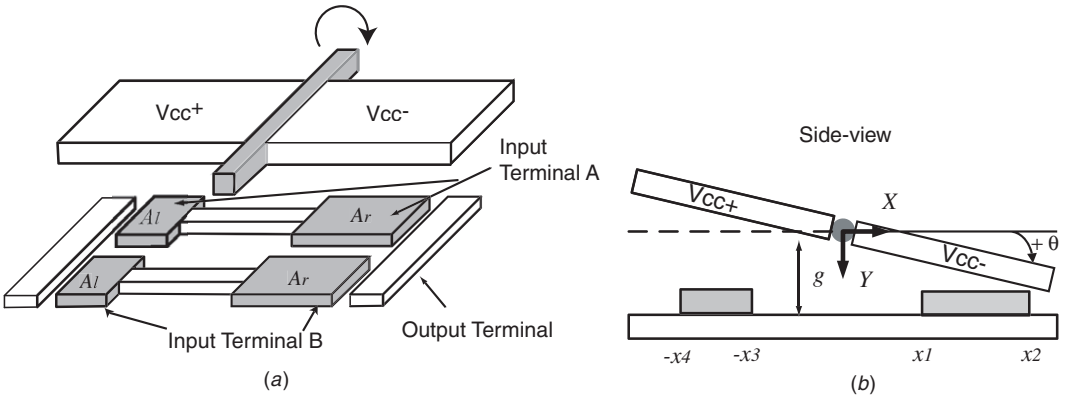


Figure 2. A torsional two-layer MEMS logic gate design. (*a*) 3D view; (*b*) side view.

3. Design of MEMS logic gates

According to the operation of MEMS logic gates, the design task is to ensure that the probe would move in the designated direction and connect the output terminal at each end. This is achieved by the design of pull-in voltages and dimple structures. They are discussed in the following.

3.1. Dynamics of MEMS logic gates

In this design (figure 2), the area responsible for generating the electrostatic torque is different on two sides of the plate. The dynamics of this electrostatically-actuated tilting plate can be described by the following:

$$I_\theta \ddot{\theta} + C_\theta \dot{\theta} + K_t \theta = M_R - M_L, \tag{2}$$

where I_θ is the moment of inertia of the tilting plate; C_θ is the damping coefficient of the system; K_t is the torsion stiffness; M_R and M_L represent the respective electrostatic torque on the right and left sides of the plate. The electrostatic torque generated by different dimensions of electrodes can be derived as

$$\begin{aligned} M_R &= \frac{\varepsilon\omega((V_{cc+}-V_a)^2+(V_{cc+}-V_b)^2)}{2}\int_{x_1}^{x_2}\frac{x}{(g-x\theta)^2}\,\mathrm{d}x \\ &= V_R \times \frac{(x_2-x_1)g\theta-(g-x_1\theta)(g-x_2\theta)\ln((g-x_1\theta)/(g-x_2\theta))}{\theta(g-x_1\theta)(g-x_2\theta)} \\ M_L &= V_L \times \frac{(x_4-x_3)g\theta-(g-x_3\theta)(g-x_4\theta)\ln((g-x_3\theta)/(g-x_4\theta))}{\theta(g-x_3\theta)(g-x_4\theta)} \\ V_R &= \frac{\varepsilon\omega((V_{cc+}-V_a)^2+(V_{cc+}-V_b)^2)}{2} \\ V_L &= \frac{\varepsilon\omega((V_{cc-}-V_a)^2+(V_{cc-}-V_b)^2)}{2} \end{aligned} \tag{3}$$

where ω is the width of the plate; g is the gap of the tilting plate; x_1, x_2, x_3, x_4 are the location coordinates of the electrode that generates the electrostatic torque. The resilient torque of the system is implemented by the micro flexures on two sides of the plate. The torsion stiffness K_t of a micro flexure with 'non-warping end plane' can be precisely calculated by the following equations [8]:

$$K_t = \frac{1}{3L}Gw_s h^3\left(1-0.6324\frac{h}{w_s}\right) \qquad w_s > h \tag{4}$$

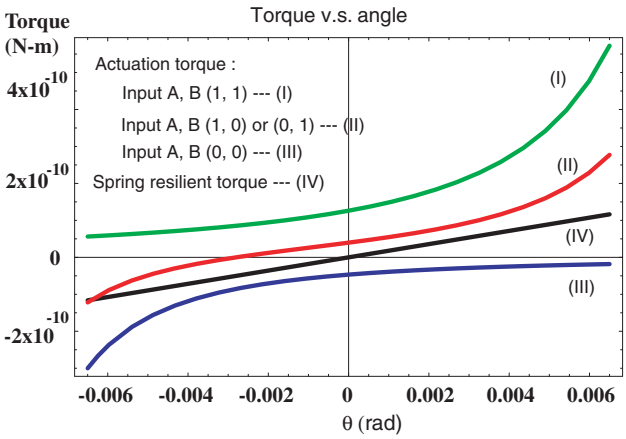


Figure 3. The actuation torque and resilient torque in the two-layer MEMS logic gate design. The torque with positive values rotates the plate clockwise, while that with negative values rotates the plate counterclockwise.

where G is the shear modulus; w_s and h are the cross-sectional width and height of the micro flexure, respectively; L is the length of the micro flexure.

3.2. State transition of MEMS logic gates

State transition is one of the most important indicators for the feasibility of digital IC devices [4]. In the proposed mechanical gate design, the state transition is achieved by the tilting plate switching from one quiescent point, where the plate connects the output terminal at one end, to the other quiescent point in different combinations of input signals. To investigate this, the resilient torques from micro flexures and the actuation torques from the electrostatic force are drawn in one plot for all combinations of input signals and for all plate-tilting angles. As shown in figure 3, the actuation torque is always positive for two input signals both at V_{cc+} ((1,1) in the plot), while it is always negative for both input signals at V_{cc-} ((0,0) in the plot). The resilient torque is a straight line that passes through the origin, and the slope of the line represents the torsion stiffness. Therefore, it is possible to design micro flexures such that the resilient torque is in between the actuation torques of cases

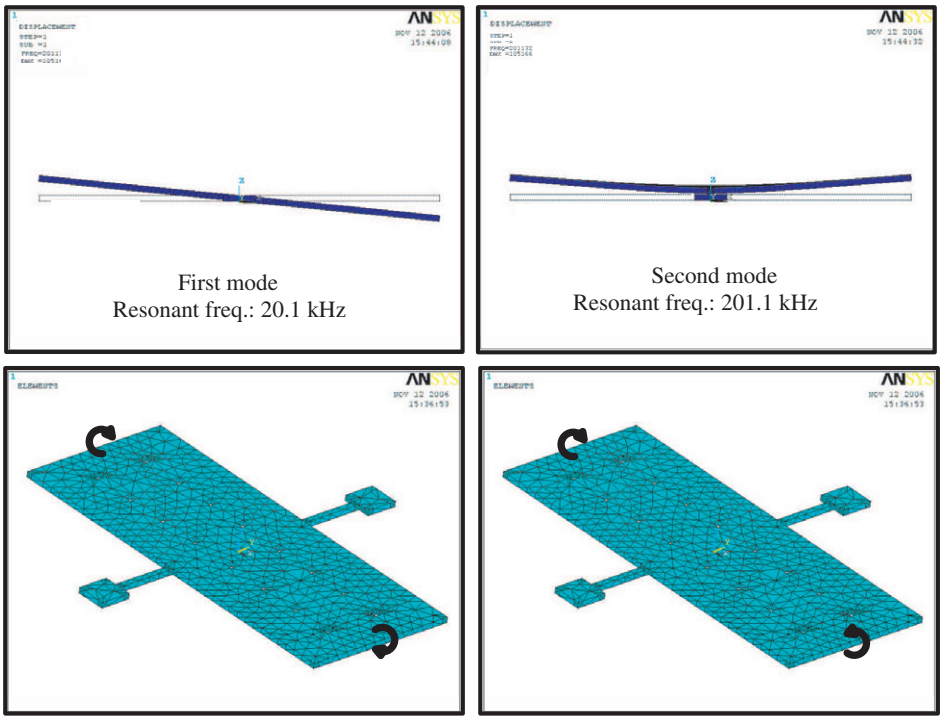


Figure 4. Modal analysis of the device by FEM simulations. (*a*) First mode: torsion, 20.1 kHz. (*b*) Second mode: bending, 201.1 kHz.

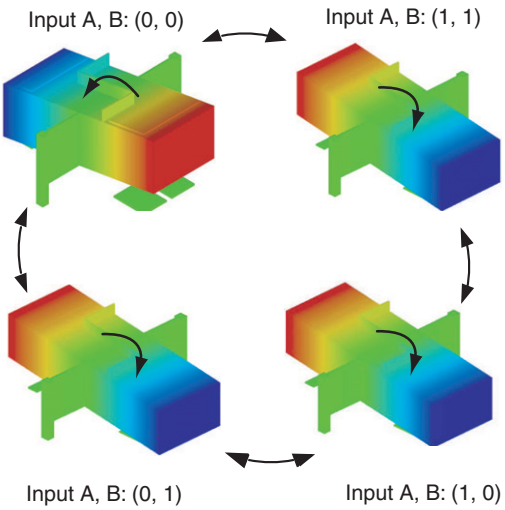


Figure 5. FEM simulations (Coventorware) of state transitions. The input voltage sequence is $(0, 0) \leftrightarrow (1, 1) \leftrightarrow (1, 0) \leftrightarrow (0, 1)$. The plate rotates in the designated direction to realize the NOR gate function.

(1,1) and (0,0). And this is done by choosing a torsion stiffness such that the resulting pull-in voltages of cases (1,1) and (0,0) are smaller than the corresponding input voltages. In that case, the net torque in case (1,1) is always positive and the plate can be actuated from any angle to the angle where it connects the output terminal on the right. Similarly, in case (0,0), the plate can be actuated from any angle to the angle where it connects the output terminal on the left.

Table 2. Dimensions and parameters of the MEMS logic gate.

Plate length	250 μm
Plate width	100 μm
Electrodes locations	50 μm, 100 μm
(x_1, x_2, x_3, x_4 shown in figure 2)	-85 μm,-100 μm
Actuation voltages V_{cc+}, V_{cc-}	10, 0 V
Gap (g)	1 μm
Dimple height	0.5 μm
Max. plate angle	$\pm 4 \times 10^{-3}$ rad
Pull-in voltage of cases (1,1) and (0,0) —3 μm flexure width	4.15/6.32 V
Pull-in voltage of cases (1,1) and (0,0) —4 μm flexure width	5.13/7.82 V
Quiescent angle for case (1,0)/(0,1) 3 μm/4 μm (flexure width)	-5.4×10^{-3}/ -6.4×10^{-3} rad
Expected bandwidth 3 μm/4 μm (flexure width)	20 kHz/33 kHz

When the input signals are the combinations of either (V_{cc+}, V_{cc-}) or (V_{cc-}, V_{cc+}), the plate should be rotated clockwise at any initial angle and then connects the output terminal to facilitate the NOR gate function. In these cases ((1,0) and (0,1) in the plot), it is impossible to obtain a design such that the actuation torque is always larger than the resilient torque at all tilting angles. However, if the movement of the tilting plate is constrained within a range, for example ± 0.006 rad in the plot, the actuation torque is larger than the resilient torque and the plate can be rotated clockwise.

The pull-in voltages (V_p) of cases (1,1) and (0,0) are the key design parameters to this design and they can be obtained

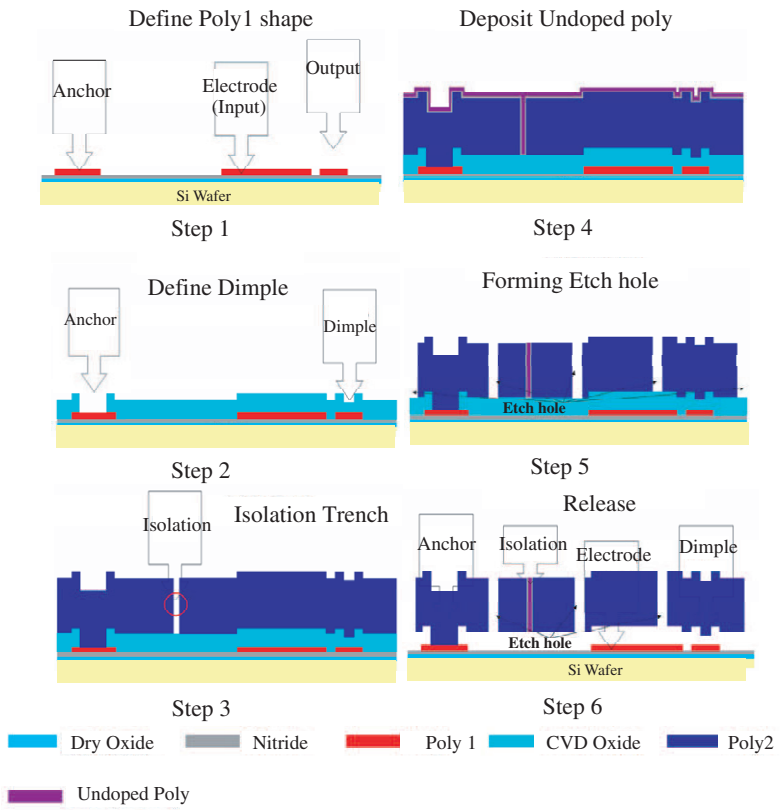


Figure 6. Process flow of the nitride isolation process.

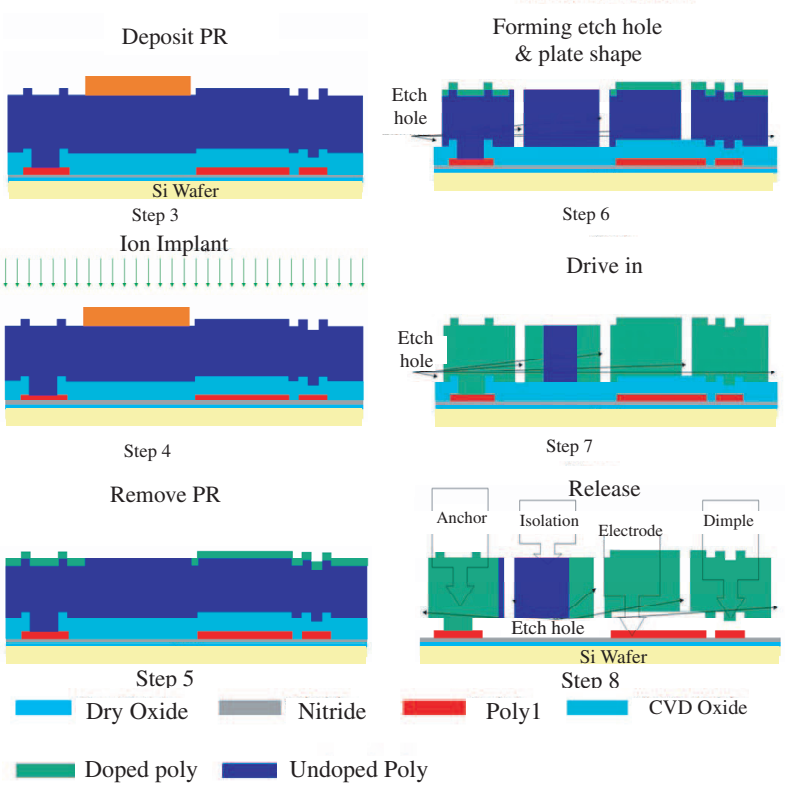
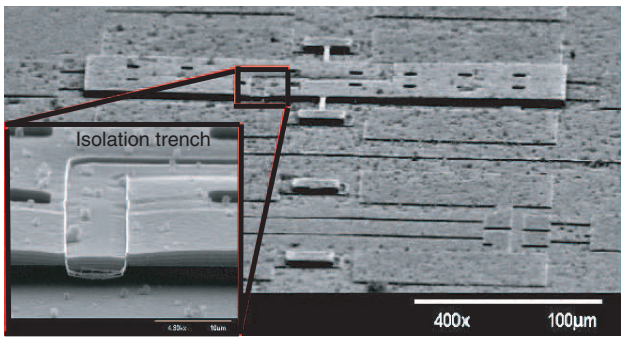
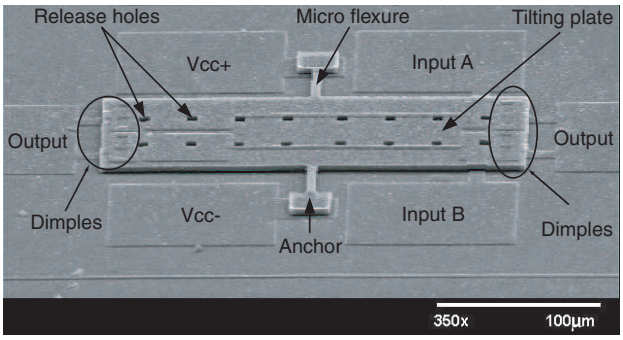


Figure 7. Process flow of the ion implantation process.



(*a*)



(*b*)

Figure 8. SEM photos of the fabricated MEMS logic gates. (*a*) Device fabricated by the nitride isolation process. (*b*) Device fabricated by the ion implantation process.

by equation (5).

$$\left.\frac{\partial M_R}{\partial \theta}\right|_{\theta=\theta_s} = K_t = \frac{M_t}{\theta} = \left.\frac{M_R}{\theta}\right|_{\theta=\theta_s}$$

$$V_p = \frac{\theta_s^{3/2}\sqrt{(g-x_1\theta_s)(g-x_2\theta_s)K_t}}{\sqrt{\varepsilon\omega}\sqrt{(x_2-x_1)g\theta_s-(g-x_1\theta_s)(g-x_2\theta_s)\ln\left(\frac{g-x_1\theta_s}{g-x_2\theta_s}\right)}}, \quad (5)$$

where M_t is the resilient torque from micro flexures; θ_s is the snap down angle.

3.3. Dimple design

The range of the tilting angle is determined by the plate length and the gap. However, changing either of them would alter the performance of the device to a large extent. Therefore, the dimple structure is used to limit the plate-moving range without changing the plate dimensions and actuation torques. Besides, this structure can be used to avoid the stiction problem which takes place at the physical contact between the two layers [9, 10].

3.4. Simulation results

The key dimensions and parameters of the proposed design are shown in table 2. Two different flexure widths, 3 μm and 4 μm, are used for the design and fabrication of torsional springs. As shown in table 2, the applied voltages $(V_{cc+}, V_{cc-}) = (10,0)$ V exceed the pull-in voltages of cases (1,1) and (0,0). The dimple design constrains the maximum tilting angle within $\pm 4 \times 10^{-3}$ rad, and thus the quiescent point of the cases (1,0)/(0,1), -5.4×10^{-3} and -6.4×10^{-3} rad for 3 μm and 4 μm design respectively, cannot be reached. Therefore, the proper state transition, discussed in section (3.2), is ensured. The expected bandwidth is 20 kHz for the 3 μm flexure-width design and 33 kHz for the 4 μm flexure-width design.

To verify the feasibility of this design, FEM simulations of device dynamics and logic functions are performed on the design with 3 μm flexure width. The modal analysis is performed using the commercial software ANSYS [11]. As shown in figure 4, the first resonant mode is torsional motion and its resonant frequency is 20.1 kHz; the second mode is the plate bending motion (up-and-down) and the resonant frequency is 201.1 kHz. The frequency of the second mode is ten times higher than that of the first mode, and thus the second mode would not interfere with the first mode (designated) motion of the plate. The CoventorWare simulation tool [12] can convert the mask layout into an FEM simulation model. Therefore, it is used for the final check of state transition. The applied voltages in simulations are 10 V and 0 V, which represent the (1/0) signal in digital circuits. According to the simulation results shown in figure 5, when a sequence of input voltages $((0,0) \leftrightarrow (1,1) \leftrightarrow (1,0) \leftrightarrow (0,1))$ is applied to the proposed design, the plate can rotate in the designated direction to realize a NOR gate function.

4. Fabrication process

As shown in figures 1 and 2, the proposed logic gate design requires two voltage levels on a plate, which presents the biggest challenges in fabricating the device. Two different processes are proposed herein, which are referred to in this paper as the 'nitride isolation' process and the 'ion implantation' process.

4.1. Nitride isolation process

In the nitride isolation process, the isolation feature is achieved by trenching the plate and refilling it with the isolation compound, which includes undoped polysilicon and the silicon nitride. The fabrication process is shown in figure 6. This process starts with (100) n-type silicon wafers and is followed by dry oxide and silicon nitride deposition for stress buffering and electrical isolation. A 0.5 μm polysilicon layer is deposited on top of the nitride layer and patterned for the electrodes and electrical interconnects. In steps 2 and 3, a 1 μm oxide layer is deposited as the sacrificial layer, which is used to form the gap of the device. This sacrificial layer is patterned by the dimple mask, from which 0.5 μm notches are transferred into the sacrificial layer. After that, another 3 μm of highly doped polysilicon layer is deposited for the structure layer of the device. In step 4, after trenching the structure layer, a low-stress silicon nitride film and an undoped polysilicon film are deposited to seal the trenches. Next, an etch-back process is performed to remove these isolation compounds on the top of the structure layer. The micro flexures, tilting plate, release holes, etc are patterned on the structure layer in step 5 and

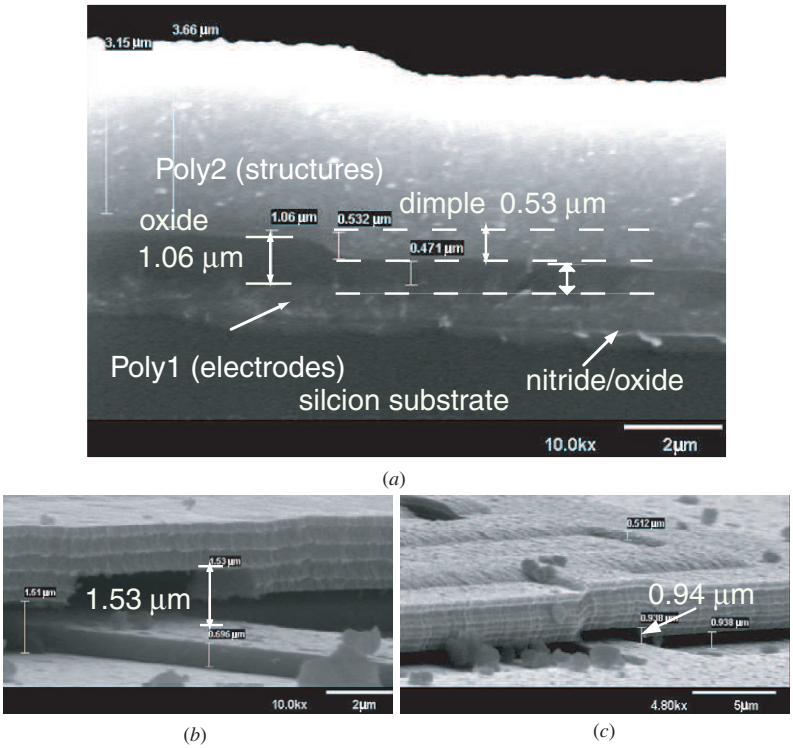


Figure 9. The suspended plate curls up with the nitride isolation process while it does not with the ion implantation process. (*a*) The gap before release is 1.06 μm. (*b*) The gap after release is 1.53 μm with the nitride isolation process. (*c*) The gap after release is 0.96 μm with the ion implantation process.

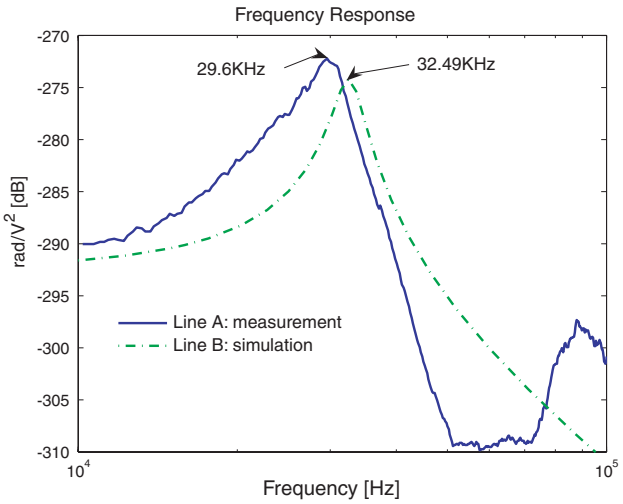


Figure 10. Frequency response of the MEMS logic gate. The first resonant mode is measured at 29.6 kHz, while it is predicted to be 32.49 kHz by simulations.

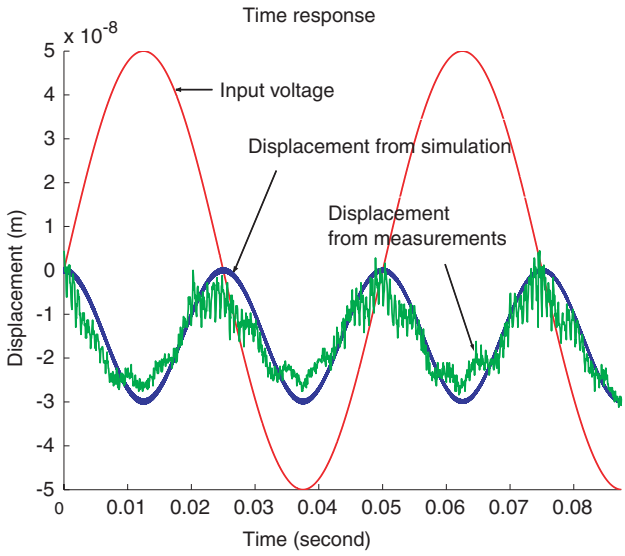


Figure 11. Time response of the MEMS logic gate. The input signal is 10 $\sin(40\pi t)$ V and the plate displacement is roughly 30 nm.

released by HF acid vapor in step 6. Totally, five masks are used to complete this fabrication process.

Two main difficulties in this process are (1) the etch-back process requires the nitride etch to stop on the polysilicon film. However, the selectivity between the nitride etch and polysilicon etch is usually not good. Therefore, it is either under-etch such that the residual nitride is left on the structure layer to curl the suspended structure, or over-etch such that the structure layer and isolation trenches are attacked; (2) the aspect ratio of the isolation trench is low in surface micromachining. Therefore, the etch-back process could severely damage the isolation compound to break the suspended plate into two pieces.

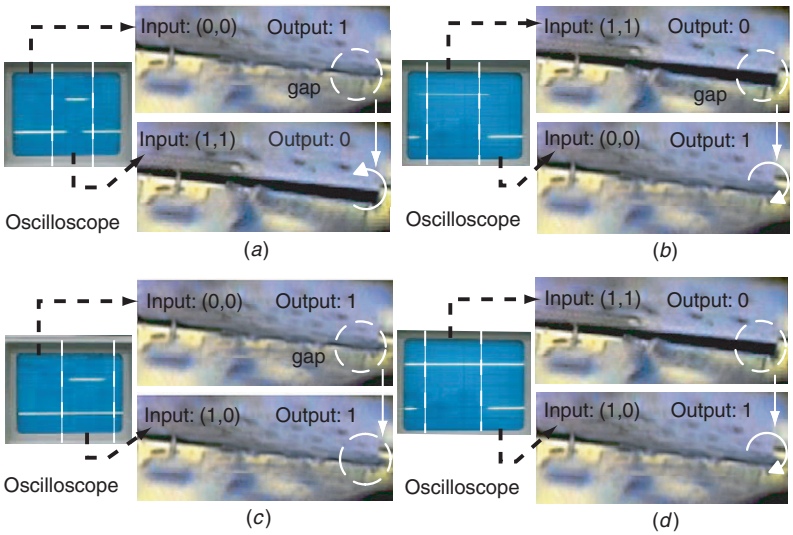


Figure 12. State transition of the proposed device (NAND gate function). (*a*) Input: (0,0) to (1,1) → output: 1 to 0 (counterclockwise rotation). (*b*) Input: (1,1) to (0,0) → output: 0 to 1 (clockwise rotation). (*c*) Input: (0,0) to (1,0) → output: 1 to 1 (no rotation). (*d*) Input: (1,1) to (1,0) → output: 0 to 1 (clockwise rotation).

4.2. Ion implantation process

Instead of using the isolation trenches to divide the one-pieced conductive material into two electrical isolated segments, the ion implantation process uses ion implantation techniques to define the separated conductive regions on the dielectric material. In this process (shown in figure 7), the first two steps are the same as those in the nitride isolation process, except that the undoped polysilicon is used for the structure layer. In step 3, the boron atoms are introduced to the undoped polysilicon film by ion implantation. The driving voltage and the boron dosage are 200 keV and $5 \times 10^{15}\,\mathrm{cm}^{-2}$, respectively. After this, the micro flexures and suspended plates are patterned on the structure layer in step 6. In step 7, the boron atoms are driven deep into the polysilicon film and activated at a temperature of 1100° C for 1 hour. Step 8 releases the structure. This process consists of five masks.

5. Experimental results and discussion

Figure 8 shows the proposed MEMS logic gates fabricated by the nitride isolation process and ion implantation process, respectively. As shown in figure 8(*a*), the isolation trench electrically isolates the suspended plate from left to right so that the plate can be biased at V_{cc+} at the left end and at V_{cc-} at the right end. In both fabrication processes, the V_{cc+} and V_{cc-} are given to the anchor and then transferred through micro flexures to the suspended plate. Two input signals are given to the input terminal A and B. The dimple structures are underneath the tilting plate on two ends, and thus they are not clearly shown. Two output terminals on the far right and left are for the ease of signal readout. They will be linked together through electrical interconnects later on.

5.1. Gap dimensions

Figure 9(*a*) shows the detailed dimensions of the device before release. The gap is 1.06 μm and the height of the dimple is 0.53 μm; this leads to 0.0042 rad for the maximum tilting angle of the plate. After release, the device fabricated by the nitride isolation method is shown in figure 9(*b*) and by the ion implantation method in figure 9(*c*). The suspended plate curls up significantly in the nitride isolation process due to the residual nitride on the top of the structure layer. And because of the process non-uniformity, the thickness of this residual nitride varies from one device to another. After measuring ten devices, the gap at the end of the plate is 1.25 μm on average in the nitride isolation process and 0.96 μm on average in the ion implantation process.

5.2. Frequency response and time response

Due to the process capability, we had more success in fabricating devices with 4 μm flexure width, and thus the experiments of the frequency response and the time response are performed on them. The resonant frequency of the device is measured by an LDV (laser virbrometer doppler) and a network analyzer. As shown in figure 10, the resonant frequency is measured at 29.6 kHz while it is predicted at 32.34 kHz, using the dimensions from the fabricated device and equations (2). The deviation is of about 8%. The damping ratio for this device, calculated from the experimental data, is 0.061.

The time response of the tilting plate is performed by applying a voltage $10\sin(40\pi t)$ V to one of the input terminals while the voltage to the other input terminal is kept at zero volts. As shown in the experimental data (figure 11), the plate is moving at a frequency twice as fast as the actuation frequency. The plate moving distance (30 nm) is close to the

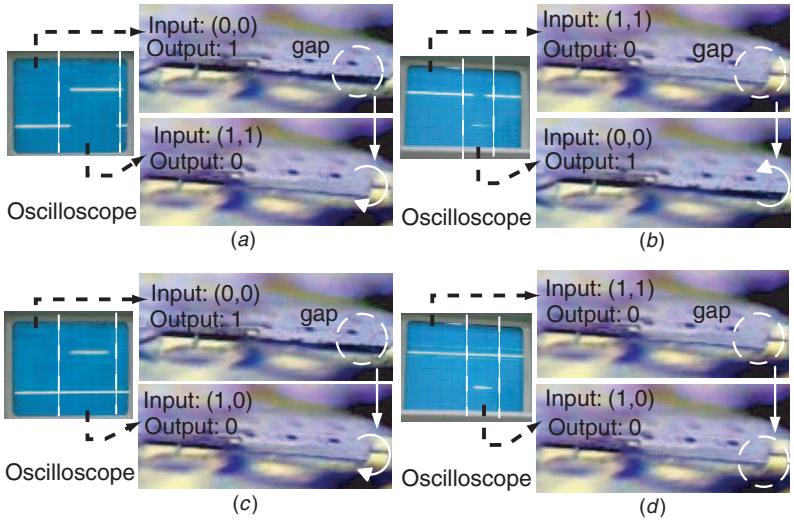


Figure 13. State transition of the proposed device (NOR gate function). The difference between this plot and figure 12 is the electrical interconnects

distance predicted by its mathematic model (equations (2) and (3)). Although the plate moving distance is quite small and thus the signal-to-noise ratio is not good, we cannot enlarge the moving distance by increasing the input voltage in this case. This is because this input voltage is already close to the pull-in voltage, which is predicted at 10.5 V by simulations.

5.3. Logic function tests

Due to no metal-to-metal contact in this prototype design, the contact resistance is large and thus the electrical readout is impossible. The logic functions of this device are verified through observations and video taping. As shown in figure 12, in each of the four cases, the oscilloscope reading is shown in the left to indicate the change of input signals; the plate motion is shown in the right to indicate the corresponding output signals. For example, in case (a), the input signals switch from (0,0) to (1,1), and the plate rotates counterclockwise so that the output signal switches from 1 to 0. After examining the listed four cases (a) to (d), the device can perform the NAND gate function with smooth state transitions. It is noted that the oscilloscope shows two input signals simultaneously. Therefore, if two input signals are the same ((1,1) or (0,0)), their oscilloscope readings overlap each other and thus only one line is visualized.

A similar experiment is performed when the bias voltages are switched on the tilting plate. As shown in figure 13, the plate can rotate in the designated manner to realize the NOR gate function. Therefore, it is concluded that the proposed design can perform either the NAND gate or the NOR gate function depending on the electrical interconnects.

6. Conclusion

This paper presents design procedures and fabrication processes in detail for a novel MEMS logic gate. The logic function of this MEMS device comes from the careful design of different dimensions of actuation pads, pull-in voltages and the dimple structure. In a prototype design, the device is 250 μm long, 100 μm wide and has 1 μm gap. The experimental results show that this device can operate at 10/0 V and achieve the proposed logic functions. The resonant frequency of the device is measured roughly at 30 kHz. Due to no metal-to-metal contact in the current design, the electrical readout of the device is not yet available. Three unique features of this design are verified through observations and video taping. They are the logic function of the device, the advantage that the proposed design can perform NAND gate and NOR gate functions with the same mechanical structure, and no undefined state of this logic device.

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