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2008 Jpn. J. Appl. Phys. 47 2097

(http://iopscience.iop.org/1347-4065/47/4R/2097)

Japanese Journal of Applied Physics
Vol. 47, No. 4, 2008, pp. 2097–2102

Investigation of Random Dopant Fluctuation for Multi-Gate Metal–Oxide–Semiconductor Field-Effect Transistors Using Analytical Solutions of Three-Dimensional Poisson's Equation

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(Received September 28, 2007; accepted January 29, 2008; published online April 18, 2008)

This paper investigates the random dopant fluctuation of multi-gate metal–oxide–semiconductor field-effect transistors (MOSFETs) using analytical solutions of three-dimensional (3D) Poisson's equation verified with device simulation. Especially, we analyze the impact of aspect ratio on the random dopant fluctuation in multi-gate devices. Our study indicates that with a given total width, lightly doped fin-type FET (FinFET) shows the smallest threshold voltage (V_{th}) dispersion because of its smaller V_{th} sensitivity to the channel doping. For heavily doped devices, quasi-planar shows smaller V_{th} dispersion because of its larger volume. The V_{th} dispersion caused by random dopant fluctuation may still be significant in the lightly doped channel, especially for tri-gate and quasi-planar devices. [DOI: 10.1143/JJAP.47.2097]

KEYWORDS: multi-gate MOSFETs, FinFET, tri-gate, 3-D Poisson's equation, random dopant fluctuation

1. Introduction

Due to its better gate control, multi-gate structure is an important candidate for complementary metal–oxide–semiconductor (CMOS) scaling.[1–3] Dependent on the aspect ratio (AR), fin-type field-effect transistor (FinFET) (AR > 1), tri-gate (AR = 1) and quasi-planar (AR < 1) devices are typical options in the multi-gate device design. Whether there is an optimum choice among the three options merits investigation.

With the scaling of device geometry, random dopant fluctuation has become a crucial issue to device design. Although Thean *et al.*[4] have examined the threshold voltage (V_{th}) variations of doped and undoped FinFET devices experimentally, a detailed analysis of the random dopant fluctuation in multi-gate MOSFETs has rarely been seen. In this work, we compare the V_{th} dispersion caused by random dopant fluctuation for FinFET, tri-gate and quasi-planar devices with both heavily doped and lightly doped channels using analytical solution of three-dimensional (3-D) Poisson's equation. Through our theoretical model, the impact of device aspect ratio on the random dopant fluctuation in multi-gate MOSFETs is examined.

This paper is organized as follows. In §2, we derive an analytical potential distribution for a generic multi-gate device structure. The threshold voltage can then be determined based on the potential solution. In §3, we investigate the V_{th} variation caused by random dopant fluctuation for multi-gate devices with various aspect ratio based on our theoretical calculation. The conclusion will be drawn in §4.

2. Potential Solution and V_{th} Calculation

An analytical potential solution is crucial to the derivation of device subthreshold characteristics such as V_{th}. Figure 1(a) shows the schematic sketch of a multi-gate silicon-on-insulator (SOI) structure. The Si-fin body covered by gate insulator is a cuboid with six faces, and each face is connected to a voltage bias. In the subthreshold regime, the Si-fin body is fully depleted with negligible mobile carriers. Therefore, the potential distribution, $\phi(x, y, z)$, satisfies the Poisson's equation:

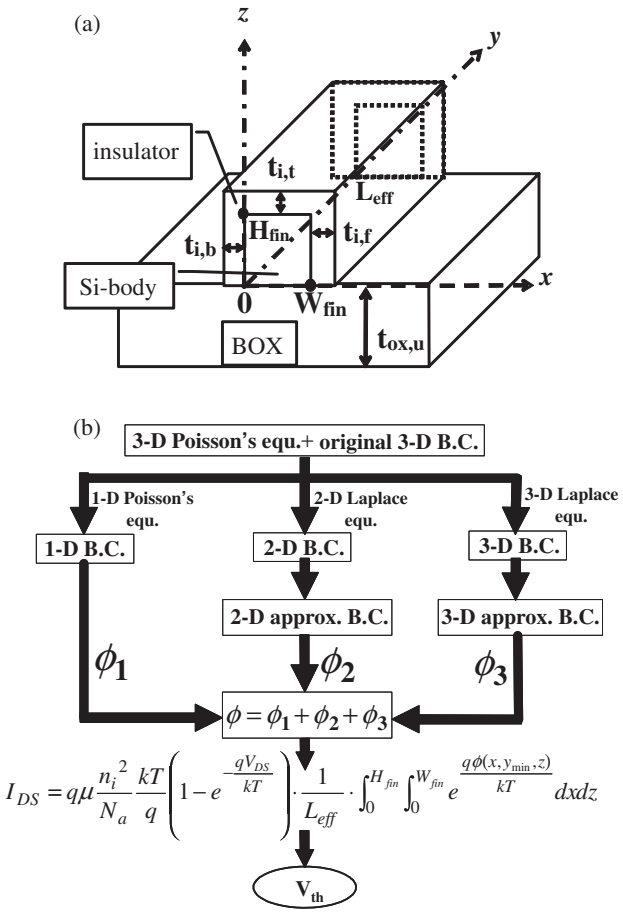

Fig. 1. (a) Schematic sketch of the multi-gate device structure investigated in this study. (b) Flow chart demonstrating the V_{th} calculation of multi-gate devices. Approximation was made to simplify the 2-D and 3-D boundary conditions (B.C.) to obtain a simplified channel potential solution form.

$$\frac{\partial^2\phi(x,y,z)}{\partial x^2} + \frac{\partial^2\phi(x,y,z)}{\partial y^2} + \frac{\partial^2\phi(x,y,z)}{\partial z^2} = -\frac{qN_a}{\varepsilon_{si}}, \quad (1)$$

where N_a is the doping concentration of the Si-fin. The required boundary conditions can be described as

$$\phi(W_{fin}, y, z) + t_{i,f}\frac{\varepsilon_{si}}{\varepsilon_i} \cdot \left.\frac{\partial\phi(x,y,z)}{\partial x}\right|_{x=W_{fin}} = V_{fg} - V_{fb}, \quad (2a)$$

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$$\phi(0,y,z) - t_{i,b}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial x}\right|_{x=0} = V_{bg} - V_{fb}, \quad (2b)$$

$$\phi(x,y,H_{fin}) + t_{i,t}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial z}\right|_{z=H_{fin}} = V_{tg} - V_{fb}, \quad (2c)$$

$$\phi(x,y,0) - t_{ox,u}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial z}\right|_{z=0} = V_{ug} - V_{fb}, \quad (2d)$$

$$\phi(x,0,z) = -\phi_{ms}, \quad (2e)$$

$$\phi(x,L_{eff},z) = -\phi_{ms} + V_{DS}, \quad (2f)$$

where ε_{si}, ε_i, and ε_{ox} are dielectric constants of the Si-fin, gate dielectric, and oxide, respectively. W_{fin}, H_{fin}, and L_{eff} are defined as fin width, fin height, and channel length, respectively. $t_{i,t}$, $t_{i,f}$, $t_{i,b}$, and $t_{ox,u}$ are thicknesses of top gate dielectric, front gate dielectric, back gate dielectric, and buried oxide, respectively. V_{fg}, V_{bg}, V_{tg}, V_{ug}, and V_{DS} are the voltage biases of front gate, back gate, top gate, buried gate and drain terminal, respectively. V_{fb} is the flat-band voltage for these gate terminals. ϕ_{ms} is the built-in potential of the source/drain to the channel.

Figure 1(b) shows the flow chart of the V_{th} calculation by solving the 3-D boundary value problem. This 3-D boundary value problem can be divided into three sub-problems, including one-dimensional (1-D) Poisson's equation, two-dimensional (2-D) and 3-D Laplace equation. Using the superposition principle, the complete potential solution is $\phi = \phi_1 + \phi_2 + \phi_3$, where ϕ_1, ϕ_2, and ϕ_3 are solutions of the 1-D, 2-D, and 3-D sub-problem, respectively. The 1-D solution ϕ_1 can be expressed as

$$\phi_1(z) = -\frac{qN_a}{2\varepsilon_{si}}z^2 + az + b, \quad (3a)$$

$$a = \frac{(V_{tg} - V_{fb}) - (V_{ug} - V_{fb}) + \frac{qN_a}{2\varepsilon_{si}}\left(H_{fin}{}^2 + 2\cdot\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,t}H_{fin}\right)}{H_{fin} + \frac{\varepsilon_{si}}{\varepsilon_i}t_{i,t} + \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox,u}}, \quad (3b)$$

$$b = \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox,u}a + (V_{ug} - V_{fb}). \quad (3c)$$

In solving the 2-D and 3-D sub-problems, approximation was made to avoid the numerical iteration required in finding the eigenvalues[5] and to simplify the solution form. The boundary conditions [eqs. (2a)–(2d)] are simplified by converting the gate dielectric thickness to $(\varepsilon_{si}/\varepsilon_i)$ times and replacing the gate dielectric region with an equivalent Si region.[6] The electric field discontinuity across the gate dielectric and Si-fin interface can thus be eliminated. In other words, the Si-fin body and the gate dielectric region are treated as a homogeneous silicon cuboid with an effective width W_{eff} and an effective height H_{eff} given by eqs. (4) and (5), respectively.

$$W_{eff} = W_{fin} + \frac{\varepsilon_{si}}{\varepsilon_i}(t_{i,f} + t_{i,b}), \quad (4)$$

$$H_{eff} = H_{fin} + \frac{\varepsilon_{si}}{\varepsilon_i}t_{i,t} + t_{ox,u}. \quad (5)$$

The 2-D solution ϕ_2 can be obtained using the method of separation of variables:

$$\phi_2(x,z) = \sum_{i=1}^{\infty}\left[c_i\sinh\left(\frac{i\pi}{H_{eff}}\left(x + \frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)\right) + c_i'\sinh\left(\frac{i\pi}{H_{eff}}\left(W_{eff} - \left(x + \frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)\right)\right)\right]\cdot\sin\left(\frac{i\pi}{H_{eff}}(z + t_{ox,u})\right), \quad (6a)$$

where

$$c_i = \frac{1}{\sinh\left(i\pi\frac{W_{eff}}{H_{eff}}\right)}\left[2(V_{fg} - V_{fb} - b)\frac{1-(-1)^i}{i\pi} + 2a\left(\frac{t_{ox,u}}{i\pi} + \frac{(H_{eff} - t_{ox,u})(-1)^i}{i\pi}\right)\right.$$
$$\left. + \frac{qN_a}{\varepsilon_{si}}\left(\frac{(t_{ox,u})^2}{i\pi} - \frac{(H_{eff} - t_{ox,u})^2(-1)^i}{i\pi} + 2H_{eff}{}^2\frac{(-1)^i - 1}{(i\pi)^3}\right)\right], \quad (6b)$$

$$c_i' = \frac{1}{\sinh\left(i\pi\frac{W_{eff}}{H_{eff}}\right)}\left[2(V_{bg} - V_{fb} - b)\frac{1-(-1)^i}{i\pi} + 2a\left(\frac{t_{ox,u}}{i\pi} + \frac{(H_{eff} - t_{ox,u})(-1)^i}{i\pi}\right)\right.$$
$$\left. + \frac{qN_a}{\varepsilon_{si}}\left(\frac{(t_{ox,u})^2}{i\pi} - \frac{(H_{eff} - t_{ox,u})^2(-1)^i}{i\pi} + 2H_{eff}{}^2\frac{(-1)^i - 1}{(i\pi)^3}\right)\right]. \quad (6c)$$

Similarly, the 3-D solution ϕ_3 can also be obtained and expressed as

$$\phi_3(x,y,z) = \sum_{m=1}^{\infty}\sum_{n=1}^{\infty}[e_{m,n}\sinh(k_y y) + e_{m,n}'\sinh(k_y(L_{eff} - y))]\sin\left(\frac{m\pi}{W_{eff}}\left(x + \frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)\right)\sin\left(\frac{n\pi}{H_{eff}}(z + t_{ox,u})\right), \quad (7a)$$

where

$$k_y = \sqrt{\left(\frac{m\pi}{W_{\text{eff}}}\right)^2 + \left(\frac{n\pi}{H_{\text{eff}}}\right)^2}, \tag{7b}$$

$$e_{m,n} = \frac{1}{\sin(k_y L_{\text{eff}})}\left\{\left[(-\phi_{\text{ms}} + V_{\text{DS}} - b)\frac{1-(-1)^m}{m\pi} + \frac{qN_{\text{a}}}{2\varepsilon_{\text{si}}}\left(-\frac{\left(W_{\text{eff}} - \frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{i}}}t_{\text{i,b}}\right)^2(-1)^m - \left(\frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{i}}}t_{\text{i,b}}\right)^2}{m\pi} + \frac{2{W_{\text{eff}}}^2((-1)^m - 1)}{(m\pi)^3}\right)\right.\right.$$
$$\left.\left. + a\left(\frac{\left(W_{\text{eff}} - \frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{i}}}t_{\text{i,b}}\right)(-1)^m + \frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{i}}}t_{\text{i,b}}}{m\pi}\right)\right] \cdot \frac{4\cdot(1-(-1)^n)}{n\pi} + 2c_m\frac{\frac{(-1)^n}{n\pi}\sinh\left(m\pi\frac{H_{\text{eff}}}{W_{\text{eff}}}\right)}{1+\left(\frac{m}{n}\frac{H_{\text{eff}}}{W_{\text{eff}}}\right)^2} - 2c'_m\frac{\frac{1}{n\pi}\sinh\left(m\pi\frac{H_{\text{eff}}}{W_{\text{eff}}}\right)}{1+\left(\frac{m}{n}\frac{H_{\text{eff}}}{W_{\text{eff}}}\right)^2}\right\}, \tag{7c}$$

$$e'_{m,n} = \frac{1}{\sin(k_y L_{\text{eff}})}\left\{\left[(-\phi_{\text{ms}} - b)\frac{1-(-1)^m}{m\pi} + \frac{qN_{\text{a}}}{2\varepsilon_{\text{si}}}\left(-\frac{\left(W_{\text{eff}} - \frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{i}}}t_{\text{i,b}}\right)^2(-1)^m - \left(\frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{i}}}t_{\text{i,b}}\right)^2}{m\pi} + \frac{2{W_{\text{eff}}}^2((-1)^m - 1)}{(m\pi)^3}\right)\right.\right.$$
$$\left.\left. + a\left(\frac{\left(W_{\text{eff}} - \frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{i}}}t_{\text{i,b}}\right)(-1)^m + \frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{i}}}t_{\text{i,b}}}{m\pi}\right)\right] \cdot \frac{4\cdot(1-(-1)^n)}{n\pi} + 2c_m\frac{\frac{(-1)^n}{n\pi}\sinh\left(m\pi\frac{H_{\text{eff}}}{W_{\text{eff}}}\right)}{1+\left(\frac{m}{n}\frac{H_{\text{eff}}}{W_{\text{eff}}}\right)^2} - 2c'_m\frac{\frac{1}{n\pi}\sinh\left(m\pi\frac{H_{\text{eff}}}{W_{\text{eff}}}\right)}{1+\left(\frac{m}{n}\frac{H_{\text{eff}}}{W_{\text{eff}}}\right)^2}\right\}. \tag{7d}$$

Our potential solution has been verified by 3-D device simulation.[7] Figures 2(a) and 2(b) compare the derived channel potential distribution with device simulation for heavily doped and lightly doped devices, respectively. Note that a smaller equivalent oxide thickness (EOT) is used in the lightly-doped case to sustain the electrostatic integrity.[3] It can be seen that our model shows satisfactory accuracy.

After deriving the channel potential solution, the subthreshold current can be calculated by[8]

$$I_{\text{DS}} = q\mu\frac{{n_{\text{i}}}^2}{N_{\text{a}}}\frac{kT}{q}\cdot\left[1-\exp\left(-\frac{qV_{\text{DS}}}{kT}\right)\right]\cdot\frac{1}{L_{\text{eff}}}\cdot\int_0^{H_{\text{fin}}}\int_0^{W_{\text{fin}}}\exp\left[\frac{q\phi(x,y_{\min},z)}{kT}\right]dx\,dz \tag{8}$$

where $\phi(x, y_{\min}, z)$ is the minimum potential (i.e., the highest barrier for carrier flow) along the y (channel length) direction.[9] For devices biased in the linear region, the minimum potential occurs at $y_{\min} = L_{\text{eff}}/2$ because of the nearly symmetrical potential distribution along the channel. We define the V_{th} as the gate voltage at which the calculated subthreshold current $I_{\text{DS}} = 300nA \times W_{\text{total}}/L_{\text{eff}}$,[10] where $W_{\text{total}} = 2H_{\text{fin}} + W_{\text{fin}}$ is the total width of the multi-gate device.

Compared with the computer-aided-design for semiconductor manufacturing technology (TCAD) device simulation, our methodology shows higher efficiency in determining the V_{th} of a multi-gate device. The central processing unit (CPU) time needed for a single V_{th} using TCAD simulation is about tens of minutes, while in our calculation only several seconds is needed. More importantly, this theoretical framework provides more scalable and predictive results than experimental or TCAD simulation does.

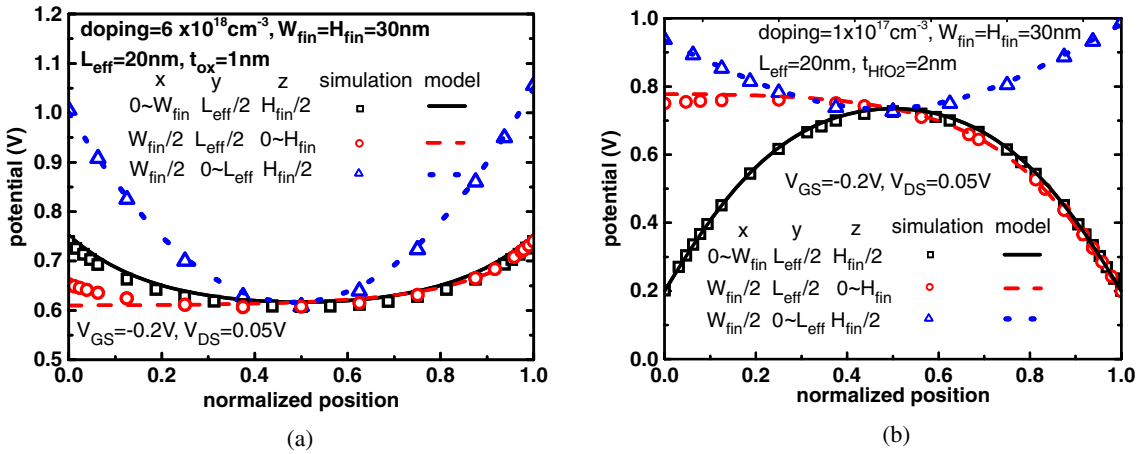

Fig. 2. (Color online) Analytical potential distribution compared with the result of 3-D device simulation. For the lightly doped case, a midgap workfunction is used (4.7 eV).

3. V_{th} Dispersion Caused by Random Dopant Fluctuation

We have derived the 3-D analytical potential solution for multi-gate MOSFETs with uniformly doped channel. Although the actual 3-D charge distribution is not uniform, we can incorporate the dopant number fluctuation in our theoretical framework to assess the feasibility of various multi-gate device designs. The dopant number in the channel has been found to follow Poisson distribution[13] and the V_{th} distribution caused by random dopant fluctuation can be approximated as Gaussian distribution.[13–15] With MOSFET scaling, the V_{th} distribution gradually changes its shape from the Gaussian to a Poisson-like distribution.[15] To assess the V_{th} variation of multi-gate devices caused by dopant number fluctuation, in this work, we assume that the dopant number in the channel follows Poisson distribution[11,15] and the standard deviation (σ) of the dopant number is $n_a^{1/2}$, where n_a is the average dopant number in the Si-body. The V_{th} variation for dopant number fluctuation can then be calculated as $\Delta V_{th} = |V_{th}(+3\sigma) - V_{th}(-3\sigma)|/2$.

To compare the multi-gate devices with various aspect ratio (AR $= H_{fin}/W_{fin}$), we focus on the FinFET (AR $= 2$), tri-gate (AR $= 1$), and quasi-planar (AR $= 0.5$) structures (Fig. 3). The total width ($W_{total} = 2H_{fin} + W_{fin}$) of various AR devices are all equal to 75 nm to make fair comparison. Besides heavily doped devices, we also examined the impact of random dopant fluctuation on the V_{th} dispersion of lightly doped devices. For heavily doped devices, the channel doping is equal to $6 \times 10^{18}\,cm^{-3}$. For lightly doped channel the channel doping is $1 \times 10^{17}\,cm^{-3}$. Note that gate oxide ($t_{ox} = 1$ nm) is used for heavily doped devices, while high-k dielectric ($t_{HfO_2} = 2$ nm and the dielectric constant of HfO_2 is 25) is used for lightly doped ones to sustain the device electrostatics.[3]

Figure 4 shows the AR dependence of ΔV_{th} caused by random dopant fluctuation, and the results are verified with device simulation.[7] For heavily doped channel, the ΔV_{th} increases with AR, and the minimum ΔV_{th} occurs at AR $= 0.5$, i.e., quasi-planar device. This is because for a given total width, the devices with AR $= 0.5$ possess the largest channel volume (Fig. 5). Since

$$\Delta V_{th} = \frac{dV_{th}}{dN_a} \cdot \Delta N_a, \tag{9}$$

$$\Delta N_a = \frac{\Delta n_a}{V} \propto \frac{\sqrt{n_a}}{V} = \frac{\sqrt{N_a \cdot V}}{V} = \frac{\sqrt{N_a}}{\sqrt{V}}, \tag{10}$$

where V is the channel volume, the devices with larger channel volume show smaller ΔV_{th}. In addition to channel volume, eq. (9) demonstrates that the V_{th} sensitivity to the channel doping (dV_{th}/dN_a) may also determine the ΔV_{th}. Figure 6 shows the channel doping dependence of V_{th} for devices with heavily doped channel. It can be seen that FinFET, tri-gate and quasi-planar devices show similar V_{th} sensitivity. Therefore, for heavily doped channel, quasi-planar device shows better immunity to random dopant fluctuation than FinFET and tri-gate because of its larger channel volume.

Figure 7 shows that for lightly doped channel, the ΔV_{th} increases as AR decreases. This is because for lightly doped channel, devices with different AR show different V_{th} sensitivity to channel doping (Fig. 8). For lightly doped channel, FinFET shows the smallest V_{th} sensitivity to channel doping because of its narrower W_{fin} for a given total width. In other words, W_{fin} scaling enhances the gate control and reduces the V_{th} dependence on the channel doping. Therefore, FinFET shows the best immunity to dopant fluctuation for lightly doped channel.

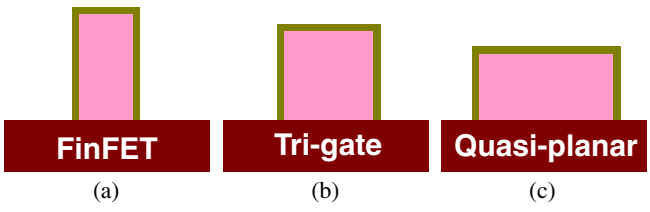

Fig. 3. (Color online) Illustration of three different AR devices for a given total width: (a) FinFET (AR = 2), (b) tri-gate (AR = 1), and (c) quasi-planar device (AR = 0.5).

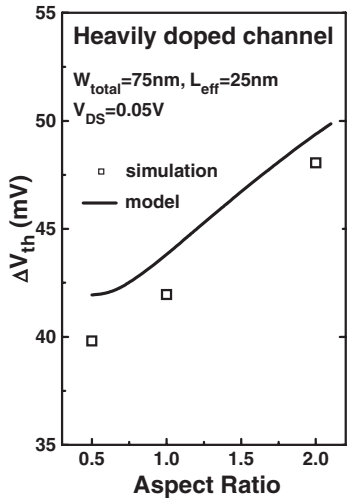

Fig. 4. The AR dependence of ΔV_{th} caused by random dopant fluctuation in the heavily doped channel.

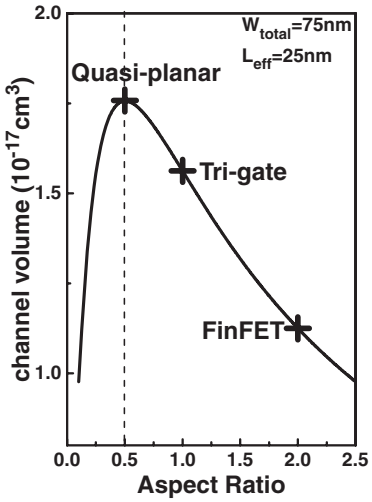

Fig. 5. For a given total width, devices with AR = 0.5 possess the largest channel volume. Devices with larger volume will show less doping variation caused by random dopant fluctuation.

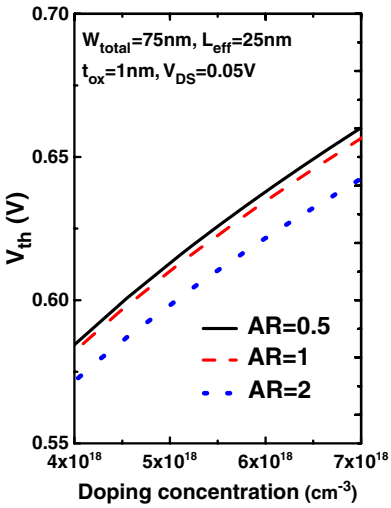

Fig. 6. (Color online) Model prediction of the doping dependence of V_{th} for heavily doped channel with the same total width.

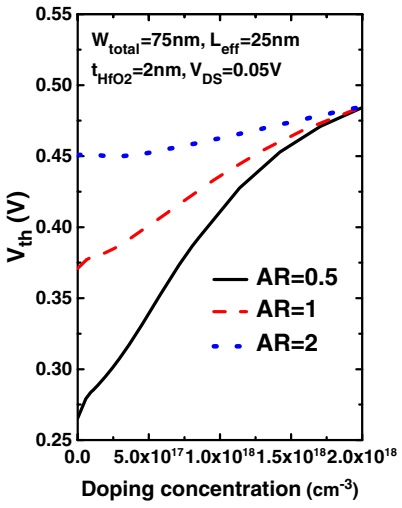

Fig. 8. (Color online) Model prediction of the doping dependence of V_{th} for lightly doped channel with the same total width.

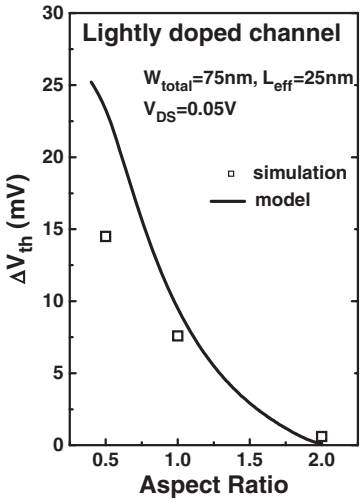

Fig. 7. The AR dependence of ΔV_{th} caused by dopant number fluctuation in the lightly doped channel.

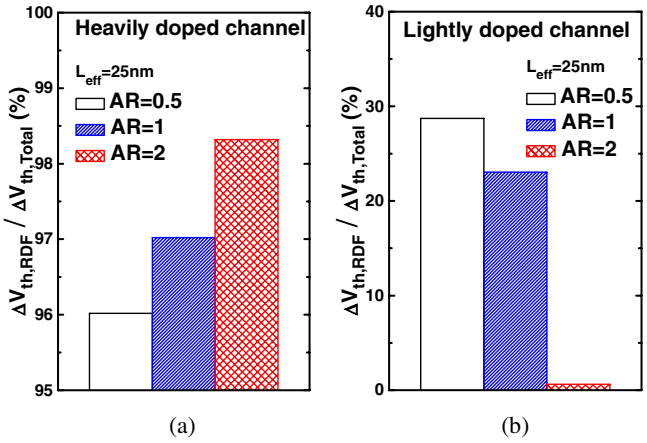

Fig. 9. (Color online) The proportional of the ΔV_{th} caused by dopant number fluctuation to the overall ΔV_{th} for (a) heavily doped channel and (b) lightly doped channel.

To assess the impact of random dopant fluctuation on the overall V_{th} variation, we have calculated the proportion of V_{th} dispersion due to random dopant fluctuation to the overall V_{th} variation (Fig. 9). The ΔV_{th} caused by L_{eff} variation ($\Delta V_{th,L_{eff}}$), W_{fin} variation ($\Delta V_{th,W_{fin}}$), H_{fin} variation ($\Delta V_{th,H_{fin}}$) and random dopant fluctuation ($\Delta V_{th,RDF}$) are considered in our calculation. We assume that the 3σ process variations of these device parameters are $\pm 10\%$ of their nominal values, and the V_{th} variation is defined as $\Delta V_{th} = |V_{th}(+10\%) - V_{th}(-10\%)|/2$.[11] The overall V_{th} variation is defined as $\Delta V_{th}^2 = \Delta V_{th,L_{eff}}^2 + \Delta V_{th,W_{fin}}^2 + \Delta V_{th,H_{fin}}^2 + \Delta V_{th,RDF}^2$. Figure 9(a) shows that for heavily doped channel, random dopant fluctuation dominates the overall V_{th} dispersion and the quasi-planar device shows better immunity than devices with other aspect ratio to dopant fluctuation. Our theoretical result is consistent with the experimental data from Thean *et al.*,[4] who showed that for doped channel, the σV_{th} of the devices with smaller volume is larger than that of the devices with larger volume. Although lightly doped channel has been suggested[12] to suppress the V_{th} variation caused by dopant fluctuation, Fig. 9(b) shows that the V_{th} variation caused by dopant fluctuation is still significant for lightly-doped tri-gate and quasi-Planar devices. The impact of random dopant fluctuation may still be an issue to the V_{th} dispersion of lightly doped channel unless devices with good electrostatic integrity such as FinFET are used.

4. Conclusions

We have investigated the V_{th} dispersion caused by random dopant fluctuation of multi-gate MOSFETs using analytical solutions of 3-D Poisson's equation verified with device simulation. Especially, we analyze the impact of aspect ratio on the dopant fluctuation in multi-gate devices. With a given total width, lightly doped FinFET shows the smallest V_{th} dispersion because of its smaller V_{th} sensitivity to the channel doping. For heavily doped channel, quasi-planar device shows smaller V_{th} dispersion because of its larger channel volume. The V_{th} dispersion due to random dopant fluctuation may still be significant in the lightly doped channel, especially for tri-gate and quasi-planar devices.

Acknowledgements

This work was supported in part by the National Science Council of Taiwan under contract NSC95-2221-E-009-327-MY2, the Ministry of Education in Taiwan under ATU Program, and Taiwan Semiconductor Manufacturing Company.

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