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Investigations on highly stable thermal characteristics of a dilute $In_{0.2}Ga_{0.8}AsSb/GaAs$ doped-channel field-effect transistor

Ke-Hua Su[1,2], Wei-Chou Hsu[1,2], Ching-Sung Lee[3], Po-Jung Hu[1,2], Yue-Han Wu[4], Li Chang[4], Ru-Shang Hsiao[5], Jenn-Fang Chen[5] and Tung-Wei Chi[6]

[1] Institute of Microelectronics, Department of Electrical Engineering, National Cheng-Kung University, 1 University Road, Tainan, Taiwan 70101, Republic of China
[2] Advanced Optoelectronic Technology Center, National Cheng Kung University, 1 University Road, Tainan, Taiwan 70101, Republic of China
[3] Department of Electronic Engineering, Feng Chia University, 100 Wenhwa Road, Taichung, Taiwan, Republic of China
[4] Department of Materials and Engineering, National Chiao-Tung University, Hsinchu, Taiwan, Republic of China
[5] Department of Eletrophysics, National Chiao Tung University, Hsinchu 300, Taiwan, Republic of China
[6] Industrial Technology Research Institute, Hsinchu, Taiwan, Republic of China

E-mail: wchsu@eembox.ncku.edu.tw

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Abstract

This work reports for the first time a novel $In_{0.2}Ga_{0.8}AsSb/GaAs$ heterostructure doped-channel field-effect transistor (DCFET) grown by the molecular beam epitaxy system. The interfacial quality within the InGaAsSb/GaAs quantum well of the DCFET device has been effectively improved by introducing surfactant-like Sb atoms during the growth of the Si-doped InGaAs channel layer. The improved device characteristics include the peak extrinsic transconductance ($g_{m,\,max}$) of 161.5 mS mm^{-1}, the peak drain–source saturation current density ($I_{DSS,\,max}$) of 230 mA mm^{-1}, the gate–voltage swing (GVS) of 1.65 V, the cutoff frequency (f_T) of 12.5 GHz and the maximum oscillation frequency (f_{max}) of 25 GHz at 300 K with the gate dimensions of 1.2 × 200 μm^2. The proposed design has also shown a stable thermal threshold coefficient ($\partial V_{th}/\partial T$) of −0.7 mV K^{-1}.

1. Introduction

Dilute nitride [1] quaternary compounds $In_xGa_{1-x}As_{1-y}N_y$ have been intensively studied because of their lower bandgap characteristics in the past few years [2, 3]. The InGaAsN/GaAs heterostructures possess the advantages of long wavelength characteristics due to their narrower bandgap properties. The incorporation of nitrogen atoms into the InGaAs layer can effectively decrease its bandgap energy. Yet it usually results in a poor crystalline quality and degraded carrier transport property [4, 5] for the electronic device applications. To improve the crystal and optical properties, a thermal annealing process has been adopted in an attempt to remove the interfacial defects and the nonradiative impurities [6–8]. Recently, some efforts [9–13] have been devoted to using Sb atoms as surfactants in the GaAs/InGaAsNSb quantum well (QW) laser to improve the crystal quality. The advantages of incorporating Sb atoms into the optoelectronic devices and electronic devices can not only improve the threshold current densities [9–14], but also effectively reduce the energy bandgap [15] and red shift the light emission. Therefore, this paper presents for the first time a doped-channel field-effect transistor (DCFET) device using the dilute $In_{0.2}Ga_{0.8}AsSb$ antimony-doped-channel design grown

Table 1. Comparisons of electron mobility and concentration characteristics.

Reference	This work	[16]	[17]	[18]
Channel materials	$In_{0.2}Ga_{0.8}AsSb$	$In_{0.15}Ga_{0.7}As$ $In_{0.2}Ga_{0.8}As$ $In_{0.25}Ga_{0.75}As$	$In_{0.2}Ga_{0.8}As$	$In_{0.15}Ga_{0.7}As$ LR-DCFET DCFET
μ ($cm^2\ V^{-1}\ s^{-1}$)	2674	1565 1810 1180	2200	1250 1152
n_s ($\times 10^{12}\ cm^{-2}$)	3.82	5.01 7.97 6.52	4.5	5.7 5.1
$\mu \times n_s$ ($\times 10^{16}\ V^{-1}\ s^{-1}$)	1.021	0.784 1.442 0.769	0.99	0.713 0.587

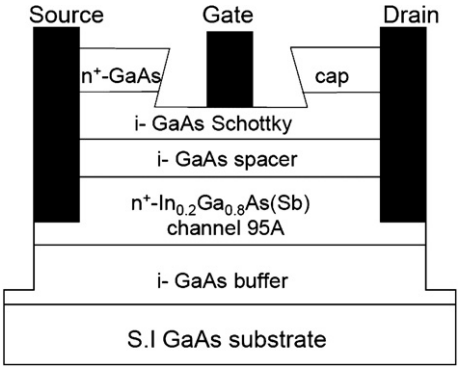

Figure 1. The device cross-section of the proposed $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET.

by the molecular beam epitaxy (MBE) system to improve the interfacial quality, device characteristics and thermal stability at the same time.

2. Material growth and device fabrication

The epitaxial structure of the $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET was grown by the solid-source MBE (SSMBE) system. Arsenic and antimony in separate thermal cracked cells were used as the group-V sources for growing the InGaAsSb layer. The flux rate of As was maintained constantly at about 1×10^{-6} Torr during the entire growth procedure, and only the ratio of In to Ga was adjusted. An excess Sb flux of 1.5×10^{-7} Torr, measured by the high vacuum gauge, was introduced during the growth of the InGaAs channel by setting the cracked cell temperature at 530 °C for the Sb valve. The growth temperatures for the InGaAsSb and GaAs layers were set around 510 °C and 600 °C, respectively.

Figure 1 shows the device cross section of the proposed $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET. The epitaxial structure consists of a 0.4 μm GaAs buffer layer on a (1 0 0)-oriented semi-insulating GaAs substrate, sequentially followed by a 9.5 nm thick Si-doped $In_{0.2}Ga_{0.8}AsSb$ channel (5×10^{18} cm^{-3}), a 4 nm undoped GaAs spacer layer, a 35 nm undoped GaAs Schottky layer and finally a 20 nm Si-doped (7×10^{18} cm^{-3}) GaAs cap layer. Hall measurements were carried out on the proposed $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET to characterize the two-dimensional electron gas concentration (n_{2DEG}) and electron mobility (μ_n) under a magnetic field of 5000 G. The values of μ_n and the corresponding n_{2DEG} were 2674 $cm^2\ V^{-1}\ s^{-1}$ and 3.82×10^{12} cm^{-2} at 300 K, respectively. The proposed design in this work has demonstrated superior transport properties with comparable 2DEG concentrations and InGaAs channel compositions as compared to other DCFET reports [16–18], as shown in table 1. The improved transport properties are mainly due to the Sb incorporation in the InGaAs-doped channel, which will be discussed later. Standard photolithography, lift-off and the rapid thermal annealing (RTA) techniques were employed for the device fabrication. The mesa etching process was performed down to the buffer layer to reduce the gate leakages current. The $H_3PO_4/H_2O_2/H_2O$ solution was used as the wet-etching solution for the GaAs cap layer. AuGeNi alloys were used for the source/drain ohmic contacts, onto which Au was evaporated to reduce the contact resistance. Au was deposited on the undoped GaAs Schottky layer as the gate electrode. The gate dimensions were 1.2×200 μm^2 with the drain-to-source spacing of 7 μm.

3. Experimental results and discussions

Figure 2 shows the secondary ion mass spectrometry (SIMS) intensity as a function of the depth of the $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET. The $In_{0.2}Ga_{0.8}AsSb$ dilute channel is inserted about 59 nm below the wafer surface. The SIMS measurement profile also indicates the stable compositions of both Ga and As during the sample growth. On the other hand, the In, Si and Sb ion compositions were increased to their maximum at about 60 nm depth. The SIMS profiles have demonstrated the successful incorporations of the Sb and Si atoms within the channel growth. The Sb atoms reacted like surfactants to be slightly incorporated into the InGaAs film to improve the crystalline quality.

Though the academic studies of having successfully applied Sb incorporation to laser devices [9–13], improved the crystalline quality [14] or effectively reduced the energy gap [15] have already been cited and discussed in section 1, we have further performed the Shubnikov–de Hass (SdH) measurement on simple InGaAs/GaAs QW

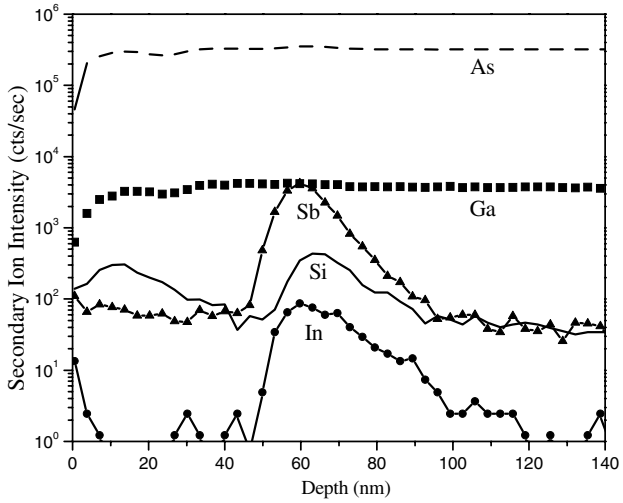

Figure 2. SIMS measurement profiles.

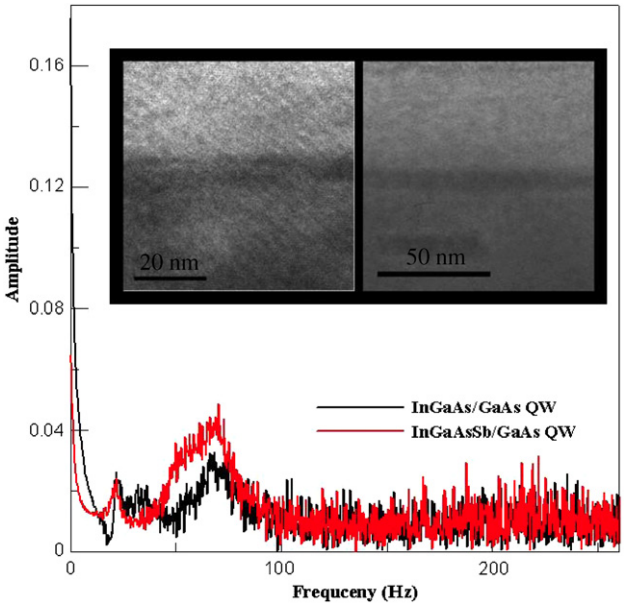

Figure 3. SdH measurement results for the InGaAsSb/GaAs and InGaAs/GaAs QWs. The inset shows the TEM photos of the studied $In_{0.2}Ga_{0.8}AsSb$/GaAs DCFET.

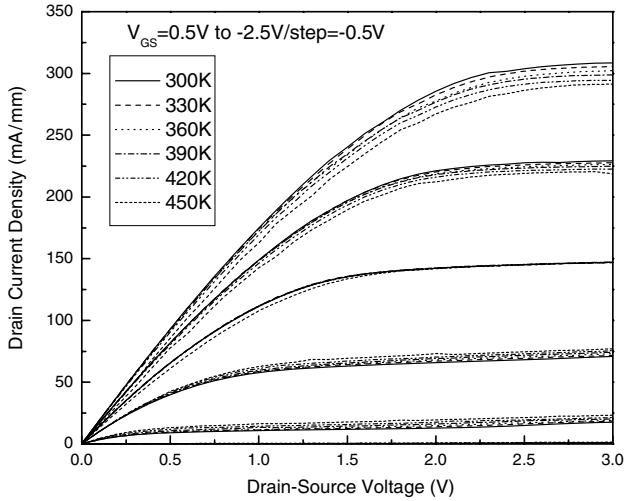

Figure 4. The current–voltage characteristics of the $In_{0.2}Ga_{0.8}AsSb$/GaAs DCFET at elevated temperatures.

samples with/without the Sb incorporation. SdH is a powerful tool to give detailed information about the sub-band occupancies and carrier transport property in the 2DEG system. The SdH measurement results, as in figure 3, clearly show that two frequencies were observed. It indicates that two different sub-bands have been occupied in both the InGaAsSb/GaAs and InGaAs/GaAs QWs. The first peak frequencies of the two samples are not distinct from each other, since the lowest sub-bands in both samples have been occupied by the 2DEG population. However, the second peak frequency of the InGaAsSb/GaAs QW is higher than that of the InGaAs/GaAs structure, indicating its increased 2DEG concentrations in the second sub-band by incorporating the Sb atoms in the InGaAs channel. In addition to the Hall characterization results, as discussed before, the SdH comparisons further verify the enhanced 2DEG confinement capability by incorporating Sb atoms into the InGaAs channel of this work. The inset of figure 3 shows the TEM pictures for the proposed $In_{0.2}Ga_{0.8}AsSb$/GaAs DCFET. The $In_{0.2}Ga_{0.8}AsSb$/GaAs heterointerfaces were observed to be more flat and uniform than those in the conventional InGaAs/GaAs sample [19]. The TEM photos and SdH characterizations have clearly verified the improved crystalline quality and enhanced electron confinement capability after the incorporation of surfactant-like Sb atoms into the InGaAs channel.

Figure 4 shows the typical current–voltage characteristics of the $In_{0.2}Ga_{0.8}AsSb$/GaAs DCFET from 300 K to 450 K. Good pinch-off characteristics at different temperatures have been observed. It is mainly attributed to the increased barrier heights of the conduction-band discontinuities (ΔE_C) within the devised $In_{0.2}Ga_{0.8}AsSb$/GaAs interfaces to effectively reduce the electron injections at decreased gate biases. Consequently, decreased substrate leakages and improved pinch-off properties at high electric fields have been achieved.

Figure 5 shows the g_m and I_{DSS} characteristics with respect to the gate-to-source bias (V_{GS}) at elevated temperatures. The observed $g_{m,\,max}$ and peak I_{DSS} values were found to be 161.5 (142) mS mm^{-1} and 230 (220) mA mm^{-1} respectively at 300 (450) K. The studied device also demonstrates improved current-driving capability (I_{DSS}) and maximum room-temperature extrinsic transconductance ($g_{m,\,max}$) as compared with other works [14, 20–23], as shown in table 2. Define the gate–voltage swing (GVS) value as the available gate bias range at a 10% drop from the $g_{m,\,max}$ value. The GVS characteristics of the proposed device are superiorly high to be 1.65 (1.71) V at 300 (450) K, which is higher than that of the uniform channel HFET (1.45 V) [21]. Though the GVS value of this work is lower than that of the V-shape channel HFET (1.75 V) [21], yet the V-shaped graded-channel structure [21] can also be used in the

Table 2. Comparisons of I_{DSS}, $g_{m,max}$ and thermal threshold coefficient ($\partial V_{th}/\partial T$) characteristics.

References	Material	I_{DSS} (mA mm^{-1})	$g_{m,max}$ (mS mm^{-1})	$\partial V_{th}/\partial T$ (mV K^{-1})
This work	GaAs/InGaAsSb DCFET	230	161.5	−0.7
[14]	GaAs/InGaAsNSb HEMT	87.5	109	−0.807
[20]	AlGaAs/InGaAsN			
	As-grown HEMT	220	56	–
	RTA 700 °C HEMT	290	64	–
[21]	AlGaAs/InGaAs			
	Uniform channel HFET	112	102	−1
	V-shape channel HFET	201	112	−0.82
[22]	InGaP/InGaAs PDDCHFET	100	162.2	−1.81
[23]	InGaP/InGaAs HFETs			
	Device A	390	208	−1.139
	Device B	400	158	−1.418

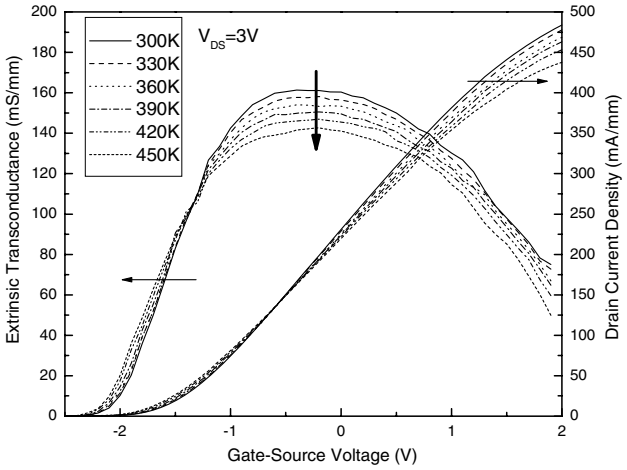

Figure 5. g_m and I_{DSS} characteristics with respect to V_{GS} at elevated temperatures.

proposed $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET to further improve the GVS linearity property.

Figure 6 shows the two-terminal gate–drain *I–V* characteristics of the $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET at different temperatures. The reverse gate–drain breakdown voltage (BV_{GD}) is defined to be the gate-to-drain voltages, at which the gate current density reaches 1 mA mm^{-1}. The measured BV_{GD} values are −14.6 V, −14.8 V, −14.9 V, −14.8 V, −14.4 V and −13.9 V at 300 K, 330 K, 360 K, 390 K, 420 K and 450 K, respectively. It is noted that the breakdown voltage increases with the temperature from 300 K to 360 K, as shown in figure 6(*a*). This is mainly attributed to the degraded transport characteristics and the decreased gate current density by the enhanced scattering mechanism at elevated temperatures. However, the breakdown voltages were observed to decrease from 360 K to 450 K, as shown in figure 6(*b*). An interesting polarity change is mainly due to the switching of the dominant mechanism from the previously described scattering mechanism to

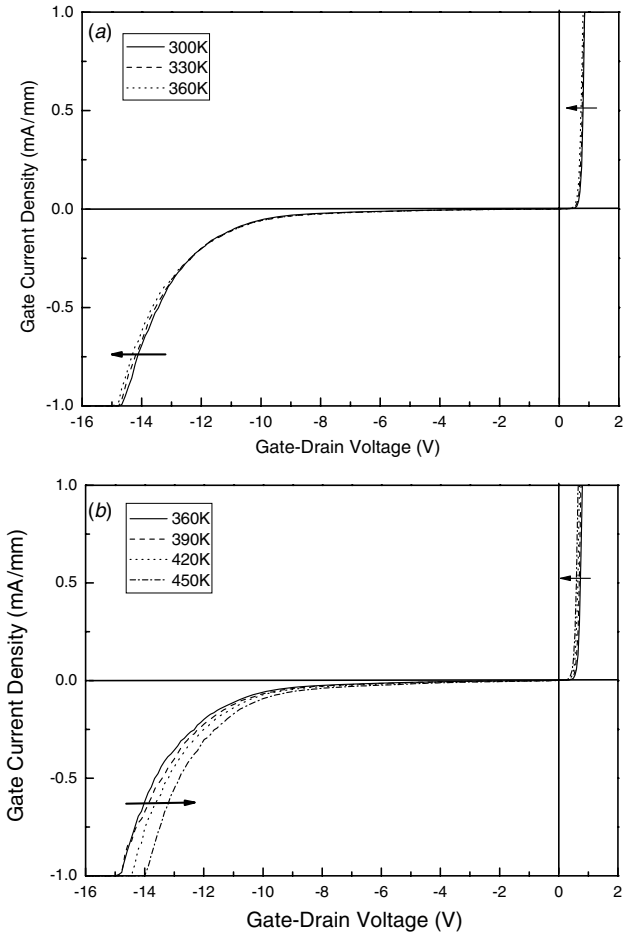

Figure 6. (*a*) Two-terminal gate-to-drain breakdown characteristics from 300 K to 360 K. (*b*) Two-terminal gate-to-drain breakdown characteristics from 360 K to 450 K.

the combinational effects of the enhanced barrier-lowering phenomenon, the enhanced tunneling mechanism and the decreased bandgap above 360 K. Consequently, the electron

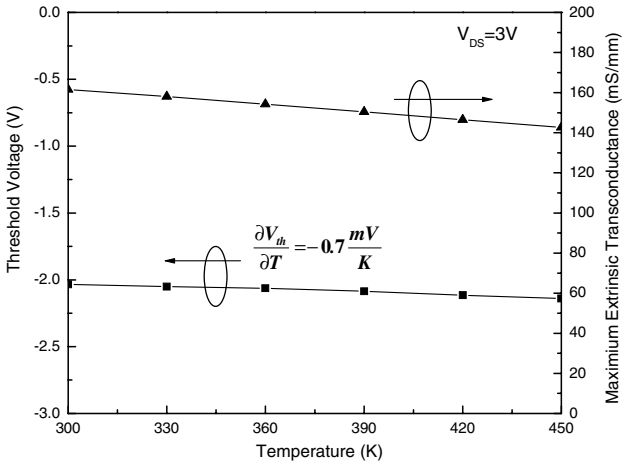

Figure 7. Maximum extrinsic transconductance and threshold characteristics versus temperature, at $V_{DS} = 3$ V.

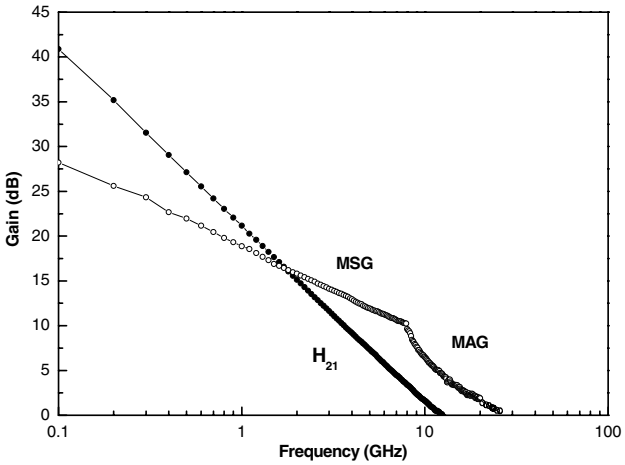

Figure 8. High-frequency characteristics at 300 K, with $V_{DS} = 3.5$ V and $V_{GS} = -1.5$ V.

injection was increased to deteriorate the breakdown characteristics at higher temperatures.

Figure 7 shows the temperature-dependent characteristics of $g_{m,\max}$ and the threshold voltage (V_{th}) from 300 to 450 K at $V_{DS} = 3$ V. The values of V_{th} are -2.034 V, -2.052 V, -2.062 V, -2.085 V, -2.116 V and -2.139 V at 300 K, 330 K, 360 K, 390 K, 420 K and 450 K, respectively. The threshold shift (ΔV_{th}) from 300 K to 450 K is only 0.105 V, with a superior thermal threshold coefficient ($\partial V_{th}/\partial T$) of -0.7 mV K^{-1}. The studied device has also demonstrated improved thermal threshold stability as compared to other HFETs [14, 21–23], as also listed in table 2. Superior thermal threshold stability is mainly due to the improved channel confinement capability in the $In_{0.2}Ga_{0.8}AsSb/GaAs$ QW structure with devised high discontinuity barriers. The microwave characteristics of the studied devices were characterized by using an HP 8510B vector network analyzer in conjunction with the cascaded probes over the range from 0.5 GHz to 20 GHz, as shown in figure 8. f_T and f_{max} were determined to be 12.5 GHz and 25 GHz, respectively, at 300 K with $V_{DS} = 3.5$ V and $V_{GS} = -1.5$ V for the proposed $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET.

4. Conclusion

A novel $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET with a dilute antimony-doped channel has been successfully investigated for the first time. By incorporating the surfactant-like Sb atoms into the InGaAs channel, the proposed design can effectively improve the crystalline quality of the InGaAsSb/GaAs heterointerface and the electron transport properties. In addition, the decreased energy bandgap of the dilute antimony-doped $In_{0.2}Ga_{0.8}AsSb$ channel can further improve the carrier transport properties and the channel confinement capability at the same time. Various characterization techniques, including the SIMS spectrometer and the TEM photography, have been performed to verify the improved crystalline property. Consequently, superior device performances of high linearity, high gain and improved thermal stability have all been successfully achieved in the proposed $In_{0.2}Ga_{0.8}AsSb/GaAs$ DCFET.

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References

[1] Choulis S A, Hosea T J C, Ghosh S, Klar P J and Hofmann M 2003 *IEEE Photonics Technol. Lett.* **15** 1026
[2] Shan W, Walukiewicz W, Ager J W III, Haller E E, Geisz J F, Friedman D J, Olson J M and Kurtz S R 1999 *Phys. Rev. Lett.* **82** 1121
[3] Kim K and Zunger A 2001 *Phys. Rev. Lett.* **86** 2609
[4] Ptak A J, Johnston S W, Kurtz S, Friedman D J and Metzger W K 2003 *J. Cryst. Growth* **251** 392
[5] Geisz J F, Friedman D J, Olson J M, Kurtz S R and Keyes B M 1998 *J. Cryst. Growth* **195** 401
[6] Wang J S, Kovsh A R, Hsiao R S, Chen L P, Chen J F, Lay T S and Chi J Y 2004 *J. Cryst. Growth* **262** 84
[7] Kovsh A R, Wang J S, Wei L, Shiao R S, Chi J Y and Volovik B V 2002 *J. Vac. Sci. Technol.* B **20** 1158
[8] Hsiao R S *et al* 2004 *Japan J. Appl. Phys.* **43** L1555
[9] Shimizu H, Kumada K, Uchiyama S and Kasukawa A 2000 *Electron. Lett.* **36** 1379
[10] Yang X, Jurkovic M J, Heroux J B and Wang W I 1999 *Electron. Lett.* **35** 1082
[11] Yang X, Jurkovic M J, Heroux J B and Wang W I 1999 *Appl. Phys. Lett.* **75** 178
[12] Yang X, Heroux J B, Mei L F and Wang W I 2001 *Appl. Phys. Lett.* **78** 4068
[13] Ha W, Gambin V, Wistey M, Bank S, Yuen H, Kim S and Harris J S 2002 *Electron. Lett.* **38** 277
[14] Su K H, Hsu W C, Lee C S, Hu P J, Hsiao R S, Chen J F and Chi T W 2007 *Japan J. Appl. Phys.* **46** 2344
[15] Shimizu H, Kumada K, Uchiyama S and Kasukawa A 2001 *IEEE J. Sel. Top. Quantum Electron.* **7** 355
[16] Chan Y J and Yang M T 1995 *IEEE Trans. Electron Devices* **42** 1745
[17] Lour W S, Liu W C, Tasi J H, Laih L W and Chen H R 1996 *Superlattices Microstruct.* **20** 15

[18] Chiu H C, Chien F T, Yang S C, Kuo C W and Chan Y J 2000 *Electron. Lett.* **36** 1320
[19] Su K H, Hsu W C, Lee C S, Wu T Y, Wu Y H, Chang L, Hsiao R S, Chen J F and Chi T W 2007 *IEEE Electron Device Lett.* **28** 96
[20] Su Y K, Chen W C, Hsu S H, Wu J D, Chang S J, Chuang R W and Chen W R 2006 *Japan J. Appl. Phys.* **45** 3372
[21] Su K H, Hsu W C, Hu P J, Chen Y J, Lee C S, Lin Y S and Wu C L 2007 *J. Korean Phys. Soc.* **50** 1878
[22] Chuang H M, Cheng S Y, Chun-Yuan Chen, Liao X D, Liu R C and Liu W C 2003 *IEEE Trans. Electron Device* **50** 1717
[23] Lai P H, Fu S I, Tsai Y Y, Yen C H, Chuang H M, Cheng S Y and Liu W C 2006 *IEEE Trans. Device Mater. Reliab.* **6** 52