行政院國家科學委員會專題研究計畫成果報告

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中文摘要：本研究主要在考量晶圓製造廠之控片與擋片的降級特性，來構建一個控擋片管理系統之網路模式。首先是分析控擋片等級特性與控擋片使用之情況，了解控擋片與生產系統之作用。並以階段式的架構『控檔片批次演算法』，解決控擋片水準的問題。而對於『控檔片批次演算法』，是在不考慮等級調降的情況下，以拉式生產系統之存貨概念，決定不同等級間迴圈內之控擋片最佳水準。經由實例驗證，得知本模式所設定之控擋片水準，能滿足生產系統控擋片消耗之需求。因此，在控擋片提供完全無缺料之虞，此情況實能說明本文所設計之存量控制模式具有應用上之可行性與有效性。

關鍵詞：晶圓製造廠、控片、擋片、網路、拉式生產系統

Abstrac: This paper considers control/dummy (C/D) wafers level problem in the wafer fabrication furnace area, where C/D wafers are employed for monitoring particle content, measuring film thickness, examining refraction indices, filling blank wafer loading space, and precluding heat radiation from interfering the process. The objective of the problem is to determine the minimum work-in-process (WIP) level of C/D wafers, while maintaining the same level of production throughput. In this paper, we propose a C/D wafers batch (CDWB) algorithm to estimate the optimal WIP level of C/D wafers for each grade. Two circumstances are investigated and analyzed, with one considering PUR process cycle time and the other considering both the PUR process cycle time and the lacking rate of C/D wafers. Experiments with simulation studies are conducted to investigate the performance of the algorithm. The results show that the algorithm performs reasonably well in estimating the optimal WIP level of C/D wafers.

Keywords: Furnace area, control wafer, dummy wafer, work-in-process, cycle time.

1. Introduction

Control or dummy（C/D）wafers are employed for monitoring the machine parameters including a series of precision parameters of the production processes in semiconductor wafer fabrication, and for maintaining manufacturing conditions. C/D wafers are used not only to control the machine manufacturing capability, but also to increase the process yield. This paper considers C/D wafers problem at a preset WIP level for each grade, where C/D wafers in each grade are repeatedly used in the same process without downgrading. Any shortage of C/D wafers may stop the machine operations, thus affect the process yield and production planning. To avoid such situation, a large number of C/D wafers is usually prepared for use; and as a result, the WIP level of C/D wafers often increases unnecessarily. In order to simplify the complexity of the environment, we shall restrict the investigation on C/D wafers in the furnace area of wafer fabrication without considering interactions with other areas. In most wafer fabrication factories, the WIP level of C/D wafers is currently set to 30%-50% of that for normal products, with 30% being the benchmark. An increase of this preset C/D wafers level would result in an increase in holding cost but with a

decrease in shortage cost; therefore, a trade-off decision must be made. Common decisions in current industrial practice often result in maintaining each C/D wafers grade at its maximum service level. How to determine the optimal WIP level of C/D wafers for each grade is an important problem, which is essential to performance measure for the model.

2. An Overview of C/D Wafers

In wafer fabrication furnace area, control wafers are utilized for monitoring and measuring the particle content, examining refraction indices, and inspecting the thickness of the membrane cumulated on normal wafer products in the oxidization process. Dummy wafers are used for filling the blank wafer loading, and precluding heat radiation interfering the process. The use of C/D wafers can assure that the manufacturing process in the furnace area satisfying the required manufacturing specifications. C/D wafers are repeatedly used until their immaculacy and thickness do not conform to the process requirements. For C/D wafers not conforming to the process requirements, we assume that they are discarded without downgrading. To avoid pollution to the factory machines due to misuse of C/D wafers, managers often apply the C/D wafer grading rule to different machine demand according to the requirement of processing circumstances, such as the required immaculacy degree.

3. Estimating C/D Wafers WIP Level

This paper develops C/D wafers batch (CDWB) algorithm to estimate an appropriate WIP level for each grade of C/D wafers. The proposed algorithm can be divided into three phases: (1) calculating C/D wafers depletion rate, (2) determining workstation utilization, and (3) estimating cycle time of PUR process. First, the depletion rate for each grade of C/D wafers depends on the product mix ratio of normal products and the utilization of workstation for C/D wafers. The depletion time is calculated by multiplying the number of machines available, planning period, and the utilization of workstation. Second, the number of machines available is separated into the number for producing normal wafers and the number for producing C/D wafers according to the product mix between normal wafers and C/D wafers. The utilization of workstation is calculated by dividing arrival rate by service rate and number of machines available. Finally, the cycle time for each grade of C/D wafers is calculated by adding up the batch waiting time, load waiting time and the PUR process time of each grade of C/D wafers. The WIP level for each grade of C/D wafers is calculated by multiplying the depletion rate, cycle time of C/D wafers and a safety index. The estimation procedures for the three phases will be described in the next section and are depicted in Figure 1

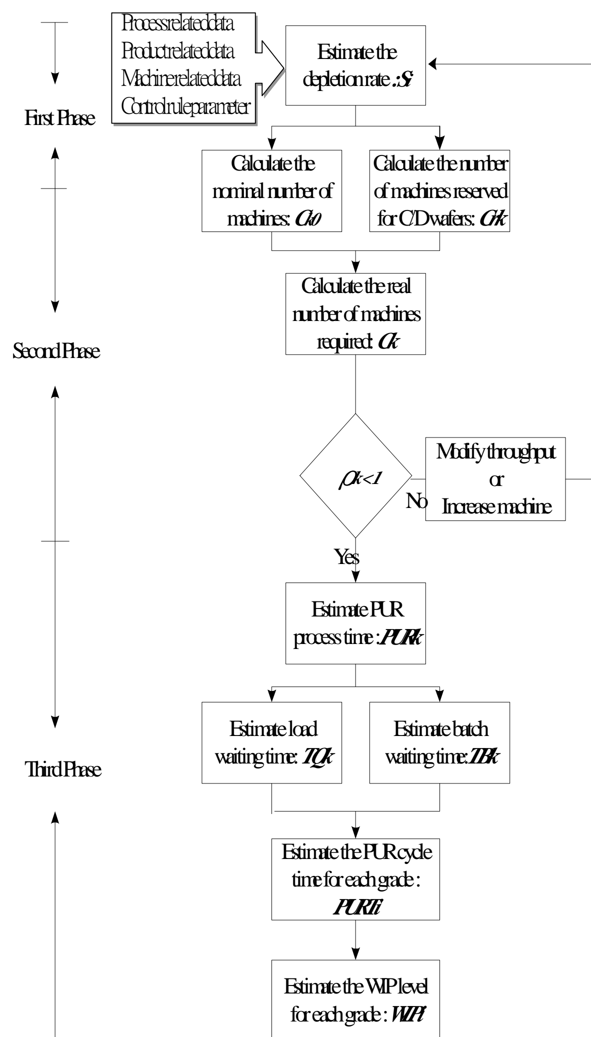

Figure 1. Flow process of the CDWB algorithm

Estimating WIP of C/D Wafers for each Grade

This paper does not consider downgrading interaction among different grades of C/D wafers. In the following, we propose an algorithm to estimate the WIP level for each grade. The C/D wafers batch (CDWB) algorithm for a single loop system may be described as follows:

Step 1. Estimate the depletion rate, S_i, for each C/D wafers grade on each machine in the furnace area under the planned production throughput target and product mix ratio.

Step 2. Calculate the number of machines available for producing normal wafers. （Nominal number）

$$C_{k0} = \sum_h \left(1 - \frac{MTTR_h}{MTBF_h + MTTR_h} - \frac{MTTPM_h}{MTBPM_h + MTTPM_h} \mid h \in workstation\ k \right)$$

Step 3. Calculate the number of machines reserved for producing C/D wafers.

$$Cr_k = \frac{p_k}{d}$$

Step 4. Calculate the number of machines available for producing normal products under the impact of C/D wafers.（Real number）

$$C_k = C_{k0} - Cr_k$$

Step 5. Evaluate the utilization rate（ρ_k）of workstation k. If the value is greater than one, then modify the throughput target or increase the number of machines to solve the problem, go to step 1. Otherwise, go to step 6.

Step 6. Estimate the theoretical process time of workstation k (PUR_k).

Step 7. Estimate the load waiting time of workstation k.

$$TQ_k = \frac{L_k}{\lambda_k} - \frac{1}{\mu_k}$$

Step 8. Estimate the batch waiting time of workstation k.

$$TB_k = \frac{B_k}{\lambda_k}$$

Step 9. Estimate the PUR process cycle time of C/D wafers for grade i.

$$PURT_i = \sum_{k \in i_{PUR}} \left(PUR_k + TQ_k + TB_k \right)$$

Step 10. Estimate the WIP level of C/D wafers for grade i.

$$\lceil WIP_i \rceil = \lceil S_i \times PURT_i \times (1 + r) \rceil$$

4. Experimental Designs and Simulation Results

In order to justify the applicability and evaluate the accuracy of the proposed C/D wafers batch algorithm, we investigate two real-world examples to study the effects of different WIP level on the system, and to search for efficient C/D wafers managing strategies. We compare our estimated parameters with the result from the simulation model built by SIMPLE^{++} simulation programming software (TECONMATIX TECHNOLOIES Ltd. (1999)). Two experiments aim to determine the WIP level of C/D wafers for each grade while meeting the system throughput target.

Basic Input Information： To verify the effect of this model, actual data are taken from a wafer fabrication factory located on the Science-Based Industrial Park in Hsinchu, Taiwan.

(1) Planning period. The planning period is 28 days.

(2) Releasing mechanism. Based on Little's formula (Hiller, 2001), we estimate total WIP level with the given throughput target and the estimated cycle time. Wafer lots are released under fixed-WIP policy for the simulation model.

Monthly output target is 630 lots, and the most suitable WIP level for the system is 270 lots. The release batch size is six lots.

(3) Dispatching rule. The dispatching rule is FIFO.

(4) Machine data for C/D wafers. In the furnace process, there are 7 workstations that require C/D wafers. The depletion of C/D wafers is related to the amount of products processed. The depletion of C/D wafers for the corresponding

5. Conclusions

Simulations have been carried out on a furnace area to study C/D wafers WIP level. The simulation results indicated that the proposed single loop CDWB algorithm provided a near optimal WIP level for C/D wafers. Its performance is fairly close to that from the simulation and it takes a very short time to calculate. In real production environment, production planner can use the proposed algorithm as the basis for routine control and management of the C/D wafers. From the results obtained in the two experiments, the CDWB algorithm performed quite well on WIP level estimation. The absolute value for the maximum discrepancy in estimating the throughput is 0.02. The overall absolute value for the maximum discrepancy in estimating the utilization is no greater than 0.03, the lacking rate is less than 0.10, and the cycle time of products is about 0.09. The results showed that the proposed algorithm has high accuracy in estimation. Further, the proposed algorithm takes only about 30 seconds CPU time for an experiment and thus outperforms other simulation packages in terms of responsiveness. With this advantage, production planners can deal with the problem of C/D wafers WIP level determination in a very short time. This investigation has taken a step in the direction of defining single loop system for C/D wafers in the furnace area wafer fabrication. It is possible, of course, that considering downgrading and diverse cost may produce different results. Future research could include other manufacturing phases in wafer fabrication such as in photolithography, CVD, thin film, etching, and ion implantation in order to construct a model of minimum cost in a variety of phases.

References

1. Chung, S. H. & Huang, H. W.(1999). The block-based cycle time estimation algorithm for wafer fabrication factories. *International Journal of Industrial Engineering*, 6(4), 307-316.

2. Chung, S. H. & Huang, H. W. (2002). Cycle time estimation for wafer fab with engineering lots. *IIE Transactions on Scheduling and Logistics*, 34(2),105-118.

3. Chen, H. C. & Lee, C. E. (2000). Control and dummy wafers management. *Journal of the Chinese Institute of Industrial Engineer*, 17(4), 437-449.

4. Hiller, F. S. & Lieberman, G. J. (2001). *Introduction to Operations Research*, Seventh Edition, McGRAW-HILL Publishing Company.

5. Glynn, P. M. & O'dea, M.(1997). How to get predictable throughput times in a multiple product environment. *1997 IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings*, 27-30.

6. Kumar, S. and Kumar, P. R. (2001). Queuing network models in the design and analysis of semiconductor wafer fabs. *IEEE Transactions on Robotics and Automation*, 17(5), 548-561.

7. Lawrence, S. R. (1995). Estimating flowtimes and setting due-dates in complex production systems. *IIE Transactions*, 27(5), 657-668.

8. Lin,Y. L. (2000). The design of inventory control model for dummy/control wafers at the furnace area in the wafer fab., *Master Thesis*, National Chiao Tung University, Hsin-Chu, Taiwan.

9. Wang, T. H., Lin, K. C. & Huang, S. R. (1997). Method of dynamically determining cycle time of a working stage. *1997 IEEE/CPMT Twenty-First Electronics Manufacturing Technology Symposium*, 403-407.

附件：封面格式

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※　　晶圓製造廠爐管區控檔片之單迴圈網路模式　　※
※ A Single Loop Network Model for Dummy/Control Wafers in the Furnace ※
※　　　　　　Area Wafer Fabrication　　　　　　※
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中 華 民 國 九十一 年 九 月 二十一 日