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Effect of annealing temperature for $Si_{0.8}Ge_{0.2}$ epitaxial thin films

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Abstract

This study investigates the effect of annealing temperature on the $Si_{0.8}Ge_{0.2}$ epitaxial layers. The $Si_{0.8}Ge_{0.2}$ epitaxial layers were deposited by using ultrahigh vacuum chemical vapor deposition (UHVCVD) with different annealing temperatures (400–1000 °C). Various measurement technologies, including high-resolution X-ray diffraction (HRXRD), atomic force microscopy (AFM) and interfacial adhesion tester, were used to characterize the materials properties of the SiGe epilayers. The experimental results showed that the SiGe epilayers gradually reduced lattice-mismatch to the underlying substrate as annealing temperature increased (from 400 to 800 °C), which resulted from a high temperature enhancing interdiffusion between the epilayers and the underlying substrate. In addition, the average grain size of the SiGe films increased from 53.3 to 58 nm with increasing annealing temperature. The surface roughness in thin film annealed at 800 °C was 0.46 nm. Moreover, the interfacial adhesion strength increased from 476 ± 9 to 578 ± 12 kg/cm^2 with increasing the annealing temperature.

Keywords: SiGe epilayers; Annealing; Adhesion strength; UHVCVD

1. Introduction

Research and development into high performance optoelectronic devices enabling ultrahigh speed operation and excellent electronic transfer characteristics were urgently required. This is because these new high-quality devices are essential for future highly intelligent information and optoelectronics systems. Silicon germanium (SiGe) gave rise to great interest due to its useful features in many optoelectronic applications, including thin-film transistors (TFTs) [1,2], modulation-doped field effect transistors (MODFETs) [3,4], metal-oxide-semiconductor field effect transistors (MOSFETs) [5,6], heterojunction bipolar transistors (HBTs) [7,8], optical modulators [9] and other applications.

The high-quality SiGe thin films, such as low density of crystal defects, smooth surface morphology and/or high interfacial adhesion strength, can achieve high performance optoelectronic devices. Unfortunately, large lattice-mismatch in germanium and silicon (∼4%) can lead to high density of crystal defects (such as misfit dislocation), or poor mechanical characteristic (include surface roughness and interfacial adhesion strength) in SiGe thin films. These structural defects and uncertain mechanical properties may seriously degrade the performance of optoelectronic devices. Several researches have used various methods to improve the material properties of SiGe films. For instance, Lee et al. [10] added a Si buffer layer to decrease the dislocation density in the SiGe films. Sheng et al. [11] used UHVCVD to deposit the SiGe epilayers on SiGe substrate for reducing the lattice-mismatch. Watakabe et al. [12] enhanced the structural properties of the SiGe films using the pulsed-laser annealing.

In this study, we report the effect of annealing temperature in thermal treatment to improve the material properties in the SiGe epilayers. The SiGe epitaxial thin films were analyzed and characterized using field emission scanning electron microscope (FESEM), HRXRD, AFM and interfacial adhesion strength tester. Experiments show that the interfacial adhesion strength and average grain size of the SiGe epilayers increase with increasing annealing temperature, and the surface roughness of the SiGe epilayers decreases with increasing annealing temperature.

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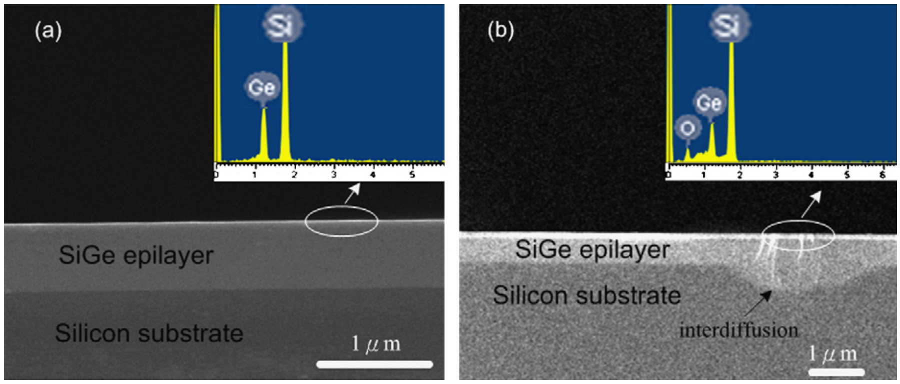

Fig. 1. SEM image of $Si_{0.8}Ge_{0.2}$/ Si(1 0 0) heterostructure (a) pre-annealing on Si, and (b) annealed at temperature 1000 °C with the energy-dispersive X-ray spectroscopy (EDS) analysis.

2. Experimental procedure

The UHVCVD technique was first described and developed by Meyerson [13]. In this study, all of the strained SiGe thin films were grown on 6-in. p-type silicon substrate orientated (1 0 0) using the UHVCVD system (ANELVA SRE-612 Inc. Japan) [14–16]. After a standard Radio Corporation of American (RCA) clean and a HF:H_2O (1:50) bath for 15 s, silicon wafers were simultaneously introduced into load-lock chamber of UHVCVD system. The system was heated to the temperature of 550 °C, and the vacuum was achieved at 1.2×10^{-9} Torr. The wafers in the load-lock chamber were directly transferred to the deposited chamber. Pure Si_2H_4 (in 1 sccm), GeH_4 (in 5 sccm) and B_2H_6 (in 1000 ppm) gas mixed were used in growing $Si_{0.8}Ge_{0.2}$ epilayers on silicon substrate. The rate of deposition was about 8.04 nm/min. Moreover, the SiGe epilayers were annealed ex situ in furnace in air.

The surface morphological characteristic of cross-section in thin films was observed by using a FESEM (JEOL JSM-6700F Inc. Japan), and the compositions in thin films were confirmed by energy-dispersive X-ray spectroscopy (EDS) analysis. Further, HRXRD (PANalytical X'Pert Pro Inc. Singapore, with Cu Kα; $\lambda = 0.154$ nm) was used to determine phase formation and the crystallographic structure of the samples. High-resolution Gonio scan ($\theta - 2\theta$) technology included the hybrid monochromator and the triple axis X-ray diffractometry was utilized to observe the structural features of SiGe thin film. Besides, AFM (Veeco Dimension 5000 Inc., USA) was used to image the surface morphology of the SiGe thin films. For each AFM parameter operating, a constant speed of 2 μm/s was obtained. The interfacial adhesion strength of SiGe thin films was measured by using an interfacial adhesion strength tester (Adhesion Tester ROMULUS III Inc., Japan).

3. Results and discussion

In order to understand the surface characteristics of the SiGe thin films before and after the heat treatments, FESEM was adopted to observe the characteristics of the films. Fig. 1 reveals the SEM image of the SiGe thin films before and after annealing. As shown in Fig. 1(a), the thickness of the SiGe films was about 614 nm before annealing. Fig. 1(b) shows a serious interdiffusion between the SiGe epilayer and silicon substrate after annealing at 1000 °C.

HRXRD analysis was performed to identify phase formation crystallographic structure of the SiGe thin films. Fig. 2 shows the XRD spectra of the (0 0 4) reflection for the layers with different heat treatment conditions. The structural property of the thin films was investigated by observing the peak width and the degree of tilt in Fig. 2. The sharp peak at the position of 69.12° was silicon substrate, and the peak at the position of 68.27° was the SiGe epilayers. The Ge composition of the SiGe epilayers measured by the XRD was 20.5% before annealing and was 17.4% after annealing at 800 °C. In this work, the thickness of the SiGe epilayers (614 nm) was larger than the critical thickness [17] of 200 nm, so the relaxation of the epilayers was unavoidable. As shown in Fig. 2, the relaxation of the films led to a shift of the SiGe peak to higher rocking angle, which the result was similar to that of Sakai et al. [18]. On the other hand, the curve annealed at 1000 °C appeared a new peak, which it could be attributed to the high temperature of 1000 °C leading to the phase transformation. Besides, the other readily observable

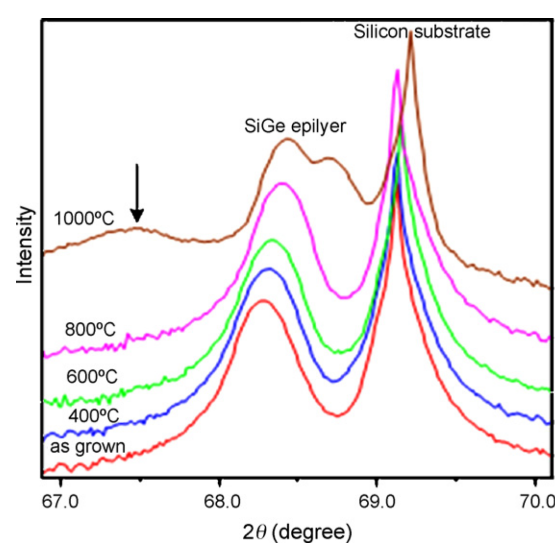

Fig. 2. The XRD spectra of the $Si_{0.8}Ge_{0.2}$ thin films with different annealing temperatures.

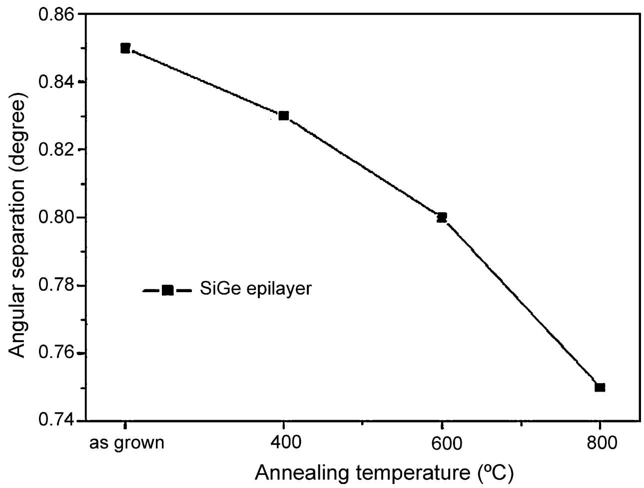

Fig. 3. The angular separation between SiGe (0 0 4) and Si (0 0 4) peaks as a function of annealing temperatures.

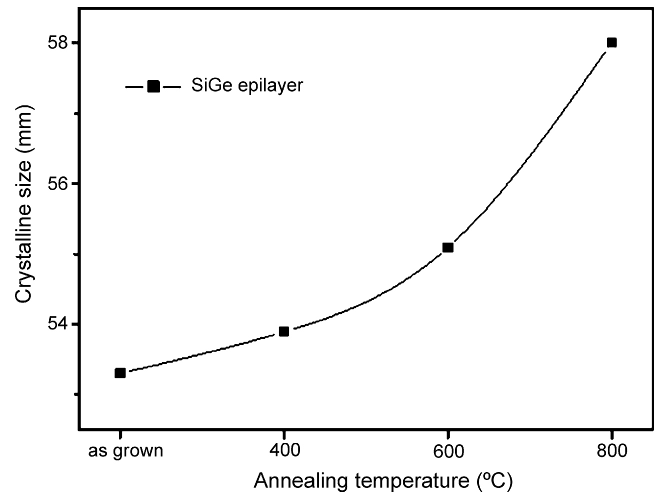

Fig. 4. The relationship between crystalline size of SiGe epilayer and annealing temperatures.

phenomenon was the change of the relative positions of Si (0 0 4) and SiGe (0 0 4) peaks. Fig. 3 indicates that the epilayers gradually reduce lattice-mismatch to the underlying substrate. The measured results showed that the angular separation decreased as the annealing temperature increased, and the results were agreeable with that of Zheng et al. [19].

The heat treatments led to a change in grain size of the thin films. The average grain size of the SiGe thin films was

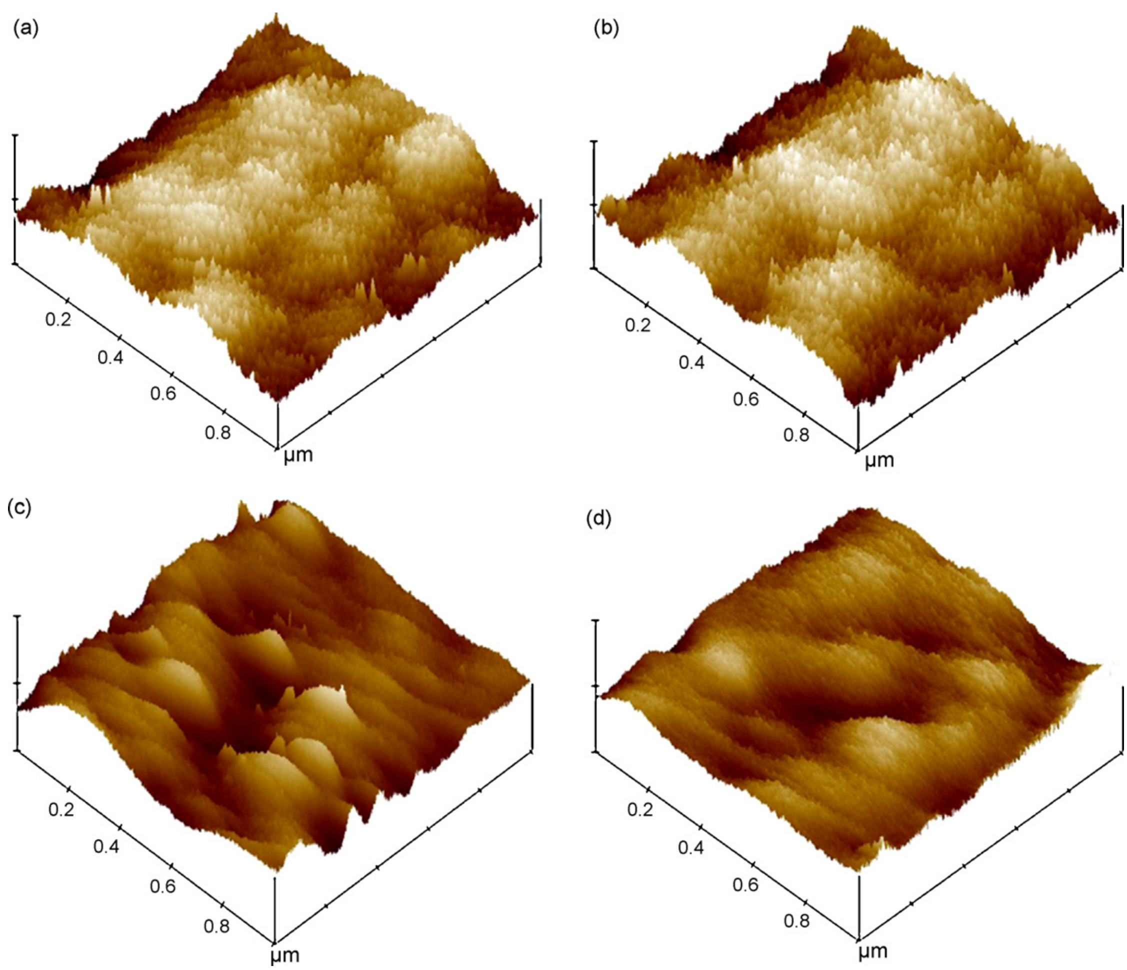

Fig. 5. AFM images of SiGe thin films in (a) as grown, and annealed at various annealing temperatures (b) 400 °C, (c) 600 °C and (d) 800 °C.

evaluated using the Scherrer equation as follows [20]:

$$L = \frac{K\lambda}{B\cos\theta} \quad (1)$$

where L represents the linear dimension of grain size, B is the full-width-half-max of the peak, λ is the wavelength of the incident X-rays (using $\lambda = 0.154$ nm X-ray), θ is the Bragg angle and K is a numerical constant value 0.93. According to Eq. (1), the average grain size of the SiGe epilayers could be yielded, and the results were presented in Fig. 4. The investigation showed that the average grain size of the SiGe epilayers was 53.3 nm before annealing and was 53.9, 55.1 and 58 nm after the annealing at 400, 600 and 800 °C, respectively. Thereby, the crystal size of the SiGe epilayers increased as the annealing temperature increased.

The electronic transport characteristics depend on the surface roughness of the SiGe thin films. Thin films with poor surface morphology will strongly degrade the performance of electronic devices [21]. The very smooth surface topography in SiGe epilayer is quite essential. Unfortunately, the relaxation of thin film will lead to induce more defects such as dislocation [22]. However, depending on heat treatment can decrease surface roughness in thin films. It may attribute to that annealing process reduced the density of crystal defects, such as threading dislocation and misfit dislocation [23]. Therefore, as shown in Fig. 5, we used AFM to measure the morphology of $Si_{0.8}Ge_{0.2}$ epitaxial layers with different annealing temperature. In our study, the 1 μm^2 area was observed and the root mean square (rms) roughness of the SiGe thin films was measured. The result showed the rms roughness of the SiGe films was 0.73 nm before annealing and was 0.46 nm after annealing at 800 °C.

The strong interfacial adhesion strength for the functional thin films is essential. Thin film with poor interfacial adhesion strength will lead to the uncertain performance and premature failure of electronic devices. The interfacial adhesion strength of the SiGe thin films relies on the heat treatments. The adhesion strength tester was utilized to measure the interfacial adhesion strength of the SiGe thin films. Fig. 6 depicts the relationship between the interfacial adhesion strength and annealing temperature for the SiGe films. The measured results revealed that the SiGe epilayers had an adhesion strength of 476 ± 9 kg/cm^2 before annealing and an adhesion strength of 578 ± 12 kg/cm^2 after annealing at 800 °C. The interfacial adhesion strength of the SiGe films increased gradually with increasing annealing temperature. The SiGe epilayer has higher interfacial adhesion strength at a higher annealing temperature of 800 °C.

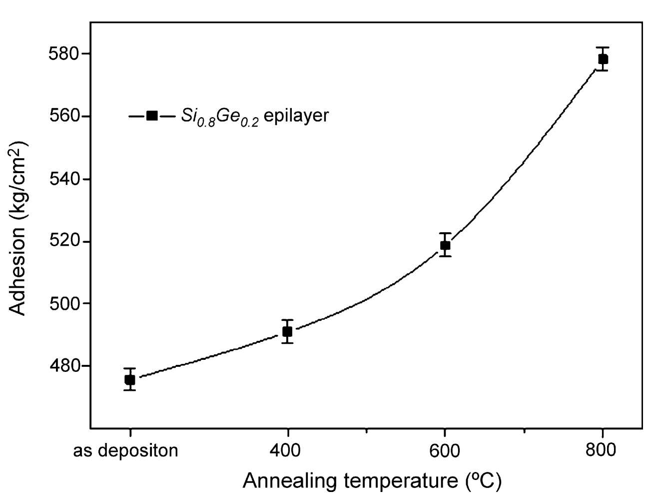

Fig. 6. Interfacial adhesion strength in SiGe thin films versus annealing temperature.

The $Si_{0.75}Ge_{0.25}$ film, presented by Bang et al. [24], was deposited on silicon substrate with SiO_2 of 1000 Å, which the average grain size of the film was 73 nm after annealing at 650 °C. Wang et al. [25] used the ion beam sputtering to deposit the SiGe films on n-Si substrate, and the average grain size of the SiGe films was 34.5 nm after annealing at 800 °C. A comparison of the above literatures, the average grain size of this work (58 nm) is larger than that of Buca et al. [26]. The SiGe films, proposed by Buca et al. [26], were grown on silicon substrate by the chemical vapor deposition, and the rms roughness of the SiGe films was 0.6 nm after an annealing of 850 °C. Sheng et al. [11] employed UHVCVD to grow the SiGe films on SiGe substrate, which the films had an rms roughness of o.267 nm. Comparing with Buca et al. [26] and Sheng et al. [11], the rms roughness of this work (0.43 nm) exceeds that of Buca et al. [26].

4. Conclusion

In summary, as the experimental result indicated, we successfully improved the material properties of the SiGe epilayers. The HRXRD, AFM and interfacial adhesion tester, were employed to measure the materials properties of the SiGe epilayers. The experimental results revealed that the SiGe epilayers had an average grain size of 53.3 nm before annealing and an average grain size of 58 nm after annealing at 800 °C. The rms roughness of the SiGe epilayers was 0.73 nm before annealing and 0.43 nm after annealing of 800 °C. The interfacial adhesion strength of the SiGe epilayers was 476 ± 9 kg/cm^2 before annealing and 578 ± 12 kg/cm^2 after annealing at 800 °C. The SiGe epilayers reduced lattice-mismatch to the silicon substrate depending on the annealing process. The average grain size and interfacial adhesion strength of the SiGe epilayers increased with increasing annealing temperature. The surface roughness of the SiGe epilayers decreased with increasing annealing temperature.

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