行政院國家科學委員會補助專題研究計畫成果報告

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計畫類別：▒個別型計畫　　□整合型計畫
計畫編號：NSC 90-2218-E-009-043-
執行期間：90/08/01 ~ 91/07/31

計畫主持人：陳明哲

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執行單位：國立交通大學電子工程學系

中　華　民　國　91　年　10　月　25　日

行政院國家科學委員會專題研究計畫成果報告

超薄氧化層高等可靠性物理暨次世代快閃式記憶體之前瞻性研究

Pioneering Study on Ultrathin Oxide Advanced Reliability Physics and Next-Generation Flash Memory

執行期限: 90/08/01 ~ 91/07/31
計畫編號: NSC 90-2218-E-009-043-

主持人：陳明哲教授　　國立交通大學電子工程學系

一、中文摘要

本計劃提出之目的有二，第一目的為具體有效地提昇現階段對超薄氧化層薄膜可靠性物理的了解。首先，一個創新滲透統計模式提供超薄氧化層在經歷應力引致漏電流及軟崩潰發展過程中所產生陷阱之數量，並據以得到應力引致漏電流之電流電壓特性以及軟崩潰後之氧化層電流電壓特性。其二，我們進行實驗以發掘 P 型通道場效電晶體之應力引致漏電流及軟崩潰對電洞能量的依賴，並配合理論之建立。其三，一種改進的陷阱至陷阱隧道穿透工具將用以靈敏偵測超薄氧化層在應力時所產生的微觀尺度陷阱。此技術也將延伸至 P 型通道元件。其四，執行電報雜訊技巧以提供應力引致漏電流及軟崩潰之動態特性。此特性可用來萃取陷阱時間常數、陷阱位置以及陷阱分佈。最後，徹底探討低頻或 1/f 雜訊在氧化層厚度微縮的研究並與其它靈敏測量工具作一比較。

第二目的則為第一目的的應用於次世代快閃記憶體、射頻、輸出入的研發。我們示範如何利用超薄氧化層陷阱產生模式及隧道穿透模式設計出次世代快閃式記憶體應用規格以迄測試鍵的產製、量測及分析。

關鍵詞： 氧化層、應力引致漏電流、軟崩潰、滲透、電報雜訊、低頻雜訊、1/f雜訊、陷阱至陷阱隧道穿透、電洞、擾動、可靠性、互補式金氧半場效電晶體、直接隧道穿透、快閃式記憶體、毫微米元件、射頻、輸出入。

Abstract

This project is proposed with two-fold aims. The first aim is to advance significantly current understandings of reliability physics underlying ultrathin oxide films. First of all, a novel percolation statistical model offers trap quantity in ultrathin oxides undergoing SILC (stress induced leakage current) and soft breakdown, which in turn yields SILC I-V and soft breakdown I-V. Particularly addressed are dynamic behaviors in soft breakdown as well as temperature effects on SLIC and soft breakdown. Second, we carry out experiment for exploring the dependencies of SILC and soft breakdown in p-MOSFETs on hole energy, along with theory set up. Third, an improved means via trap-to-trap tunneling is employed for sensitively detecting microscopic traps in ultrathin oxides during stressing. This technology is extended to p-channel counterpart as well. Fourth, RTS (Random Telegraph Signal) technique is performed to provide dynamic characteristics of SILC and soft breakdown. Such characteristics are amenable for extraction of trap lifetime, trap position, and trap distribution. Finally, low-frequency or 1/f noise for scaled oxide thicknesses, as well as comparisons with other sensitive characterization means, is thoroughly examined.

The secondary aim is to highlight promising potential in implementation of next-generation flash memory, RF and I/O. We will show how to apply our trap generation model, tunneling model, and other means such

as to create design specifications or window where scaled flash memory can work reliably during F-N or Direct tunneling for program/erase cycles. Also explored are fabrication, characterization, and analysis of a series of test-key.

Keywords: Oxide, SILC, Soft Breakdown, Percolation, Random Telegraph Signal (RTS), Low-Frequency Noise, 1/f Noise, Trap-to-Trap Tunneling, Hole, Fluctuation, Reliability, CMOS, MOSFET, Direct Tunneling, Flash Memory, Nanodevices, RF, I/O

二、緣由與目的

了解超薄氧化層薄膜的可靠性物理（Reliability Physics）機制就如同掌握一把通往未來之路的鑰匙。理由是：它關鍵性地決定目前主流 CMOS 元件技術今後數年的走向直到受到物理基本法則限制；它攸關了世代 Gate 替換材料的潛在品質；就奈米元件技術而言，它開啟了創新的可能。研發下一世代 Flash memory, RF and I/O 非得有超薄氧化層薄膜的高等可靠性物理理解不可。

在這樣願景之下的可靠性物理顯然需具備如下三項：量子級觀點，依據量測 C-V 及 I-V 數據精確評估超薄氧化層厚度至小數點第 2 位（以 nm 為單位）；以 Poisson 及 Markov 統計併合 percolation 統計以處理微觀擾動 Fluctuation 現象；高度靈敏的氧化層陷阱 trap 偵測工具。

本研究群在上述領域鑽研至深，已在權威性學術刊物及國際會議發表一二：成功建立量子力學電子及電洞直接隧道穿透模式，厚度精確至小數點第 2 位，吻合 HTEM Device 及 C-V 等實驗。成功建立 nano-Sphere percolation 統計模式，恰當地重現 soft breakdown 現象。成功建立一套光學偵測系統：高精確偵測氧化層陷阱。成功建立低頻雜訊量測系統,能高度靈敏偵測 oxide trap 並對 percolation path 予以定位。

三、研究方法與成果

1. Percolation 統計模式之創新應用

計算超薄氧化層在 stress 時產生 traps 數量預測 SILC 並實驗驗證；計算超薄氧化層在 stress 時發生 soft breakdown 之 local percolation path，據此建立 soft breakdown I-V 模式並考慮 dynamic 行為：trapping-and-detrapping, quantum dot switching, Poisson process；

2. Hole 能量對 SILC/Soft Breakdown 之影響

以 p-channel MOSFETs 元件重 n-channel MOSFETs 實驗程序，進行 SILC 及 Soft Breakdown 之時間量測；建立 Hole 能量與 SILC 及 Soft Breakdown 之相互關係；建立理論解釋此關係並與文獻比較。

3. Trap-to-Trap Tunneling/時域擾動高靈敏度偵測技術

時域擾動 RTS（Random Telegraph Signal）可提供 dynamic behavior 有用資訊，並可萃取 trap 相關參數如 lifetime, position, distribution 等。

4. Low-frequency noise 量測及分析

我們 2001 年 1 月出版的 JAP paper 探討 3.3nm 厚超薄氧化層在 SILC 以及 soft breakdown 發展過程中的 Low-frequency noise or 1/f noise，並由此得到一連串創新發現。本計畫延伸至 2.5nm 厚以下之超薄氧化層薄膜結構。亦與其他技術作一比較如光學偵測系統、SILC、Trap-to-Trap Tunneling 技術、RTS 等。

5. 次世代 Flash memory, RF, I/O 前瞻應用

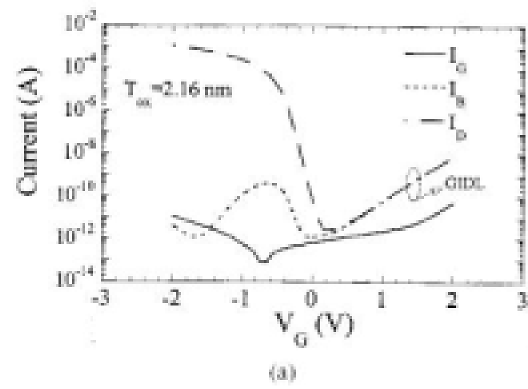
利用前述可靠性物理計算 design window；產製 Test wafer 量測建立數據並分析。

四、結論與討論

1. 完成 Percolation 統計模式創新應用。
2. 完成 Hole 能量對 SILC 及 Soft breakdown

之影響。

3. 完成 Trap-to-Trap Tunneling 偵測技術。
4. 完成時域電報雜訊偵測技術。
5. 完成低頻雜訊偵測技術。
6. 完成次世代 Flash memory 前瞻應用。
7. 完成 RF and I/O 創新研究。



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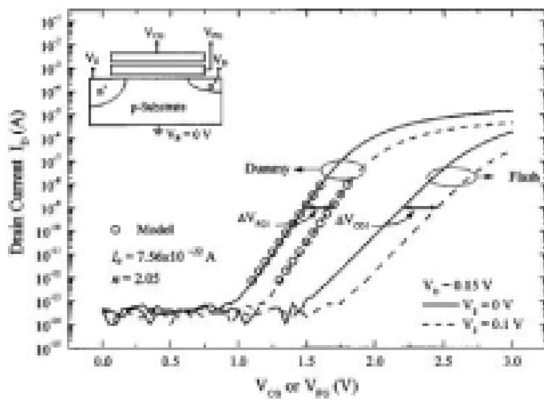


Fig. 1. Drain currents measured as a function of control gate voltage (V_{CG}) in flash memory cell and floating gate voltage (V_{FG}) in dummy transistor. V_D = 0.05 V and V_S = 0 and 0.1 V. The extracted control gate voltage shift (ΔV_{CG1}) and floating gate voltage shift (ΔV_{FG1}) are labeled at specific subthreshold current level of 10^{-10} A. The extracted values of I_o and n for two subthreshold current–voltage (I–V) of a dummy transistor are shown.

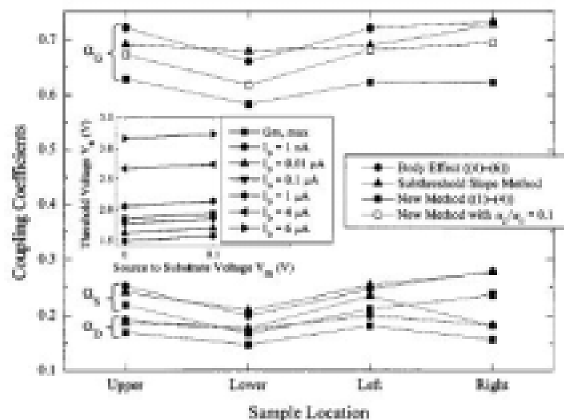
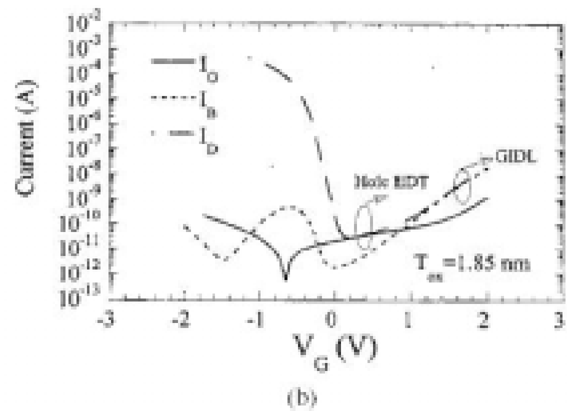


Fig. 2. Gate, drain, and source coupling coefficients extracted from various methods, plotted versus four different locations on the wafer. Involved voltage shifts are: ΔV_{CG1} ranges from 0.24 V to 0.25 V; ΔV_{CG2} from 0.24 V to 0.25 V; ΔV_{CG3} from −0.06 V to −0.05 V; ΔV_{FG1} from 0.19 V to 0.20 V; and ΔV_{FG2} from 0.19 V to 0.20 V. The inset of the figure shows the extracted V_{th} versus V_{SB} for the position "Left" by the maximum transconductance extrapolation and the constant current forcing.



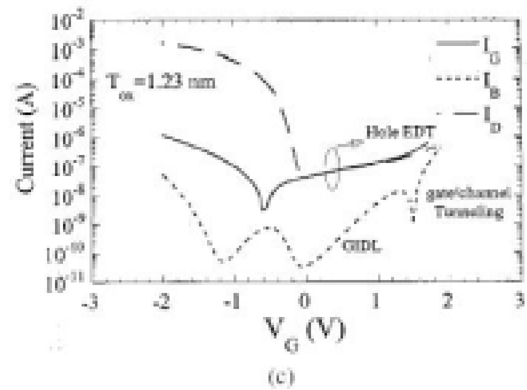


Fig. 3. Measured terminal currents versus gate voltage for both polarities. The aspect ratio is W/L = 10 μm/0.5 μm. Source grounded and V_D = −1.8 V.

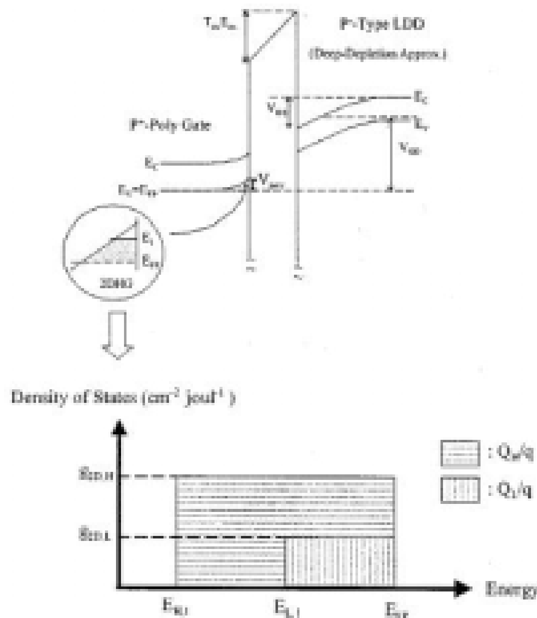


Fig. 5. Band diagram drawn along p+-polysilicon/oxide/drain extension. The accumulation potential bending, V_{pedge}, with 2-D hole gas (2DHG) concept and the silicon surface potential, V_{DEL}, with the deep depletion approximation are adopted in the procedure of E_{OX} calculation.

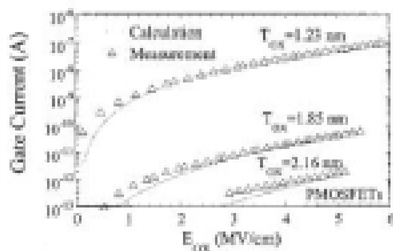


Fig. 6. Comparison of the calculated and experimental hole EDT current versus E_{OX}. The extracted effective EDT range is 6 nm wide from the gate edge. $W = 30\ \mu m$.

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