IEICE TRANS. ELECTRON., VOL.E91–C, NO.3 MARCH 2008

PAPER

Circuit Performance Degradation of Switched-Capacitor Circuit with Bootstrapped Technique due to Gate-Oxide Overstress in a 130-nm CMOS Process*

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SUMMARY The MOS switch with bootstrapped technique is widely used in low-voltage switched-capacitor circuit. The switched-capacitor circuit with the bootstrapped technique could be a dangerous design approach in the nano-scale CMOS process due to the gate-oxide transient overstress. The impact of gate-oxide transient overstress on MOS switch in switched-capacitor circuit is investigated in this work with the sample-and-hold amplifier (SHA) in a 130-nm CMOS process. After overstress on the MOS switch of SHA with unity-gain buffer, the circuit performances in time domain and frequency domain are measured to verify the impact of gate-oxide reliability on circuit performances. The oxide breakdown on switch device degrades the circuit performance of bootstrapped switch technique.

key words: *gate-oxide reliability, sample-and-hold amplifier, dielectric breakdown, bootstrapped switch, switched-capacitor circuit*

1. Introduction

The switched-capacitor circuit is an important building block in analog integrated circuits, such as analog-to-digital data converter (ADC). The high-speed and high-resolution analog-to-digital data converter needs a high performance switched-capacitor circuit. The low-supply voltage will degrade the performance of the switched-capacitor circuit due to the nonlinear effects of the MOSFET switch such as body effect, turn-on resistance variation, charge injection, and clock feedthrough [1]–[9].

The bootstrapped switch [1]–[4] and switched-opamp (switched operational amplifier) techniques [5]–[9] have been widely used in low-voltage switched-capacitor circuit. The switched-opamp technique is not suitable for high-speed switched-capacitor circuit, because it needs much more time to turn an opamp on/off than to turn a switch on/off [6]. The bootstrapped technique provided a constant voltage between the gate and drain nodes of the MOS switch is used to improve the performances of low-voltage and high-speed switched-capacitor circuit. However, the bootstrapped technique causes the gate-oxide overstress on the MOS switch to degrade the lifetime of switch device [1]. The gate-oxide reliability of MOS switch in the low-voltage and high-speed switched-capacitor circuit with the bootstrapped technique is a very important reliability issue. The suitable device size design for the bootstrapped switch circuit [1], the thick-oxide MOSFET device [2], and the drain extended MOSFET device [3] can be used to avoid the gate-oxide overstress on the switch devices. Some design techniques of limit gate voltage in bootstrapped switch circuit had been proposed [4]. The impact of gate-oxide reliability on circuit performance of switched-capacitor circuit with bootstrapped technique wasn't investigated in the previous works [1]–[4].

In this work, the impact of gate-oxide reliability on MOS switch in the switched-capacitor circuit with the bootstrapped technique is investigated with the sample-and-hold amplifier (SHA) in a 130-nm CMOS process [10]. The time-domain and frequency-domain circuit performances of the SHA with the unity-gain buffer are measured after the gate-oxide overstress on the MOS switch.

2. Bootstrapped Technique with Gate-Oxide Reliability

The conceptual schematic of the bootstrapped technique for switched-capacitor circuit is shown in Fig. 1(a). The basic schematic includes the signal MOS switch M_S, five ideal switches S_1-S_5, and a capacitor C_b. The CLK_1 and CLK_2 clock signals are the out-of-phase signals. When CLK_1 is low and CLK_2 is high (under sampling mode), the S_3 and S_4 switches charge the capacitor C_b to the supply voltage V_{DD}, and the S_5 switch is used to turn off the switch device M_S. When CLK_1 is high and CLK_2 is low (under hold

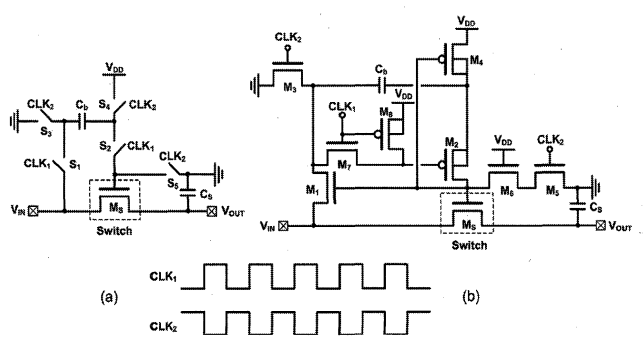

Fig. 1 (a) Conceptual schematic and (b) detail circuit implementation of bootstrapped technique for switched-capacitor circuit.

Manuscript received June 19, 2007.
Manuscript revised October 2, 2007.

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*This work was supported in part by the National Science Council (NSC), Taiwan, R.O.C., under Contract NSC 96-2221-E-009-182.

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DOI: 10.1093/ietele/e91–c.3.378

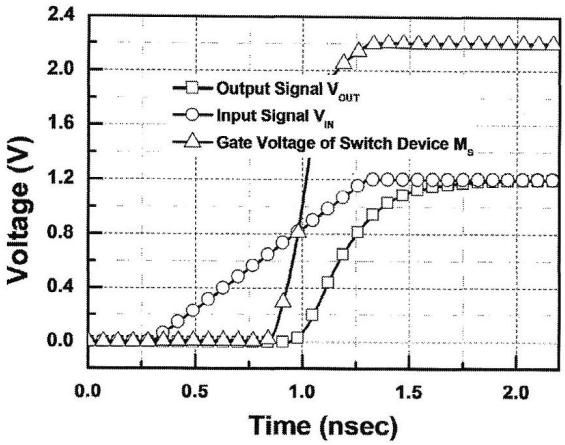

Fig. 2 Simulated waveforms of gate-oxide transient overstress event in the switched-capacitor circuit with bootstrapped technique.

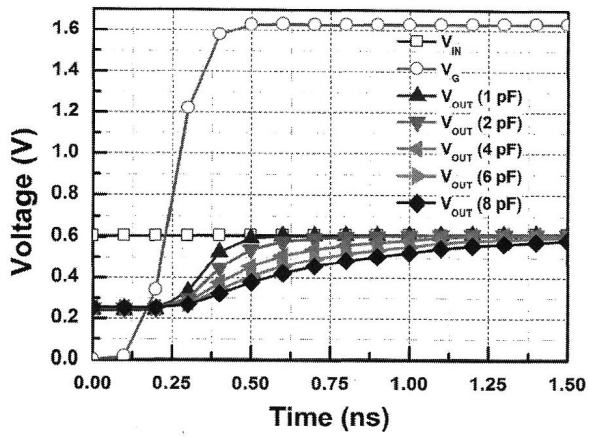

Fig. 3 The dependence of the different sampling capacitors on output voltage waveform in the switched-capacitor circuit with the bootstrapped technique.

mode), the S_1 and S_2 switches change the capacitor C_b in series with the input signal V_{IN} and connect to the gate of the switch device M_S, such that the gate-to-source voltage across the switch device M_S is equal to the supply voltage V_{DD}. The gate voltage of switch device M_S will be charged to $V_{IN}+V_{DD}$, which is larger than the supply voltage. The detailed circuit implementation is shown in Fig. 1(b) [11]. The M_1, M_2, M_3, M_4 and M_5 correspond to the five ideal switches S_1-S_5 of Fig. 1(a). The M_6 transistor is added to reduce the maximum drain-to-source voltage (V_{DS}) of M_5 transistor to avoid the gate-oxide overstress. The capacitor C_b must be large enough to supply charge to the gate of switch device in addition to all parasitic capacitors in the charge path. Moreover, charge sharing will significantly reduce the boosted voltage [1].

The sampling capacitor C_S in the switched-capacitor circuit with the bootstrapped technique is usually designed with several pF to improve the circuit performance. If the rise time of the voltage at gate node of the switch device is too fast, a large voltage could exist across the gate oxide of the switch device to degrade the lifetime of the switch device, before a channel is formed to equalize the potential between the source and drain. In order to explain the gate-oxide transient overstress event in switched-capacitor circuit with bootstrapped technique, the simulated waveforms of the bootstrapped switch circuit are shown in Fig. 2. The drain node of the switch device is driven by an input signal V_{IN}, and the source node of the switch device is connected to a large sampling capacitor. As the switch device turns on, an approximate voltage of V_{IN} + V_{DD} will be generated on the gate node to keep the constant voltage V_{DD} between the gate and drain nodes of the switch device. Before a channel is formed and before the sampling capacitor is charged to supply voltage V_{DD}, an excessive voltage greater than V_{DD} may exist across the gate-to-source side of the switch device. This effect could create an oxide reliability problem. In Fig. 2, the simulated result is a worse case of switched capacitor circuit with bootstrapped technique under the gate-oxide transient overstress.

The input signal frequency, sampling frequency, and delay times of bootstrapped and sampling networks are the major design factors in the switched-capacitor circuit with the bootstrapped technique. Figure 3 shows the dependence of the different sampling capacitors on output voltage waveform in the switched-capacitor circuit with the bootstrapped technique. The V_G is the gate voltage of the switch device M_S. The input signal V_{IN} is set to 2-MHz sinusoidal signal with peak-to-peak amplitude of 1.2 V, and sampling frequency is set to 10 MHz. The different sampling capacitors in the switched-capacitor circuit with bootstrapped technique can be used to simulate the different delay times of the sampling network. The difference RC delay time between the sampling network (M_S and C_S) and the bootstrapped network (M_1-M_8 and C_b) will induce the gate-oxide transient overstress across the gate-to-source side of the switch M_S to cause the long-term reliability issue in the switched-capacitor circuit with the bootstrapped technique.

The dependences of the input/sampling frequency (f_I/f_S) ratio on maximum transient voltage in the switched-capacitor circuit with the bootstrapped technique are shown in Fig. 4. The maximum transient voltage is defined as the maximum voltage difference between the source node and the gate node of the switch M_S during the sampling mode. The sampling capacitor of the switched-capacitor circuit with bootstrapped technique is set to 8 pF. The high input/sampling frequency ratio has a larger transient voltage than the low input/sampling frequency ratio in the switched-capacitor circuit with the bootstrapped technique.

The overstress time is related to the RC time constant ratio of the sampling and bootstrapping networks in the bootstrapped switch technique. Based on Figs. 3 and 4, the RC delay time of the bootstrapped network should be designed slower than that of the sampling network in the switched-capacitor circuit with the bootstrapped technique to avoid the transient gate-oxide reliability. The best solution is that the bootstrapped and sampling networks have the same RC delay times to avoid the transient gate-oxide over-

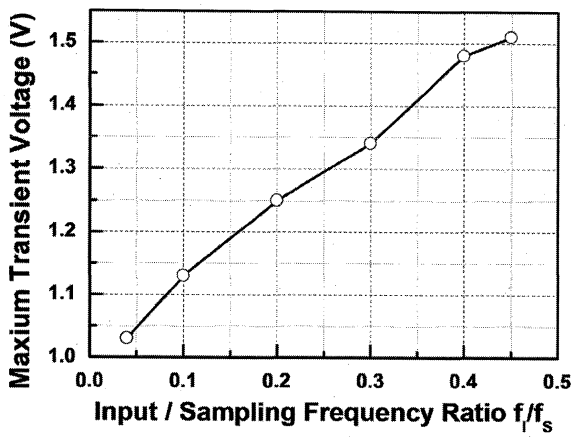

Fig. 4 The dependence of the input/sampling frequency ratio on maximum transient voltage in the switched-capacitor circuit with the bootstrapped technique.

stress and to achieve the best performance.

3. Switched-Capacitor Circuit with Gate-Oxide Reliability Test Circuit

The switched-capacitor circuit with the bootstrapped technique has a long-term reliability problem which causes circuit performance degradation. The overstress voltage on the gate oxide of the switch device depends on the voltages of input and clock signals. The obvious degradation of circuit performance in the switched-capacitor circuit with the bootstrapped technique needs a long-term operation, which may need many years, to observe the change due to the gate-oxide degradation of the switch device. The gate-oxide degradation of the switch M_S in the switched-capacitor circuit with bootstrapped technique is more likely to occur as the conventional time-dependent dielectric breakdown (TDDB). The TDDB accelerated lifetime-model equation for the nMOSFET can be expressed as [12].

$$t_f = A_{\mathrm{TDDB}} \left(\frac{1}{A}\right)^{\frac{1}{\beta}} F^{\frac{1}{\beta}} V_{\mathrm{gs}}^{a+bT} \exp\left(\frac{c}{T} + \frac{d}{T^2}\right), \qquad (1)$$

where $A = W \times L$ is the device gate-oxide area, β is the Weibull slope parameter, F is the cumulative failure percentage at use condition, V_{gs} is the gate-to-source voltage, T is the temperature, and a, b, c, and d are the model-fitting parameters determined from the experimental work, A_{TDDB} is the model factor. Note that $a + bT$ is always negative. The model of TDDB breakdown related with frequency is still a challenge. Equation (1) is not suitable to calculate the lifetime of the switch device in the switched-capacitor circuit with bootstrapped technique. Therefore, to investigate the impact of gate-oxide reliability on circuit performance of the switched-capacitor circuit with bootstrapped technique is very important in advanced CMOS technology.

In order to accelerate the degradation of circuit performance and to understand the impact of gate-oxide transient overstress event on switched-capacitor circuit with bootstrapped technique, the SHA with the gate-oxide reliability

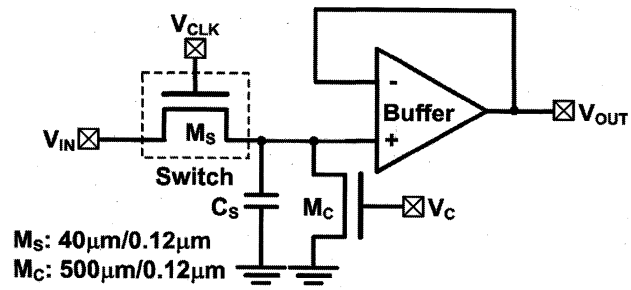

Fig. 5 The complete circuit of sample-and-hold amplifier with the gate-oxide reliability test circuit, where the control device M_C is used to control the source voltage of the switch device M_S for reliability test.

test circuit is proposed in Fig. 5. The SHA with unity-gain buffer is used to verify the gate-oxide reliability of the bootstrapped switch. The two-stage operational amplifier is used to realize the output buffer. The folded-cascode operational amplifier and common-source amplifier are used to form the two-stage operational amplifier to achieve high output swing and high small-signal gain. Simulated by HSPICE, the two-stage operational amplifier has the open-loop gain of 75 dB, the unity-gain frequency of 160 MHz, and the phase margin of 87.3 degrees, respectively, under output capacitive load of 2.5 pF. The normal operating voltage and the gate-oxide thickness (t_{ox}) of all MOSFET devices in the SHA with the gate-oxide reliability test circuit are 1.2 V and 2.63 nm, respectively, in a 130-nm CMOS process.

The control device M_C is used to control the source voltage of the switch device M_S. Therefore, the device dimension of the control device M_C should be designed larger than that of the switch device. The device dimensions of switch device (M_S) and control device (M_C) are selected as 40 μm/0.12 μm and 500 μm/0.12 μm, respectively, in a 130-nm CMOS process. If the device dimension of the control device is smaller than that of the switch device, the source voltage of switch device M_S will not be kept at near ground. In normal operation, the control voltage V_C is biased to ground, such that the control device M_C will be turned off. The SHA with the unity-gain buffer can be successfully operated. In the gate-oxide overstress test, the control voltage V_C is biased to supply voltage V_{DD}, and input signal V_{IN} is biased to the supply voltage V_{DD}. The voltage at V_{CLK} node can be applied with any higher voltage level than the supply voltage to overstress the gate oxide of switch device. The voltage across the gate-to-source nodes of switch device M_S can be controlled by the V_{CLK} voltage.

However, the switch device suffers from the dynamic (AC) stress in the real operation. The dynamic stress is less harmful than DC stress on switch device, but the dynamic stress on switch device still causes damage on gate oxide of switch device after long-term operation. The DC stress on switch device can be used to accurately estimate the damage occurring on the switch device to investigate the impact of gate-oxide reliability on MOS switch with bootstrapped technique. The difference between the AC stress in real case and DC stress in this test has the different degraded times of

circuit performance, but they will have the same degradation trend on circuit performance after long-term operation [13]. Therefore, the proposed test circuit can be used to verify the impact of gate-oxide breakdown on circuit performance of the bootstrapped switch technique.

The test chip has been fabricated in a 130-nm CMOS process, and the normal operating voltage of all MOSFET devices is 1.2 V. The chip micrograph and layout view of the SHA with the gate-oxide reliability test circuit are shown in Figs. 6(a) and 6(b), respectively. The occupied silicon area including two testing circuits and ESD (electrostatic discharge) protection devices is $390\,\mu m \times 390\,\mu m$. The top layer of test chip is covered and protected by polyimide layer. Figure 7 shows the simulated frequency-domain (10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node) and time-domain (10-MHz sampling frequency at V_{CLK} node and 1-MHz sinusoidal signal at V_{IN} node) waveforms of the sample-and-hold amplifier with the gate-oxide reliability test circuit under normal operation. The signal at V_{CLK} node is applied with clock signal between 0 V to 1.2 V. Simulated by HSPICE, the spurious free dynamic range (SFDR) of the SHA with the gate-oxide reliability test circuit is 38.6 dB.

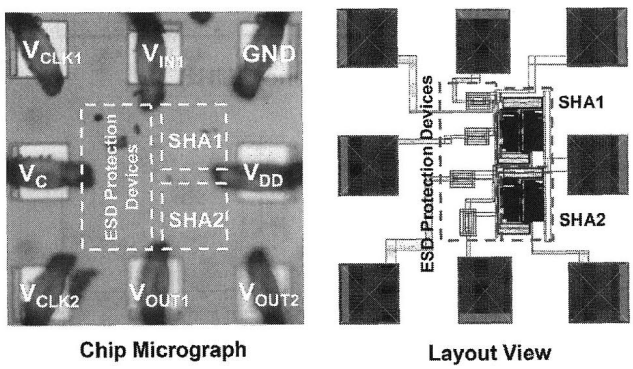

Fig. 6 (a) Chip micrograph and (b) layout view of the sample-and-hold amplifier with the gate-oxide reliability test circuit realized in a 130-nm CMOS process. Two sets of test circuit in Fig. 5 are fabricated on the chip.

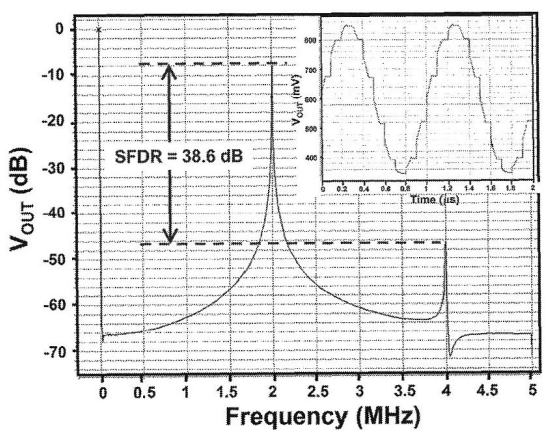

Fig. 7 The simulated frequency-domain and time-domain waveforms of the sample-and-hold amplifier with the gate-oxide reliability test circuit under normal operation.

4. Experimental Results

When the SHA with the gate-oxide reliability test circuit is operating in the overstress mode, the input signal V_{IN} is biased to supply voltage, and the control voltage V_C is set to supply voltage. In order to observe the circuit performance degradation of the SHA due to the gate-oxide degradation of the switch device, the voltage at V_{CLK} node is kept to 2.4 V for accelerating the gate-oxide degradation of the switch device. Only the gate-to-source nodes of the switch M_S is overstressed to simulate the switched-capacitor circuit with the bootstrapped technique. The measured results of test circuit are measured with die under test on the printed circuit board (PCB). When the time-domain and frequency-domain waveforms are re-evaluated after the gate-oxide overstress on the MOS switch, the signal at V_{CLK} node is applied with clock signal between 0 V to 1.2 V. After overstress time of 5.2 hours, the gate-oxide breakdown occurred on the switch device. The gate-leakage current ($I_{G-leakage}$) of the switch

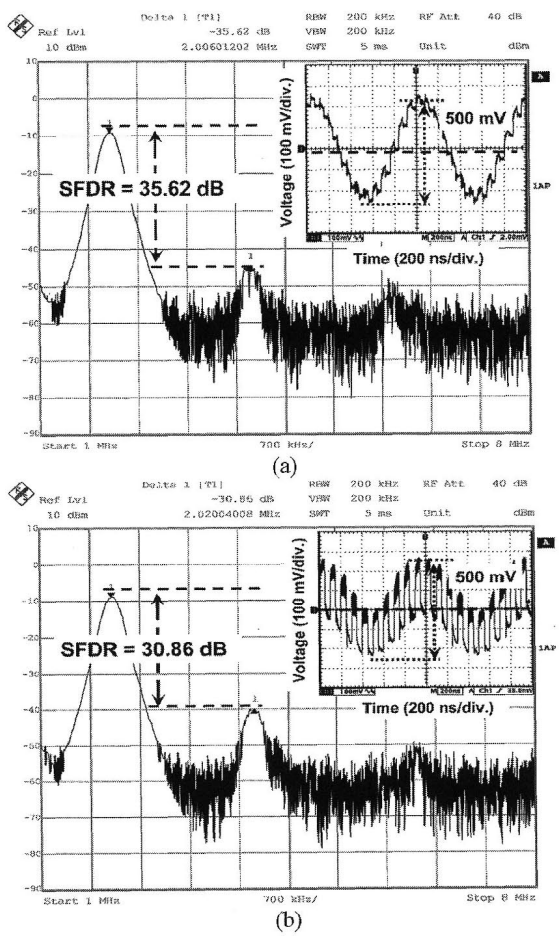

Fig. 8 The measured frequency-domain and time-domain waveforms of the sample-and-hold amplifier with the gate-oxide reliability test circuit. (a) Overstress time = 0 hour, and (b) overstress time = 5.2 hours.

device is jumped from 330 nA to 80.6 μA under V_{CLK} of 2.4 V due to the gate-oxide breakdown.

Figures 8(a) and 8(b) show the frequency-domain (10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node) and time-domain (10-MHz sampling frequency at V_{CLK} node and 1-MHz sinusoidal signal at V_{IN} node) waveforms at V_{OUT} node under the different stress times. Though date is shown till 8 MHz, only the date below 5 MHz is valid because of aliasing by Nyquist criterion. The SFDR of the test circuit is degraded by the gate-oxide breakdown on the switch device from 35.62 dB to 30.86 dB, because the gate-oxide breakdown causes extra gate-leakage current across gate oxide of the switch device to degrade the circuit performances of the SHA with the gate-oxide reliability test circuit. However, the amount of gate-leakage current depends on the gate-oxide breakdown location of the switch device. The gate-oxide breakdown location near channel region of the switch device (soft breakdown) has a smaller gate-leakage current than that near the drain or source side of the switch device (hard breakdown) [14].

5. Discussion

In order to investigate the impact of gate-oxide breakdown location (switch device) on performances of the switched-capacitor circuit with bootstrapped technique, the prior proposed method [14] can be used to simulate this impact with HSPICE. The gate-oxide breakdown of a MOSFET device can be modeled as resistor. Only the gate-to-diffusion (source or drain) breakdown was considered, since it represents the worst-case situation [12], [14]. Breakdown to the channel can be modeled as a superposition of two gate-to-diffusion events. Typical hard breakdown leakage has a close-to-linear I-V curve and an equivalent resistance of $\sim 10^3$–$10^4\,\Omega$. However, typical soft breakdown paths have high non-linear, power law I-V curve and equivalent resistance above 10^5–$10^6\,\Omega$ [14]. The equivalent breakdown resistance ($V_{CLK}/I_{G\text{-leakage}}$) of the switch device after overstress is approximate 30 kΩ (hard gate-oxide breakdown) under V_{CLK} of 2.4 V.

The SHA including equivalent breakdown resistors R_{GD} and R_{GS} is shown in Fig. 9(a). The simulated frequency-domain (10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node) and time-domain (10-MHz sampling frequency at V_{CLK} node and 1-MHz sinusoidal signal at V_{IN} node) waveforms of the SHA with equivalent breakdown resistor (R_{GS} and R_{GD}) of 30 kΩ are shown in Figs. 9(b) and 9(c), respectively. Comparing the simulated (Fig. 9(c)) and measured (Fig. 8(b)) results, the gate-oxide breakdown on the switch device in the SHA with the gate-oxide reliability test circuit is near the source side of the switch device. The differences between Fig. 8(b) and Fig. 9(c) are due to the gate-to-channel and gate-to-drain breakdowns on the switch device caused the extra gate leakage current in the SHA. Only the gate-to-source oxide breakdown on the switch device will degrade the performances of the SHA. In the sampling mode of the SHA, the gate leakage current of switch device is smaller than the charge current (I_D) of switch device current. In hold mode of the SHA, the extra gate leakage current of will discharge the stored charge in sampling capacitor to degrade the circuit performance of the SHA. The relationship between extra gate leakage current and stored charge of sampling ca-

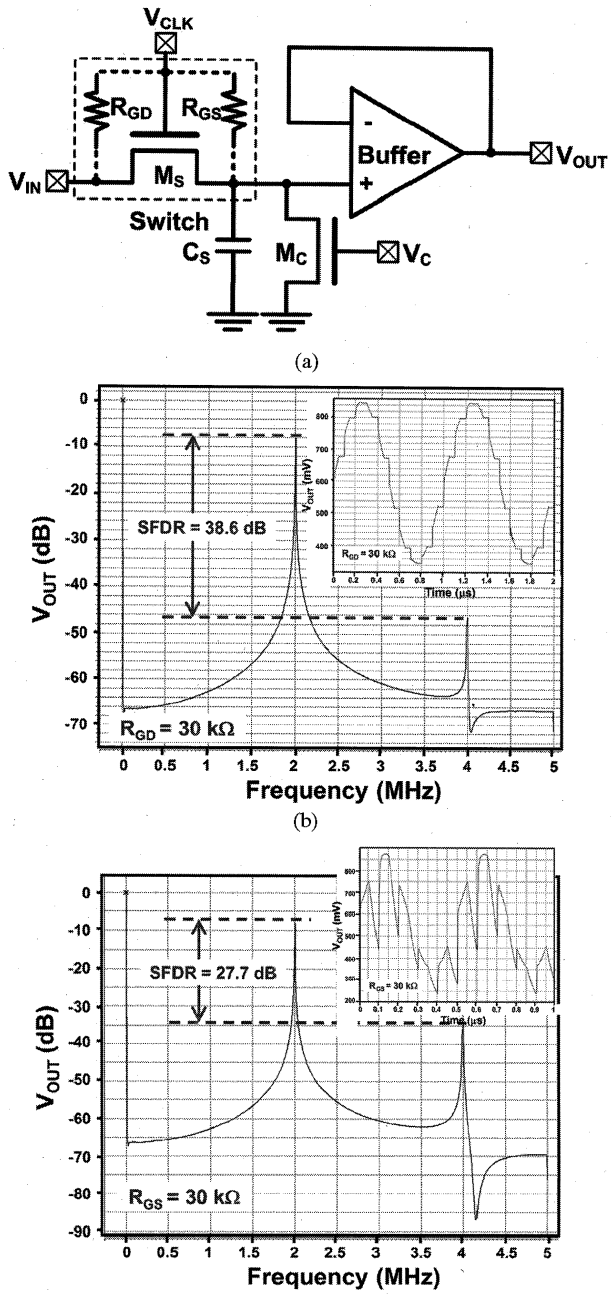

Fig. 9 (a) The sample-and-hold amplifier with the gate-oxide reliability test circuit including equivalent breakdown resistors R_{GD} and R_{GS}. The simulated frequency-domain and time-domain waveforms of the test circuit with equivalent breakdown resistors (b) R_{GD} and (c) R_{GS} of 30 kΩ, respectively.

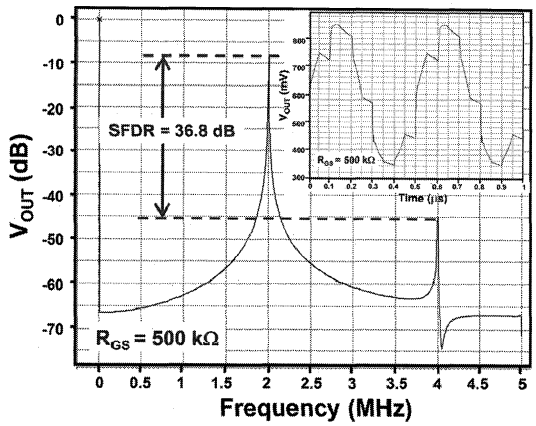

Fig. 10 The sample-and-hold amplifier with the gate-oxide reliability test circuit including equivalent breakdown resistors R_{GS}. The simulated frequency-domain and time-domain waveforms of the test circuit with equivalent breakdown resistors R_{GS} of 500 kΩ.

pacitor under the SHA operated in hold mode can be simple expressed as

$$\Delta V = \frac{Q_{\text{hold}}}{C_S} = \frac{C_S V_{\text{hold}} - I_{\text{G\_leakage}} T_{\text{hold}}}{C_S}, \quad (2)$$

where T_{hold} is the hold time ($2/f_S$, f_S sampling frequency), C_S is the sampling capacitor, Q_{hold} is a stored charge in sampling capacitor, V_{hold} is the ideal potential stored in sampling capacitor without oxide breakdown on the switch device under hold mode, and $I_{\text{G\_leakage}}$ is the extra gate leakage current of switch device due to gate-oxide breakdown. When the SHA operated in high sampling frequency, the gate-oxide breakdown on switch device has small impact on circuit performance. Therefore, the proposed SHA with the gate-oxide reliability test circuit can be used to verify the impact of gate-oxide breakdown on switched-capacitor circuit with bootstrapped switch technique.

In order to investigate the impact of soft gate-oxide breakdown on circuit performances of the switched-capacitor circuit with bootstrapped technique, the test circuit with equivalent breakdown resistor R_{GS} of 500 kΩ can be used to model the soft gate-oxide breakdowns on the switch device [14]. The simulated frequency-domain (10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node) and time-domain (10-MHz sampling frequency at V_{CLK} node and 1-MHz sinusoidal signal at V_{IN} node) waveforms of the SHA with equivalent breakdown resistor R_{GS} of 500 kΩ is shown in Fig. 10. The soft gate-oxide breakdown on the switch device also degrades the circuit performance of SHA. The soft and hard gate-oxide breakdown on a CMOS transistor will cause different extra gate leakage currents. The soft gat-oxide breakdown on a transistor causes a smaller extra gate leakage current than that of the hard gate-oxide breakdown in CMOS process [14]. Therefore, the soft and hard gate-oxide breakdown will have different impact on circuit performances of SHA. The hard gate-oxide breakdown has more serious impact on circuit performances than soft gate-oxide breakdown on switch device of switched-capacitor circuit with bootstrapped switch technique.

6. Conclusion

The impact of gate-oxide transient overstress on the MOS switch with bootstrapped technique has been investigated and analyzed with the sample-and-hold amplifier. The time-domain and frequency-domain waveforms of the SHA after different stress times have been measured. After the gate-oxide overstress, only the gate-to-source oxide breakdown on the switch device will degrade the performances of the SHA. The overstress time is related to the RC time constant ratio of the sampling and bootstrapping networks in the bootstrapped switch technique. The best solution of bootstrapped switch design is that the bootstrapped and sampling networks have the same RC delay times to avoid the transient gate-oxide overstress and to achieve the best performance. The hard gate-oxide breakdown has more serious impact on switched-capacitor circuit with bootstrapped technique.

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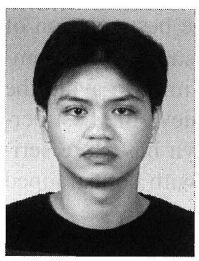

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