行政院國家科學委員會專題研究計畫成果報告

W-CDMA 基地台接收系統之初始擷取與多用戶偵測子系統之研究與實作

Study and Implementation of the Acquisition and Multiuser Detection Subsystem for W-CDMA systems

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執行期限： 90 年 8 月 1 日至 91 年 7 月 31 日
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I.　中文摘要

近年來，在第三代行動通訊系統中，寬頻多碼分工系統(W-CDMA)已經被廣泛使用在增加使用人數容量與傳送速度上。對於多碼分工系統來說，使用多使用者偵測(multiuser detection)技術可以增加使用人數容量，多使用者偵測有很多做法，在考量效能及實際實現之複雜度後，在本計劃中，我們提出一個寬頻分碼多工系統之全數位最小均方差(MMSE)多使用者偵測法。利用MMSE的運算法則能找到一個最佳之二級部分平行干擾消除(PIC)的部分消除因子(PCF)。在模擬的結果中顯示出，偵測的效能可以經由所導出的最佳PCF而有改善。最後，根據第三代行動通訊的規格，我們以FPGA的設計流程實現所提出來的接收機架構。

關鍵詞：

Abstract

Multiuser detection (MUD) is one of the techniques increasing the capacity of a DS-CDMA system. Many MUD algorithms have been proposed. Taking performance and implementation complexity into account, we propose a two-stage partial parallel interference cancellation (PIC) scheme in this project. We use the MMSE criterion to find the optimal partial cancellation factors (PCFs) for the two-stage partial PIC receiver. It is shown that the detection performance can be greatly enhanced using the derived optimal PCFs. The other advantage of the partial PIC approach is that the computational complexity is low. Then we propose an efficient hardware architecture and implement it using the FPGA design flow.

II.　計畫緣由與目的

Directly-sequence code-division multiple access (DS-CDMA) [1]-[2] has been considered as the standard transmission technique for the next generation mobile radio systems. In DS-CDMA systems, the code orthogonality property cannot always hold at the receiver due to the channel impairment. As a result, the multi-access interference (MAI) arises and this limits the capacity of the CDMA system. Thus, much research has been directed to solve this problem. Multiuser detector has been considered as the most promising technique. The optimal multiuser detector, which uses the maximum likelihood criterion, is difficult to implement due to its high computational complexity. Among the many suboptimal solutions, the PIC is considered as a good candidate for practical applications. However, the interference cancellation is not always reliable for the PIC. Thus the partial PIC scheme was proposed [20]-[22]. In the partial PIC approach, partial cancellation factors (PCFs) are introduced to control the interference cancellation level. However, the optimal PCE, which greatly influence the detection performance, cannot easily found. This project is aimed to solve the problem. We design a two-stage partial PIC receiver using the minimum mean square error (MMSE) criterion. The optimal PCFs can then theoretically derived. Using the optimal PCFs, we can significantly improve the detection performance. We also propose an efficient hardware architecture and this leads to an all-digital multiuser W-CDMA receiver. Finally, we use the FPGA design flow to implement the proposed receiver.

III. 研究方法與成果

Figure 1 is the structure of a two-stage partial PIC. Consider a K-user synchronous DS/CDMA system the received signal is expressed as

$$r(t)=\sum_{k=1}^{K}\sqrt{P_k}\left(d_{I,k}(t-\tau_k)+j*d_{Q,k}(t-\tau_k)\right)$$
$$\cdot\left(a_{1,k}(t-\tau_k)+j*a_{2,k}(t-\tau_k)\right)+n(t-\tau_k).$$

At the first stage the ith bit complex-valued decision metric of the kth user is given by

$$Z_k^{(1)}(i)=\sqrt{P_k}\,b_k(i)+\frac{1}{2N}\sum_{\substack{m=1\\m\neq k}}^{K}\sqrt{P_m}\,b_m(i)\,R_{mk}+\frac{\eta_k(i)}{2N}$$

where $b_k(i)$ is the ith bit of user k, P_k is the signal power, R_{mk} is the correlation function between user m and user k, and $\eta_k(i)$ is the noise term. At the second stage, the regenerated signal of user k is produced by

$$\hat{r}_k(t)=r(t)-C_k\sum_{\substack{j=1\\j\neq k}}^{K}\hat{s}_j(t),$$

where C_k is the PCF, and $\hat{s}_j(t)$ denotes the estimate of the jth interference and can be expressed as

$$\hat{s}_j(t)=a_j(t)\sum_{i=-\infty}^{\infty}\hat{d}_j(i)\left|Z_j^{(1)}(i)\right|\psi(t-iT_b)$$

Then the second-stage complex-valued decision metric $Z_k^{(2)}(i)$ can be obtained. The error signal $e_k(i)$ is defined as the difference between the user signal and $Z_k^{(2)}(i)$. Assume that the I and Q channel data sequence can be modeled as a sequence of independent and identically distributed random variables with equal probability. Then we form the mean square error (MSE) term as MSE=E{$e_k(i)\,e_k(i)^*$}. The optimal C_k can be determined by letting $\partial MSE/\partial C_k=0$. The MMSE PCF derived above requires knowledge of user powers, cross-correlations of signature sequences, and the noise variance. If a new user is added or dropped, the correlation matrix will change accordingly. Besides, the long scrambling codes of W-CDMA systems may make the correlation matrix to vary symbol by symbol. One way to reduce the computational complexity is to consider the signature sequence (including real and image part, i.e. $a_{1,k}(i)$, $a_{2,k}(i)$) as a random vector of length. Let the components of these vectors be independent and identically distributed random variables with equal probability. The correlation products can then be substituted by their expectation counterparts. The same procedures can be repeated to calculate $e_k(i)$ and MSE.

Differentiating MSE_k with respect to C_k and setting the result to zero, we can obtain the MMSE PCF for long codes as

$$C_k=\frac{N\left\{\sum_{\substack{m=1\\m\neq k}}^{K}P_m[N+K-2]+\frac{N_0}{8}(K-1)\right\}}{P_k[(K-1)(KN-1)]+\sum_{\substack{m=1\\m\neq k}}^{K}P_m\left[N^2+(K-2)(3N+K-3)\right]+\sum_{\substack{m=1\\m\neq k}}^{K}\frac{N_0}{8}[K-2+N]}$$

The partial PIC detector which uses the above PCF is called the random MMSE (RMMSE) PIC detector. If all users have equal power (under perfect power control), i.e., $P_1=P_2=\ldots=P_K$, then we have a simple result as

$$C_k=\frac{N\left\{(K-1)(N+K-2)+\frac{N_0}{8}(K-1)\right\}}{P_k[(K-1)(KN-1)]+(K-1)\left[N^2+(K-2)(3N+K-3)\right]+\frac{N_0}{8}(K-1)(K-2+N)}$$

Figures 3 and 4 show the performance comparison for the conventional and proposed detector. We can see that that the proposed algorithm performs much better than the matched filter.

The second part of this project is concerned about the FPGA implementation. The received consists of several functional blocks, i.e., (1) complex-valued multiplier, (2) pulse shaping filter, (3) chip matched filter, (4) interpolation filter, (5) the noncoherent DLL, and (6) the adder. We have proposed many efficient architectures to decrease the implementation complexity. Figure 2 is the detailed structure for the proposed receiver. Figure 4 is the RTL architecture for the proposed receiver.

IV. 結論

In this project, we have developed a two-stage MMSE partial PIC detector. The

PCF is derived based on the MMSE criterion. Using simulation results, we show that the proposed algorithm performs significantly better than the conventional matched filter and the two-stage full PIC receiver. We also propose a hardware architecture for the detector and implement it using the FPGA design flow.

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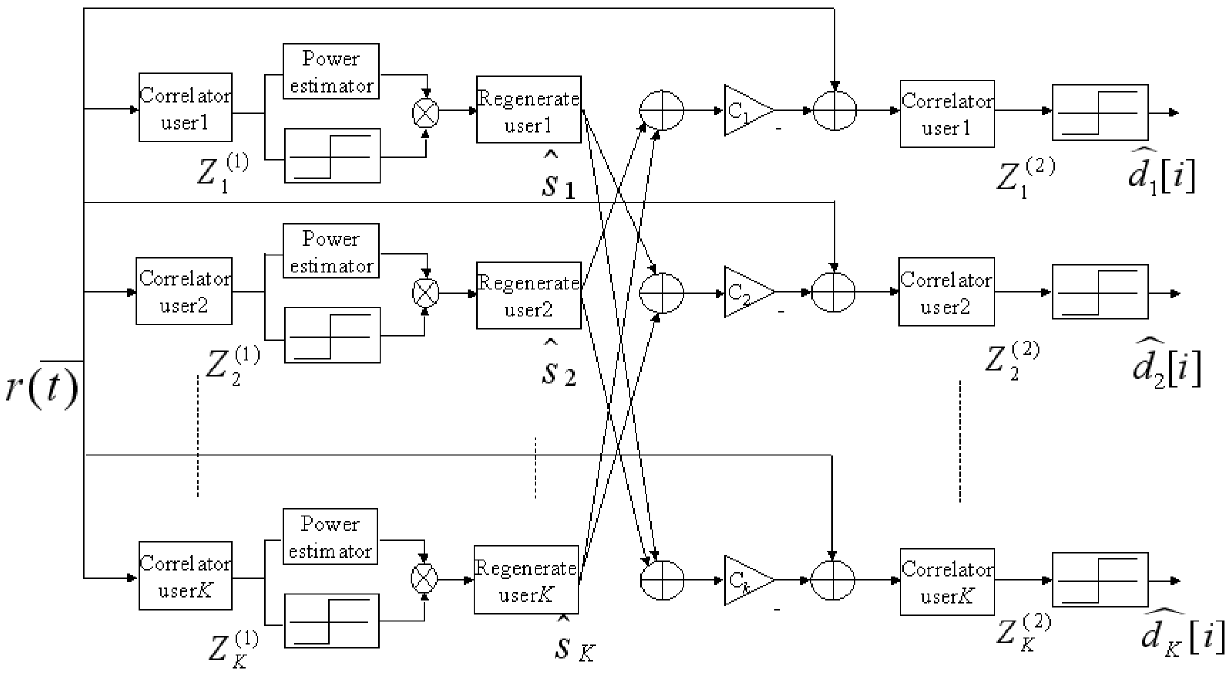

Figure 1. The partial PIC structure

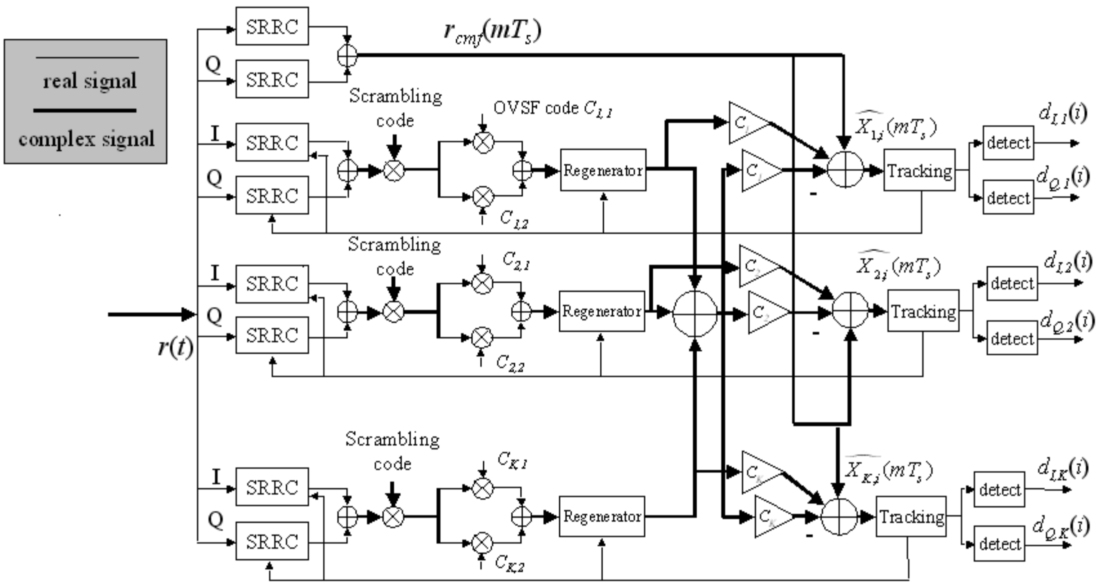

Figure 2. The partial PIC implementation structure.

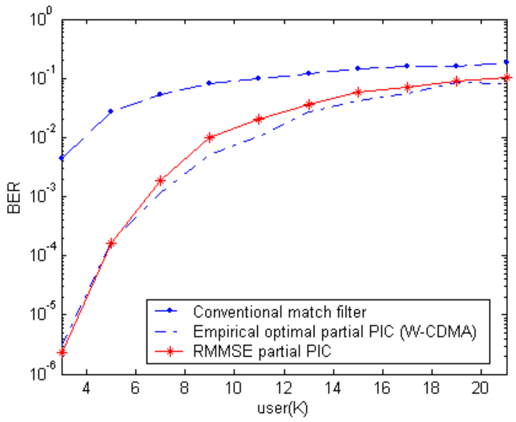

Figure 3. BER vs. user numbers (asynchronous, perfect power control, SNR=10 dB).

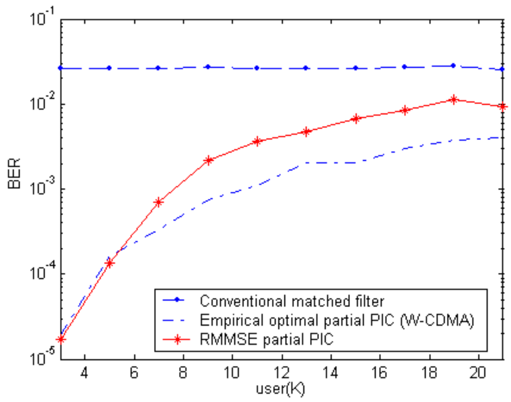

Figure 4. BER vs. user numbers (asynchronous, SNR=10 dB, SIR=-6 dB)

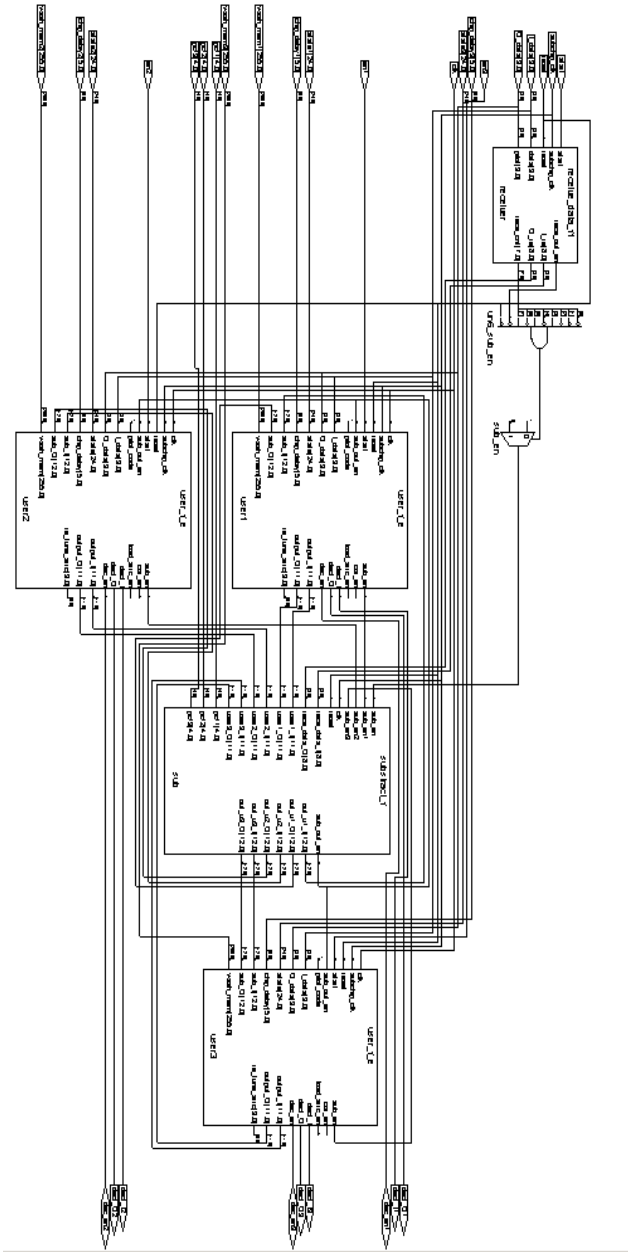

Figure 5. The RTL structure