Electrical Measurement of Local Stress and Lateral Diffusion Near Source/Drain Extension Corner of Uniaxially Stressed n-MOSFETs

Chen-Yu Hsieh, *Student Member, IEEE*, and Ming-Jer Chen, *Senior Member, IEEE*

***Abstract*—On a 1.27-nm gate oxide n-MOSFET that undergoes longitudinal stress via a layout technique, subthreshold current is measured as a function of the gate edge to shallow-trench isolation (STI) spacing and is transformed via bandgap shift into the source/drain extension corner stress. The extracted local stress is quantitatively comparable with those of the channel as created by the gate direct tunneling measurement in inversion, the mobility measurement, and the threshold voltage measurement. In addition, its dependencies on the gate edge to STI spacing confirm the validity of the layout technique in controlling the corner or channel stress. The gate edge direct tunneling (EDT) measurement in accumulation straightforwardly leads to the quantified gate-to-source/drain-extension overlap length. Particularly, a retarded diffusion length of 1.1 nm for a stress change of −320 MPa and the resulting strain-induced activation energy both are in satisfactory agreement with those of the process simulation. A physically oriented analytic model is, therefore, reached, expressing the lateral diffusion as a function of the corner stress.**

***Index Terms*—Dopant diffusion, mechanical stress, MOSFET, piezoresistance, shallow-trench isolation (STI), strain, tunneling.**

I. Introduction

MECHANICAL stress has been widely recognized to be one of the key issues in the area of highly scaled MOSFETs. So far, there have been two distinct directions concerning the significance of the mechanical stress. On the one hand, the mechanical stress experienced during the manufacturing process can enhance or retard the dopant diffusion, thereby influencing the final doping profile of the device. There have been significant studies with emphasis on the material aspect covering a wide range of experimental findings and confirmations [1]–[8], as well as the atomistic calculations and physical models [1], [9]–[12]. Extension to the actual devices has been achieved by means of the sophisticated device/process-coupled simulation, namely the technology computer-aided design (TCAD) [10], [13], [14]. On the other hand, the presence of the mechanical stress can also alter the band structure of the formed device, which, in turn, can significantly affect properties such as mobility [15]–[17], hot carrier immunity [18], threshold voltage [19], and gate direct tunneling [20]–[23]. Besides the aforementioned TCAD technique [10], [13], [14], there have been several methods applied on the formed devices with which the magnitude of the underlying stress and its status both can be determined: 1) wafer bending jig [24]; 2) stress/strain simulation and modeling [25]; 3) Raman spectroscopy [26]; and 4) gate direct tunneling [23].

Indeed, the ability of tracing the electrical measurements on the formed devices back to the stress-related dopant diffusion in the manufacturing process is essential. Traditionally, this was done with the TCAD method [10], [13], [14], as mentioned before. In this paper, we present the *electrical* approach to the local mechanical stress around the source/drain extension corner of uniaxially stressed n-MOSFETs, which can straightforwardly determine the underlying lateral diffusion. The validity of the proposed method will be addressed in detail.

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II. Device Under Study

The test device was an n^+ polysilicon gate n-MOSFET as fabricated in a state-of-the-art manufacturing process. The device process flow is depicted in Fig. 1. Also plotted in the figure is the schematic topside view of the test device. Three key process parameters were obtained by capacitance–voltage (C–V) fitting: n^+ polysilicon doping concentration $= 1 \times 10^{20}$ cm^{-3}, gate oxide thickness $= 1.27$ nm, and substrate doping concentration $= 4 \times 10^{17}$ cm^{-3}. In this process, the shallow-trench isolation (STI)-induced compressive stress was applied. The gate length along the $\langle 1\ 1\ 0\rangle$ direction is 1 μm large enough that the following effects can be effectively eliminated: external series resistance and short-channel or drain-induced barrier lowering (DIBL). The gate width has a large value of 10 μm, indicating that the transverse strain is relatively negligible. A layout technique was utilized to produce a variety of stress in terms of the gate edge to STI sidewall spacing, designated as a, with four values of 10, 2.4, 0.495, and 0.21 μm. A decrease in a means increased magnitude of longitudinal stress. Considerable number of contacts were formed on the source/drain diffusion along the gate width direction, far away from the STI in the $\langle 1\ 1\ 0\rangle$ direction. The spacing between the diffusion contact and the gate edge is fixed in this paper. With the source, drain, and substrate all tied to ground, the measured valence-band electron tunneling current in inversion (for the gate voltage V_G larger than the threshold voltage $V_{\rm th}$) or equivalently the substrate hole current was found to be unchanged, regardless of the stress. This indicates that the gate oxide thickness under study remains constant.

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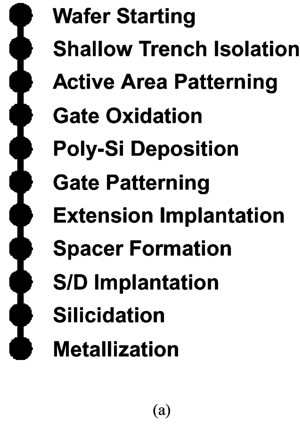
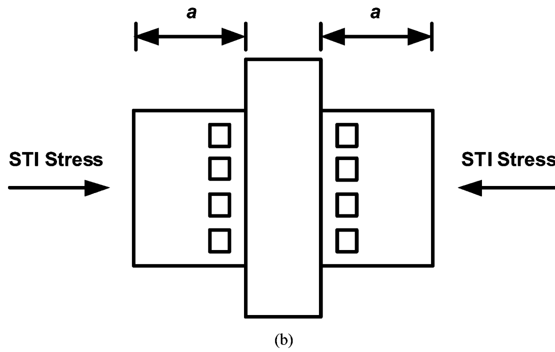


(a)



(b)

Fig. 1. (a) Device formation process flow. (b) Schematic topside view of the device. The gate edge to STI sidewall spacing a is highlighted. The stress condition is compressive due to the lower thermal expansion rate of STI oxide compared to silicon.

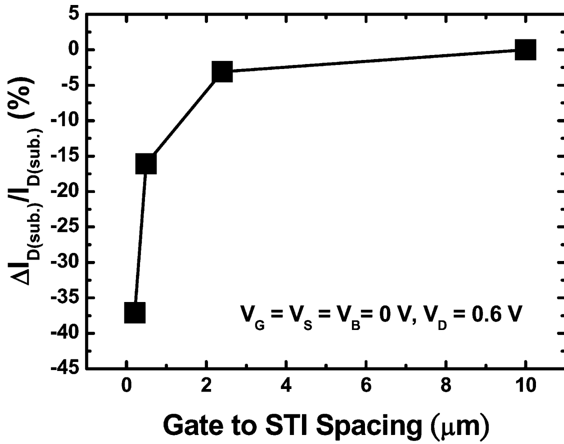


Fig. 2. Measured subthreshold current change versus gate-to-STI spacing.

III. Corner Stress Extraction and Validation

Measurement of the subthreshold current is adopted to quantify the mechanical stress around the source/drain extension diffusion corner. The measured subthreshold current change with respect to the reference device, namely $a = 10$ μm, is shown in Fig. 2, revealing a decreasing trend with decreasing gate-to-STI spacing. Since the mobility in depletion ($V_G < V_{\rm th}$) is primarily due to Coulomb scattering rather than phonon scattering, and hence is independent of stress, the subthreshold current must be proportional to n_i^2 only, where n_i is the intrinsic concentration. As a result, the change of the subthreshold current can be transformed into the bandgap change ΔE_g, as shown in Fig. 3. By means of a well-known relationship of $\Delta E_g = -3.66 \times 10^{-11} \sigma$ eV [19], the extracted ΔE_g further produces the source/drain extension corner stress of -20, -125, and -320 MPa for a of 2.4, 0.495, and 0.21 μm, respectively, as illustrated in Fig. 3.

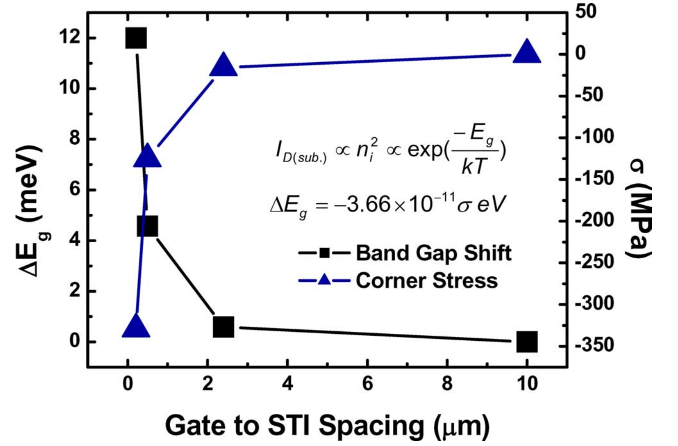


Fig. 3. Extracted bandgap change and source/drain extension corner stress versus gate-to-STI spacing.

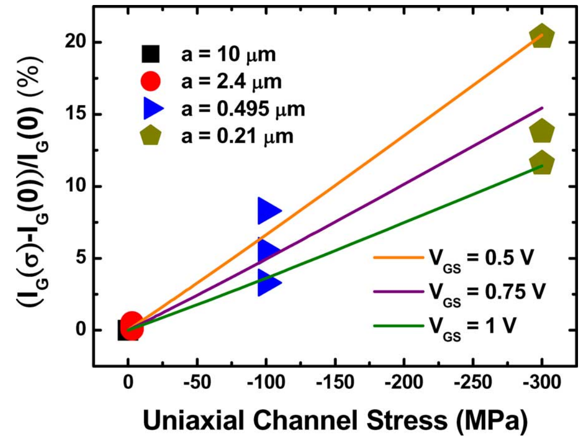


Fig. 4. Experimental gate current change percentage versus uniaxial channel stress with both gate-to-STI spacing and gate voltage as parameters.

The extracted corner stress is found to be comparable with those of the channel as created by other electrical measurements on the same device. First, by incorporating the stress dependencies of quantized energies [22], [23], [27]–[29] into a triangular potential method [30] in the channel, a Wentzel–Kramers–Brillouin (WKB) tunneling approach [31] was adopted to quantify the conduction-band electron direct tunneling current. As a consequence, the uniaxial channel stress of 0, $\sim$0, -100, and -300 MPa was extracted for gate-to-STI spacing of 10, 2.4, 0.495, and 0.21 μm, respectively, each of which can reproduce experimental gate direct tunneling current versus gate voltage characteristics. The detailed extraction process can be found elsewhere [23]. The corresponding gate current change is plotted in Fig. 4 versus extracted channel stress with gate voltage as a parameter. It was found that the twofold subband Δ_2

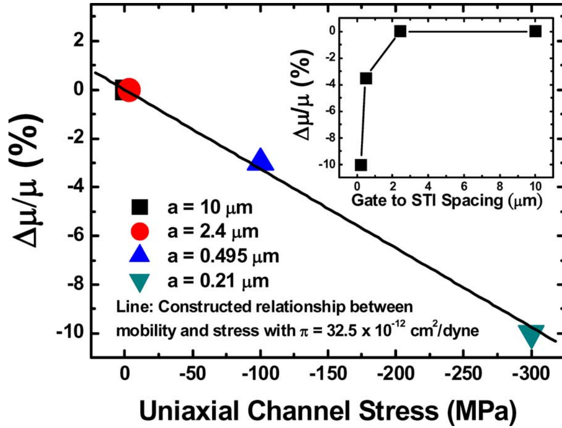


Fig. 5. Measured mobility change percentage versus extracted stress. The inset demonstrates the mobility variation versus gate-to-STI spacing.

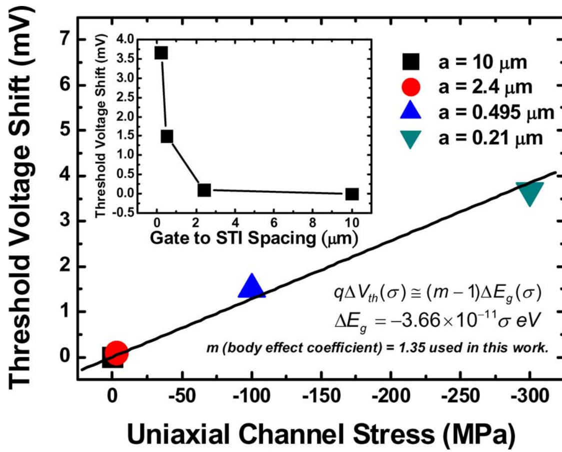


Fig. 6. Measured threshold voltage shift versus extracted stress. The inset shows the threshold voltage shift versus gate-to-STI spacing.

lies a few *kT* below the fourfold subband Δ_4 at high gate voltages, and therefore electrons primarily populate Δ_2, whereas for low gate voltages, electrons populate both Δ_2 and Δ_4. Hence, at low gate voltages, stress gives rise to not only a change in the barrier height but also an increased population in Δ_4. This effect becomes weakened for high gate voltages due to the dominating Δ_2 electrons. As a result, the gate current change due to the stress increases with decreasing gate voltage (refer to [22] for the detailed interpretations). Second, the mobility at $V_D = 25$ mV was characterized. The measured mobility change percentage versus extracted stress is shown in Fig. 5. A straight line used to fit the data points yields the slope or piezoresistance coefficient of 32.5×10^{-12} dyne^{-1} cm^2, close to that (31.5×10^{-12} dyne^{-1} cm^2) in the literature [32]. The inset depicts the corresponding mobility change as a function of the gate-edge-to-STI spacing. Third, the threshold voltage measurement was conducted at $V_D = 25$ mV. As shown in Fig. 6, the threshold voltage shift $\Delta V_{\rm th}$ produces a straight line of its own. This line can be related to the body-effect coefficient *m* and the band offset ΔE_g [19]: $q\Delta V_{\rm th}(\sigma) \approx (m-1)\Delta E_g(\sigma)$. The band offset term can further be linked to the strain ε [19]: $\Delta E_g = -6.19\varepsilon = -3.66 \times 10^{-11}\sigma$ eV. The slope of the line in

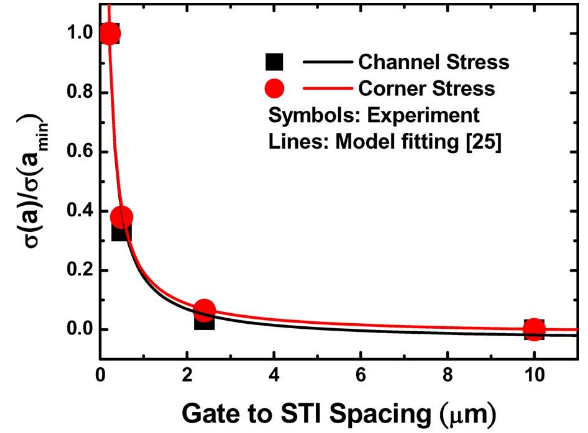


Fig. 7. Extracted channel and corner stress, divided by that of the minimum *a*, versus the gate-to-STI spacing, along with fitting curves from [25].

Fig. 6 furnishes $m = 1.35$, which exactly falls within the cited range of 1.3–1.4 [19].

Finally, to testify to the validity of the layout technique, we quote the existing relationship between the effective stress and the gate-to-STI spacing, which was derived from the stress simulation [25]

$$\sigma(a) = \sigma(a_{\min})\left(1 + V_{m\sigma}\frac{a - a_{\min}}{a}\right) \qquad (1)$$

where $a_{\min}$ represents the minimum gate-to-STI spacing and $V_{m\sigma}$ is the maximum $\sigma(a)$ variation (i.e., when $a \to \infty$) with respect to $\sigma(a_{\min})$. Evidently, as displayed in Fig. 7, the extracted channel stress and corner stress for a given gate-to-STI spacing are close to each other, indicating that the stress distribution beneath the gate oxide is considerably uniform. In addition, the corner stress follows the same trend as the channel counterpart. The resulting $V_{m\sigma}$ values are comparable as well: -1.04 for the channel stress and -1.02 for the corner stress. Good fitting quality in both stress cases confirms the validity of the layout technique in *controlling* the stress there.

IV. Lateral Diffusion Extraction and Confirmation

The electron direct tunneling from the accumulated polysilicon surface down to the underlying silicon was measured versus negatively biased gate voltage with the source, drain, and substrate all tied to the ground. It can be seen in Fig. 8 that the resulting substrate hole current, which essentially is equal to the electron gate-to-substrate tunneling current, increases with decreasing *a*. Such dependency reflects the increasing magnitude of lateral compressive stress in the polysilicon. The confirmative evidence of this origin is that for a given gate-to-STI spacing, the corner stress and channel stress both are comparable, and since the tunnel oxide is rather thin, the lateral compressive stress at the surface of the polysilicon is reasonably close to that of the underlying silicon. In contrast, the simultaneously measured source/drain or edge direct tunneling (EDT) current decreases with decreasing *a*, as shown in Fig. 9. To determine the underlying gate-to-source/drain-extension overlap length where the EDT prevails, the existing

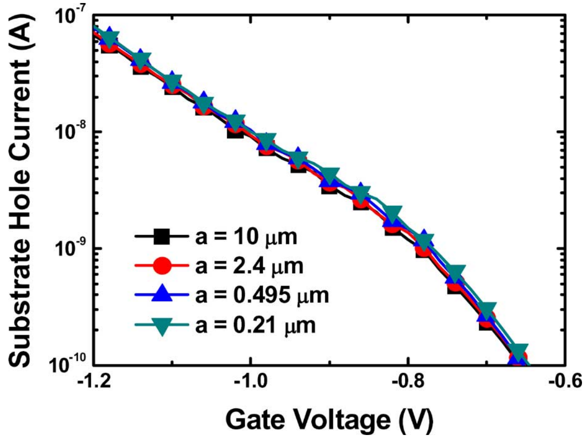
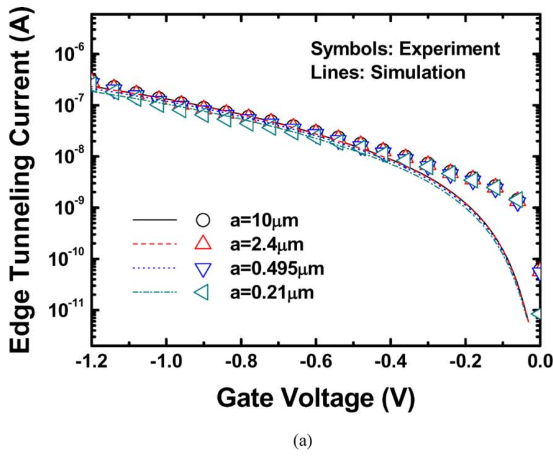
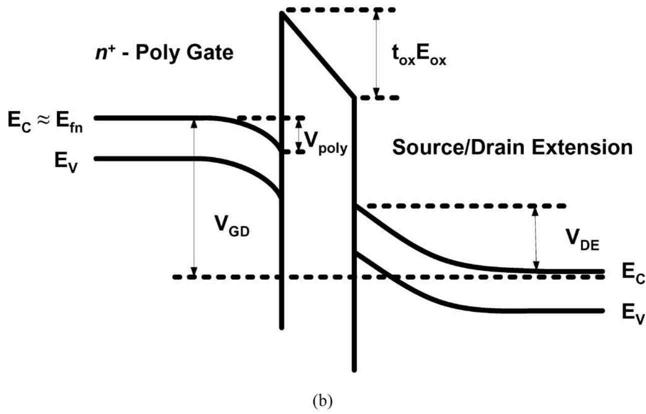


Fig. 8. Measured substrate hole current versus negative gate voltage.



(a)



(b)

Fig. 9. (a) Comparison of calculated and measured edge direct tunneling current versus negative gate voltage. (b) Band diagram drawn along n^+ polygate/SiO_2/diffusion extension.

edge direct tunneling models [33]–[35] on the basis of the triangular potential approximation [30] can readily apply with some slight modifications such as incorporating stress dependencies of the subbands in the accumulated polysilicon surface. First of all, the oxide field $E_{\rm ox}$ at the gate edge is determined through the following expression:

$$V_{\rm DG} - V_{\rm FB} = V_{\rm poly} + t_{\rm ox} E_{\rm ox} + V_{\rm DE} \tag{2}$$

where $V_{\rm DG}$ is the applied source/drain-to-gate voltage, $V_{\rm FB}$ is the flatband voltage, $t_{\rm ox}$ is the gate oxide thickness, and $V_{\rm poly}$ and $V_{\rm DE}$ are the potential drops in the n^+ polysilicon and source/drain extension region, respectively. The accumulated electrons mainly populate in the first subband E_1 due to the lowest quantized energy dominating. Then, relating the sheet charge density to the number of occupied subband states can establish the charge conservation relationship

$$q\left(E_{\rm fn} - E_1\right)\frac{\eta m_d}{\pi\hbar^2} = \varepsilon_{\rm ox} E_{\rm ox} = Q \tag{3}$$

where $E_{\rm fn}$ is the quasi-Fermi level in n^+ polygate, η is the degeneracy factor, and Q is the available charge for tunnel process. The corresponding stress dependency of the quantized energy is well defined in the literature [22], [23], [27]–[29]

$$E_1(\sigma) = \left(\frac{9hq\varepsilon_{\rm ox}E_{\rm ox}}{16\varepsilon_{\rm Si}\sqrt{2m_z}}\right)^{2/3} + \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11} + 2S_{12})\sigma + \left(\frac{\Xi_u}{3}\right)(S_{12} - S_{11})\sigma \tag{4}$$

where the elastic compliance constants $S_{11} = 7.68 \times 10^{-12}$ m^2/N and $S_{12} = -2.14 \times 10^{-12}$ m^2/N. The hydrostatic and shear deformation potential constants $\Xi_d = 1.13$ eV and $\Xi_u = 9.16$ eV [19], close to those of [22], were cited here. With the aforementioned parameters as input, the lowest subband level with respect to the Fermi level can be quantified. Employing the lowest subband approximation to the accumulated n^+ polygate and the deep depletion approximation to the source/drain extension region, as drawn in Fig. 9(b), the following expressions can, therefore, be derived:

$$V_{\rm poly} \approx \frac{E_{\rm fn}}{q} = \varepsilon_{\rm ox}E_{\rm ox}\frac{\pi\hbar^2}{q^2\eta m_d} + \frac{E_1}{q} \tag{5}$$

$$V_{\rm DE} = \frac{\varepsilon_{\rm ox}^2 E_{\rm ox}^2}{2q\varepsilon_{\rm Si}N_{\rm DE}} \tag{6}$$

where $N_{\rm DE}$ is the dopant concentration of the source/drain extension. Here, the quantization effective masses $m_z = 0.98\ m_0$ and $m_d = 0.19\ m_0$, and $\eta = 2$ were adopted to approximate the band structure for $\langle 1\ 0\ 0\rangle$ oriented polysilicon grain [31]. Then, it is a straightforward task to calculate the WKB tunneling probability, taking into account the corrections for reflections from the potential discontinuities [31]. Here, the electron effective mass in the oxide for the Franz-type dispersion relationship was used with $m_{\rm ox} = 0.61\ m_0$. The SiO_2/Si interface barrier height in the absence of stress is 3.15 eV. Consequently, the edge electron direct tunneling current density can be calculated as a function of the stress σ

$$I_{\rm EDT}(\sigma) = WL_{\rm TN}\frac{Q}{\tau_1(\sigma)} \tag{7}$$

where W is the channel width, and $L_{\rm TN}$ is the gate-to-source/drain-extension overlap length. The tunneling lifetime in this equation can be connected with the transmission probability T: $\tau_1(\sigma) = \pi\hbar/(T_1(\sigma)E_1(\sigma))$.

Then, with known process parameters and published deformation potential constants [19] as input, the measured EDT was

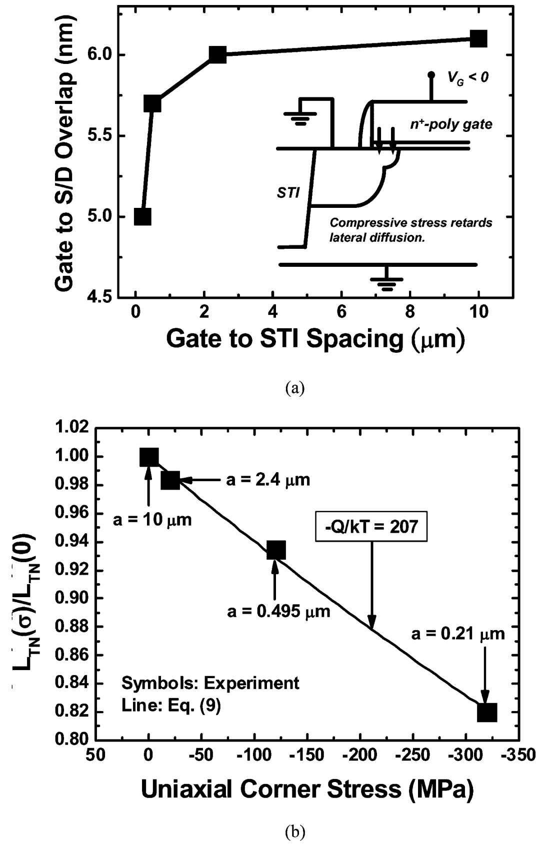


Fig. 10. (a) Extracted gate-to-source/drain extension overlap length versus gate-to-STI spacing. The decreasing trend with decreasing a can be related to the retarded lateral diffusion under the influence of the compressive stress. (b) Extracted (symbols) extension overlap length change versus corner stress. Also shown is a fitting line from (9).

reproduced well, as displayed in Fig. 9(a). Electron tunneling onto the forbidden silicon bandgap occurs in $-0.1\ \mathrm{V} < V_G < 0\ \mathrm{V}$; however, an appreciable gate current was measured there. This indicates the existence of the oxide traps or interface states. Only at a more negatively biased gate voltage where the EDT dominates can the effect of the traps be alleviated. In addition, it was found experimentally that the gate edge direct tunneling current is several orders of magnitude larger than the gate-to-substrate current, and hence is dominant over the gate voltage range of interest. The extracted gate-to-source/drain overlap L_{TN} spans a range of 6.1, 6.0, 5.7, and 5.0 nm for a of 10, 2.4, 0.495, and 0.21 μm, respectively, as demonstrated in Fig. 10(a). The L_{TN} values are found to be comparable with those in the literature [33]–[35]. The shift of around 1.1 nm, caused by retarded dopant lateral diffusion for stress change from 0 to -320 MPa, is reasonable with respect to the process simulation [13]. In the cited work [13], a device/process-coupled simulation was carried out to produce the lateral doping profile from the source through the channel to the drain, with and without the strain dependencies. The resulting doping profiles reveal the retarded diffusion of about 1.8 nm as caused by a stress change from -10 to -500 MPa. It is, therefore, inferred that the extracted local stress and lateral diffusion shift are in satisfactory agreement with those of the process simulation published elsewhere [13].

Finally, it is noticed that the gate-to-source/drain-extension overlap length designated L_{TN} is essentially proportional to the square root of the dopant diffusivity D. The stress-dependent dopant diffusivity can be expressed as [1], [4], [12]

$$D(\varepsilon) = D(0)\exp\left(\frac{-Q\varepsilon}{kT}\right) \tag{8}$$

where Q is the strain-induced activation energy and ε is the uniaxial strain. ε can be related to the uniaxial stress σ: $\sigma = Y\varepsilon$, where Y is the Young's modulus. Then, the effect of the stress on the extension overlap length can be derived

$$\frac{L_{\mathrm{TN}}(\sigma)}{L_{\mathrm{TN}}(0)} = \exp\left(\frac{-Q\sigma}{2kTY}\right). \tag{9}$$

The extracted extension overlap length is plotted in Fig. 10(b) versus the uniaxial corner stress. Fitting of the data yields a value of $-Q/kT = 207$. Assuming a typical temperature of $T = 1300$ K for the manufacturing process, the activation energy Q of -23.3 eV results, which is reasonable relative to those (-14 eV for arsenic and -30 eV for phosphorus) of the process simulation [13]. Therefore, a physically oriented analytic model is reached, expressing the lateral diffusion as a function of the corner stress.

V. Conclusion

With the aid of the layout technique, the source/drain extension corner stress has been, for the first time, extracted by using the subthreshold current measurement, and has been compared with the channel stress obtained by the additional measurements on the gate direct tunneling in inversion, mobility, and threshold voltage. The validity of the layout technique has been confirmed as well. With known process parameters and published deformation potential constants as input, fitting of the gate edge direct tunneling data has led to the value of the underlying lateral diffusion. The retarded lateral diffusion length and the strain-induced activation energy both have been quantitatively consistent with those of the process simulation. A physically oriented analytic model has been reached, expressing the lateral diffusion as a function of the corner stress.

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