Low Subthreshold Swing HfLaO/Pentacene Organic Thin-Film Transistors

M. F. Chang, P. T. Lee, S. P. McAlister, *Senior Member, IEEE*, and Albert Chin, *Senior Member, IEEE*

***Abstract*—We have integrated a high-κ HfLaO dielectric into pentacene-based organic thin-film transistors. We measured good device performance, such as a low subthreshold swing of 0.078 V/dec, a threshold voltage of -1.3 V, and a field-effect mobility of 0.71 $\mathrm{cm^2/V \cdot s}$. This occurred along with an ON–OFF state drive current ratio of 1.0×10^5, when the devices were operated at only 2 V. The performance is due to the high gate-capacitance density of 950 nF/cm^2 that is given by the HfLaO dielectric, which is achieved at an equivalent oxide thickness of only 3.6 nm with a low leakage current of 5.1×10^{-7} A/cm^2 at 2 V.**

***Index Terms*—HfLaO, high-κ, organic thin-film transistors (OTFTs), subthreshold swing (SS).**

I. Introduction

POLY-Si thin-film transistors (TFTs) [1]–[6] are currently used for active matrix liquid crystal displays on glass substrates. These poly-Si TFTs are operated in inversion mode, and the ion implantation for the n$^+$ source–drain requires activation at 600 °C, which is typically for ~12 h. This extended annealing slows down the process sequence, and the large thermal budget is unfavorable for environment energy conservation. In contrast, organic TFTs (OTFTs) [7]–[9] can be processed with a significantly lower thermal budget and without requiring ion implantation or an extended dopant activation period. This is because the OTFTs can be operated in the accumulation mode, where Schottky source–drain contacts [10] are used rather than ion-implanted n$^+$ source–drain regions. Unfortunately, for OTFTs, their low hole mobility and poor subthreshold swing (SS) limit the drive current when operated at low voltage [7]–[9]. The poor SS leads to inverters being slow when used in logic circuits. In this letter, we report using high-κ HfLaO [11]–[13] as the gate dielectric for OTFTs, with the aim of addressing the aforementioned issues. In addition to displaying a high-κ value of up to 24, HfLaO permits low-temperature processing due to the strong metal–oxide bond enthalpy of both Hf–O and La–O [14]. The addition of LaO into HfO is particularly important to decrease the leakage current at low-temperature process due to the larger conduction band offset of La_2O_3 (2.3 eV to Si) than that of HfO_2 (1.5 eV to Si) [15]. The HfLaO MOSFET also shows less Fermi-level pinning than using HfO_2 [11]–[13]. Our HfLaO/pentacene OTFTs showed a low SS of only 0.078 V/dec, a high gate capacitance density of 950 nF/cm^2, a low threshold voltage V_T of -1.3 V, a good mobility μ_{FE} of 0.71 $\mathrm{cm^2/V \cdot s}$, and a large ON–OFF state drive current ratio $I_{\mathrm{on}}/I_{\mathrm{off}}$ of 1.0×10^5. This superior performance permits the devices to be operated at 2 V, which could be useful for display applications.

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II. Experimental Details

The devices were fabricated on a thick SiO_2 layer grown on Si wafers to mimic poly-Si TFTs fabricated on glass substrates [2]. A 50-nm-thick TaN gate electrode was then deposited on the SiO_2/Si, through a shadow mask, using reactive sputtering. The surface of the TaN gate was subsequently treated with an NH_3 plasma to improve the gate leakage current [15]–[17]. Such nitrogen plasma treatment is the key factor to achieve low leakage current and small equivalent oxide thickness (EOT) in previous dynamic random access memory capacitors [15]–[17]. The 20-nm-thick HfLaO gate dielectric was then deposited by electron beam evaporation and annealed in O_2 at 350 °C for 10 min. Next, pentacene (Aldrich Chemical Company) was evaporated through a shadow mask onto the sample to form an active layer that is 70 nm thick. This evaporation was performed at a deposition rate of 0.5 Å/s at 70 °C, under a pressure of 3×10^{-6} torr. Finally, Au source–drain electrodes, which are 50 nm thick, were deposited onto the pentacene. The devices had a channel length of 80 μm and a width of 2000 μm. We also deposited Au directly onto HfLaO/TaN to make 200×200 μm^2 capacitors to analyze the dielectric properties. The devices were characterized using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter, under dark and air ambient conditions.

III. Results and Discussion

In Fig. 1(a) and (b), we show the schematic diagram of OTFT and C–V (inset: J–V) characteristics of Au/HfLaO/TaN capacitors, respectively. The data indicate a leakage current of 5.1×10^{-7} A/cm^2 at 2 V, at a capacitance density as high as 950 nF/cm^2. This gives an EOT of only 3.6 nm and a high-κ value of 21.7. Such a low leakage current at 2 V is better than that of the previous high-κ $LaAlO_3$ poly-Si TFTs, which had

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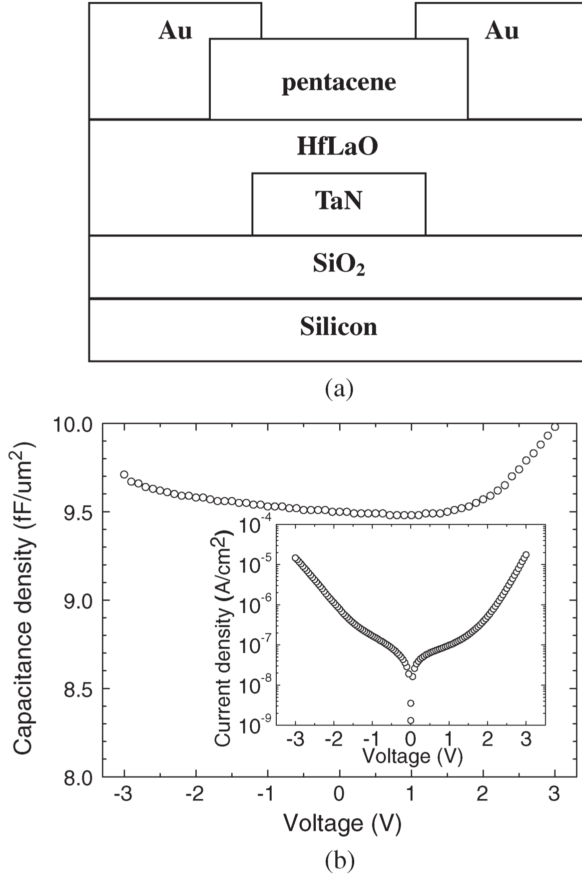

Fig. 1. (a) Schematic diagram of the high-κ HfLaO/pentacene OTFTs. (b) C–V (inset: J–V) characteristics of Au/HfLaO/TaN capacitors.

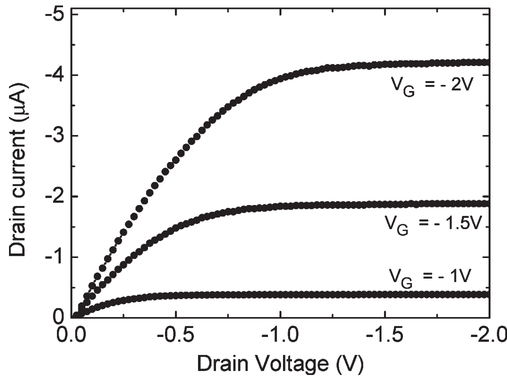

Fig. 2. Output characteristics (I_D–V_D) for a HfLaO gate dielectric OTFT.

a lower capacitance density of 390 nF/cm^2 (8.7 nm EOT) and involved annealing at 400 °C for 30 min [6]. These observations point to the merit of using HfLaO as the gate dielectric.

The output characteristics of a high-κ HfLaO/pentacene OTFT are displayed in Fig. 2. The I_D–V_D characteristics are well behaved and suggest possible operation at 2 V, which has the advantage of reducing the power consumption $(I_D \times V_D)$ in circuit operations. The transfer characteristics $(I_D$–$V_G)$, as shown in Fig. 3, enable the extraction of the mobility and V_T from the $-I_D^{1/2}$ versus V_G plot. This device shows a record low SS of 0.078 V/dec, a V_T of -1.3 V, and a good $\mu_{\rm FE}$ of

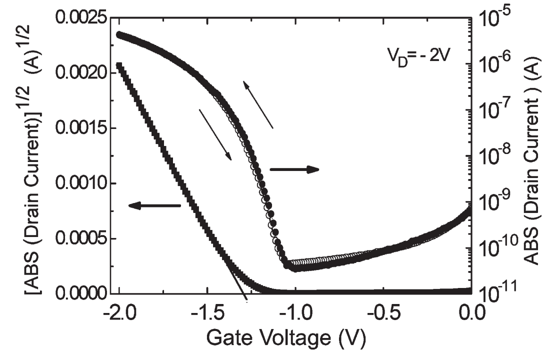

Fig. 3. Transfer characteristics $(I_D$–$V_G)$ and $-I_D^{1/2}$–V_G of a HfLaO gate dielectric OTFT at $V_D = -2$ V. The data point is spaced to only 0.0125 V to ensure the good accuracy of SS calculation. The resolution setting and noise in the measurement system are 10 pA and smaller than 100 fA, respectively.

TABLE I
COMPARISON OF p-CHANNEL HfLaO/PENTACENE OTFTs WITH n-CHANNEL POLY-Si TFTs

	HfLaO	LPCVD SiO_2	PECVD TEOS oxide	PECVD TEOS oxide
Gate dielectric	20 nm	80 nm [3]	60 nm [4]	40 nm [5]
Conduction channel	thermally evaporated pentacene	poly-Si by SPC	poly-Si by SPC	poly-Si by SPC
C_i (nF/cm^2)	950	43.1	57.5	86.3
V_T (V)	-1.3	5.6	8.14	Not extracted
μ_{FE} (cm^2/Vs)	0.71	20	12.44	3
SS (V/decade)	0.078	1.4	1.97	2.67
$\mu_{FE}C_i$ (nF/cm^2)	674.5	862.8	715.7	258.8
I_{on}/I_{off}	1.0×10^5	3.5×10^5	2.97×10^5	Not extracted

0.71 cm^2/V · s, along with an $I_{\rm on}/I_{\rm off}$ as high as 1.0×10^5. To analyze the low SS, we used the following relationship:

$$SS = \frac{KT}{q} \times \ln 10 \times \left(1 + \frac{C_{\rm dep} + C_{\rm it}}{C_i}\right) \qquad (1)$$

where $C_{\rm dep}$ is the depletion capacitance density of pentacene, $C_{\rm it}$ is the capacitance density from charged interface traps, and C_i is the gate capacitance density. Here, the SS controls the ON-to-OFF voltage swing, which should be as low as possible for high-speed and low-voltage operation. The SS of only 0.078 V/dec is better than that for poly-Si TFTs [1]–[6] and OTFTs [7]–[9] and is close to the theoretical minimum value of 0.06 V/dec at room temperature. We attribute these results to the high C_i of 950 nF/cm^2 and the small EOT of 3.6 nm, resulting from the use of advanced high-κ HfLaO dielectric that is even processed at low temperature. In addition, a small hysteresis of 15 mV is measured, showing the good HfLaO quality even when processed at low temperature.

The important device parameters are detailed in Table I, where the data from the conventional n-channel poly-Si TFTs using solid phase crystallization (SPC) and low-pressure

chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD) oxides [3]–[5] are included for comparison. Note that the $\mu_{\mathrm{FE}}C_i$ term is directly related to I_D $(W/2L_G \times \mu_{\mathrm{FE}}C_i\ (V_G - V_T)^2)$, which is normalized to the channel length L_G, channel width W, and overdrive voltage of $V_G - V_T$. The performance of our HfLaO OTFTs is comparable with that of poly-Si TFTs, which incorporate LPCVD and PECVD tetra-ethyl-ortho-silicate (TEOS) oxides [3]–[5], but with the additional merits of a better SS, lower V_T, faster process sequence, and lower thermal budget process.

IV. Conclusion

We have fabricated and characterized low-voltage OTFTs that incorporate high-κ HfLaO as the gate dielectric. These devices exhibit good electrical characteristics such as a low SS, a small V_T, and a large $\mu_{\mathrm{FE}}C_i$.

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