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Materials Chemistry and Physics 107 (2008) 471–475
MATERIALS CHEMISTRY AND PHYSICS
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Effectiveness of Si thin buffer layer for selective SiGe epitaxial growth in recessed source and drain for pMOS

P.L. Cheng [a,b,*], C.I. Liao [a], C.C. Chien [a], C.L. Yang [a], S.F. Ting [a], L.S. Jeng [a], C.T. Huang [a], Osbert Cheng [a], S.F. Tzou [a], W.S. Hsu [b]

[a] *United Microelectronics Corp., Tainan Science Park, Tainan County 741, Taiwan, ROC*
[b] *National Chiao Tung University, Hsinchu City 30050, Taiwan, ROC*

Received 31 May 2007; received in revised form 14 August 2007; accepted 17 August 2007

Abstract

Locally strained Si technology using embedded SiGe has been used to improve pMOSFET device performance through hole mobility enhancement. Embedded SiGe is achieved by selectively growing epitaxial SiGe film in recessed Si pMOSFET source and drain areas. Prior to selective SiGe epi growth, a thin layer of Si seed was employed to help nucleate following low-temperature selective SiGe epitaxial film in recessed source and drain areas. In combination with pre-epi wet clean and low-temperature chemical bake, use of Si seed resulted in improved SiGe film morphology and micro-loading effect, and further improved device performance.
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Keywords: Epitaxial growth; Dislocations; Surfaces; Semiconductors

1. Introduction

Locally strained Si technology using embedded SiGe has been demonstrated to improve pMOSFET device performance through hole mobility enhancement [1–3]. Widely used, embedded SiGe is achieved by selectively growing epitaxial SiGe film in recessed Si pMOSFET source and drain areas. Prior to the selective SiGe deposition step, device wafers go through gate formation, spacer formation, multiple implants (e.g. LDD, halo, and HDD), anneal, etc. Typical process steps and the impact of process sequence for recessed source and drain SiGe application are described elsewhere [2]. Reactive ion etch used in recessed source/drain formation, and photo resists strip prior to selective SiGe deposition result in physical damage and chemical residues on the film growth surface. Growth surfaces free of damage and chemical contaminants are required to obtain high quality SiGe epi films. Non-ideal surface conditions lead to film nucleation difficulties and prevent smooth film growth in mild cases and film growth in severe cases.

Typically, wet clean (in diluted HF) or high temperature bake (>800 °C) is used as a pre-epi step to remove surface C and O. A previous study [4] indicated improvement of SiGe film morphology by multiple cycles of wet clean in ozonated DI/SC1/DHF. But the bake temperature cannot exceed the thermal budget of the device wafer. Besides, Si migration is a concern for high temperature bake. For the harshest surfaces with severe damage caused by implant and dry etch and limitation of process window, use of a silicon seed layer is employed to nucleate uniform SiGe film with good quality and to minimize the micro-loading effect. Device performance without degradation is also discussed in this paper.

2. Experimental

The experimental wafers were prepared by a 300 mm single-wafer CVD reactor operating at reduced pressure. The process tool contains vacuum load locks to prevent the wafers from being exposed to air prior to processing.

The Ge and boron doping sources are GeH_4 and B_2H_6, respectively, and H_2 is used as the carrier gas. The wafers are treated by diluted DHF clean followed by a low temperature H_2 bake prior to SiGe epi film growth. The growth temperature is below between 600 and 750 °C at reduced pressure (5–20 Torr) for both Si seed and SiGe. A thin Si seed is deposited in the source/drain region prior to in situ boron-doped SiGe film growth. The Si seed layer thickness is around 10–30 A, and SiGe thickness is around 800–1200 A with around 15–30% Ge concentration. Fig. 1 shows the fabrication flow with evolution scheme (with Si seed layer) and TEM view of pFET with SiGe.

* Corresponding author at: United Microelectronics Corp., No. 18, Nanke 2nd Rd., Tainan Science Park, Sinshih Township, Tainan County 741, Taiwan, ROC. Tel.: +886 6 505 4888x12472; fax: +886 6 505 0960.
E-mail address: po_lun_cheng@umc.com (P.L. Cheng).

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doi:10.1016/j.matchemphys.2007.08.020

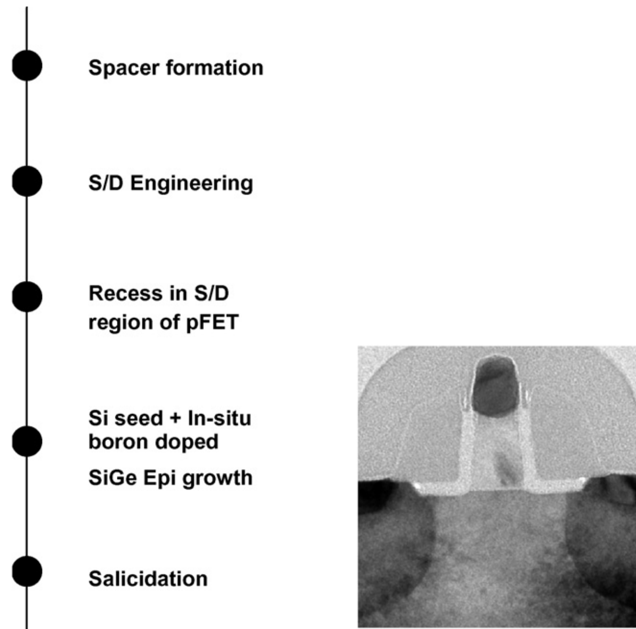

Fig. 1. Process flow with Si seed and TEM view of pFET with SiGe.

The film morphology and thickness are identified by spectroscopic ellipsometer and transmission electron microscopy (XTEM). The Ge content, boron concentration and doping profile in SiGe film are measured using secondary-ion mass spectrometry (SIMS). Atomic force microscopy (AFM) is used to observe the surface roughness.

3. Results

3.1. SiGe growth characteristics

Prior to SiGe deposition, device wafers were cleaned in diluted HF (DHF). Wafers were introduced to the reaction chamber for low-temperature bake followed by selective deposition of Si seed and SiGe film in recessed pMOS source and drain areas. A control wafer was processed with similar pre-epi wet clean, bake, and deposition without the seed layer. Wafers with severe surface damage did not yield SiGe film growth of good morphology without the seed layer. However, wafers with surface damage showed a difference in SiGe film morphology between wafers with and without the Si seed, as shown in Fig. 2. Improved surface morphology is observed in the clear faceting and lack of dislocations around the lateral recessed interface in the case with the Si seed. Also, the surface roughness recovered well in the different density area of the wafer with Si seed, further improving micro-loading with a similar incubation time. Micro-loading between the isolated area and dense area was improved 92% once the Si seed layer was applied. Micro-loading was defined as (maximum thickness − minimum thickness)/minimum thickness in the same die.

Roughness analysis by AFM shows that we can obtain better roughness in epi film with Si seed. The rms value is 0.188 nm for epi film with Si seed, and 0.481 nm for epi film without Si seed. The AFM images are in Fig. 3. It also indicates the Si seed process can recover initial surface roughness and further improve the epi roughness.

Furthermore, Si seed not only decreased the micro-loading effect, it did so without SiGe quality degradation. Since the Si seed is an undoped Si layer, the depletion region is of concern, but the SIMS profile, shown in Fig. 4(a), reveals the boron dopant diffused to this thin layer by the following process, and the junction depth can be controlled well by this kind of Si layer. Fig. 4(b) shows the boron profile without Si seed increased 30–50 A junction depth, which is compared with the profile of Si seed.

3.2. Device characteristics

Electrical data tested by $V_{cc} = -1$ V shows the Si seed layer suppresses boron out-diffusion from subsequent thermal steps, thus further resulting in better short channel control. Fig. 5 shows that a device with Si seed has a better roll-off curve than one without Si seed, which shows 8% C_{ov} (overlap capacitance) increase caused by boron out-diffusion. This allows us to optimize the thickness of the Si seed layer to control boron out-diffusion and decrease short channel effect at the same time. In addition, Fig. 6 shows I_{on}–I_{off} characteristics of SiGe pFET devices

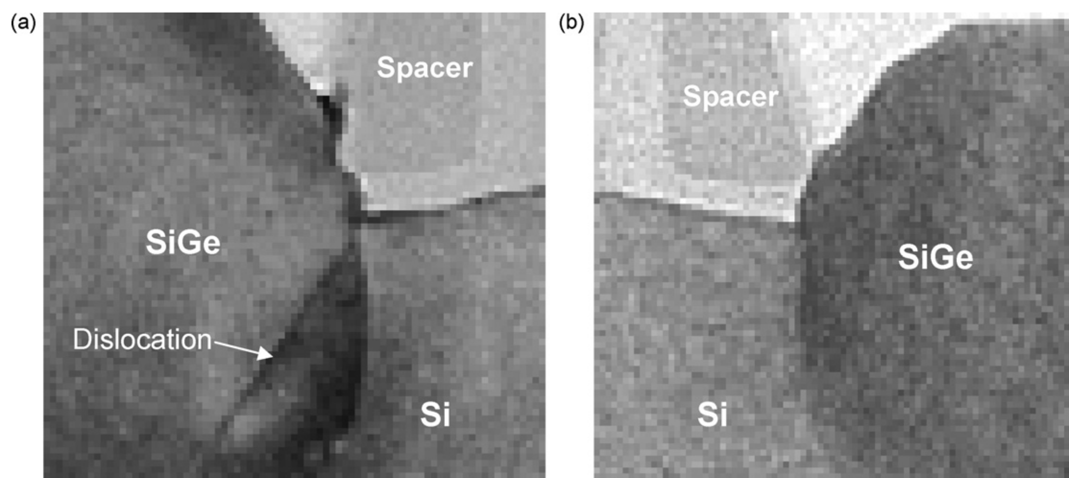

Fig. 2. XTEM comparison of selectively grown SiGe film (a) without and (b) with Si seed.

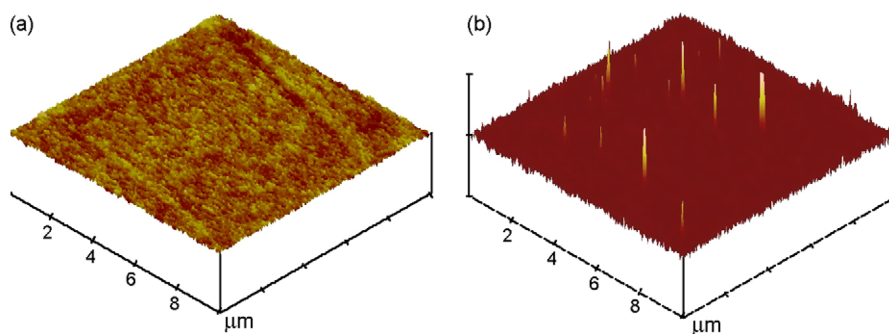

Fig. 3. SiGe roughness (a) with and (b) without Si seed.

with Si seed layer. A 32% saturation current enhancement is achieved at 100 nA μm^{-1} I_{off} with its additional compressive local strain.

4. Discussion

Normally, SiGe film can be deposited on Si and dielectric surfaces. It is called epitaxial SiGe film when SiGe is deposited on Si surface. In addition, when SiGe is deposited on dielectric film, such as oxide film, poly SiGe film is formed. To obtain selective growth, just epitaxial SiGe is deposited on the Si surface but no poly SiGe film is deposited on the oxide surface. Finally, we need a kind of etching source to remove poly SiGe on oxide film to achieve selective epitaxial SiGe growth. HCl is a choice to achieve this purpose. Basically, HCl gas can both etch epitaxial SiGe on Si and poly SiGe on oxide. Although both kinds of SiGe film can be etched by HCl, the etch rate is quite different. The etch rate of poly SiGe is about four times faster, compared with epitaxial SiGe under the same HCl condition, which means selectivity can be achieved.

The HCl gas not only causes the selective SiGe epitaxial growth, but also helps to passivate a Si–Cl layer. Regardless of the Si seed layer proposed in this paper or in situ boron-doped SiGe film growth, the HCl gas is necessary to obtain selective growth and the adsorption of Cl-based species makes Si nucleation on oxide more difficult, which makes the SiGe growth rate on oxide lower than on the Si surface.

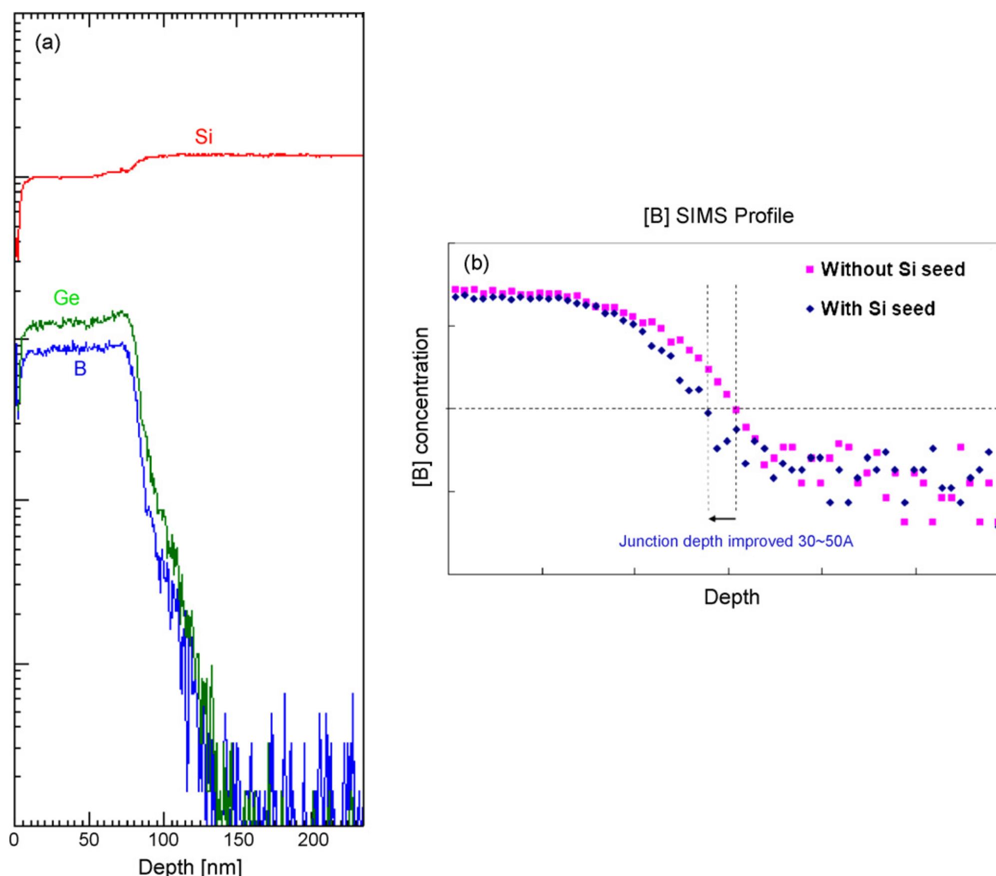

Fig. 4. SIMS profile (a) SiGe:B film with Si seed, (b) boron profile comparison between SiGe:B film with and without Si seed.

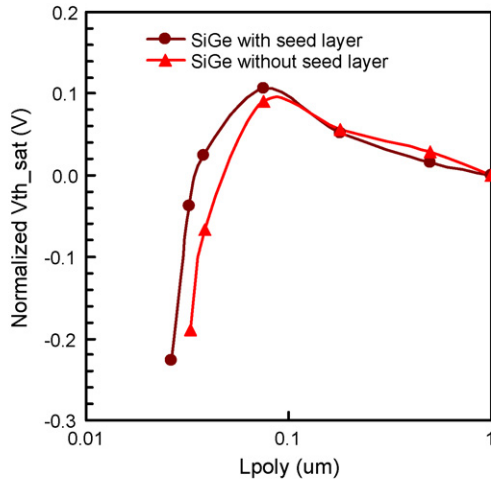

Fig. 5. V_{th} vs. L_{poly}. SCE is improved by Si seed.

In this work, the surface is passivated with Cl atoms prior to in situ boron-doped SiGe film growth since the Si seed layer is deposited with HCl gas for selective growth. However, the addition of HCl reduces the growth rate and leads to the growth mechanism changing from mass-transport-like to surface-reaction-like [5]. Since the reaction is switched to surface-reaction-like, the micro-loading is minimized too.

Comparing the growth rate of epitaxial SiGe on a surface with and without Si seed layer, the growth rate of epitaxial SiGe is reduced once the Si seed layer is implemented due to the larger surface coverage of Cl-based species, which saturate the adsorption sites, thus disturbing the adsorption of Si atoms [6]. That is why the growth rate of epitaxial SiGe with Si seed layer is lower than of the one without the Si seed layer. Our data shows the growth rate of the film with Si seed is 25% slower than without Si seed. But if a high temperature bake is inserted between Si seed and SiGe growth, the growth rate of the films with and without Si seed is equal since the Cl atoms on Si surface are desorbed. Normally, a lower growth rate decreases pattern sensitivity because gas phase reaction length is increased, which enhances surface reaction (decreased surface reaction length), which also explains why micro-loading is minimized.

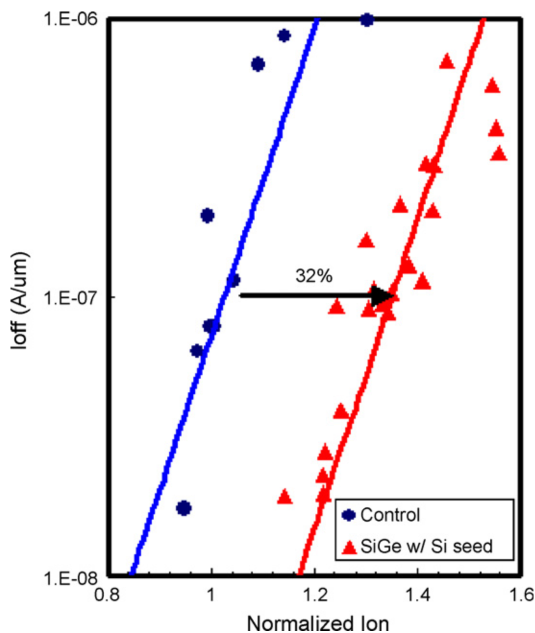

Fig. 6. pFet I_{on}–I_{off} characteristics. A 32% I_{on} current gain is achieved at $I_{off} = 100\,\text{nA}\,\mu\text{m}^{-1}$.

As mentioned above, epitaxial SiGe film without Si seed has a higher growth rate than with Si seed, which means higher atom mobility is achieved. Then, high atom mobility during processing results in poor surface roughness [7]. We implement the Si seed layer to reduce surface mobility of atoms, and the resulting film has less surface roughness. Besides, the Si seed layer also can recover surface roughness that comes from previous process steps, such as multiple implants, reactive ion etch used in recessed source/drain formation, and photo resists strip prior to selective epi growth. HCl plays an important role here because HCl can etch Si slightly. The mixing process combined with the etch of HCl and the growth of the Si seed layer will recover the surface from rougher to smoother prior to epitaxial SiGe growth. Although HCl is also used for the epitaxial SiGe growth step, the lattice mismatch between SiGe and Si will make the growth more difficult if the SiGe is deposited on a rougher surface directly without Si seed.

However, HCl has not been suggested for use with long time and high flow conditions, even though this kind of process shows more selective behavior. But the more selective process will lead to another side effect because HCl also can etch oxide film even though the etch rate is very low. In the integrated CMOS device with selective SiGe epitaxial growth process for pMOSFET, oxide or nitride film is often used as a protective layer on nMOSFET. If the protective layer is damaged by HCl, the epitaxial SiGe will be deposited on unexpected areas.

That selective epitaxial SiGe can introduce higher strain into the channel region and reduce source/drain extension resistance has been addressed [8,9]. To reduce extension resistance, the in situ boron concentration in SiGe should be raised. However, higher boron concentration will lead to boron out-diffusion during the thermal treatment process subsequently, and further increase junction depth and degrade short-channel effect. To solve this kind of challenge, Si seed layer is proposed in this paper. The electrical results show boron can be suppressed by implementing Si seed layer since the C_{ov} is decreased about 8% and has better short-channel control. Moreover, Ge incorporation results in compressive strain in the Si channel region. The effect shows 32% saturation current enhancement at $100\,\text{nA}\,\mu\text{m}^{-1}$ I_{off}. Normally, higher Ge concentration in SiGe causes more I_{on} gain due to more strain in the channel, but makes growth in the Si surface more difficult due to the increased lattice mismatch between SiGe and Si. As we discussed above, the Si seed layer can recover surface roughness and cause SiGe growth with higher Ge concentration. Since the Si seed layer is deposited at low temperature, the device performance is not degraded by that. Besides, this film thickness is optimized to suppress boron out-diffusion, prevent depletion layer creation, and further improve short channel effect.

5. Conclusion

With an optimal wet clean process, a uniform layer of SiGe film was selectively grown in recessed source and drain areas with and without seed. However, the best SiGe epi morphology was obtained with use of Si seed prior to SiGe deposition. Use of a silicon seed layer also led to improved micro-loading, resulting in better control of SiGe film thickness. A thin layer of Si seed was implemented in selective SiGe epitaxial film growth in recessed source and drain areas. It can improve the epi film morphology to prevent dislocations and improve micro-loading by about 92%. Moreover, the epi surface roughness was improved by about 60%. Besides, 8% C_{ov} improvement and 32% I_{on} gain are achieved with better roll-off curve.

Acknowledgements

The authors would like to acknowledge analysis department at UMC for support on SIMS, AFM and TEM analysis.

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