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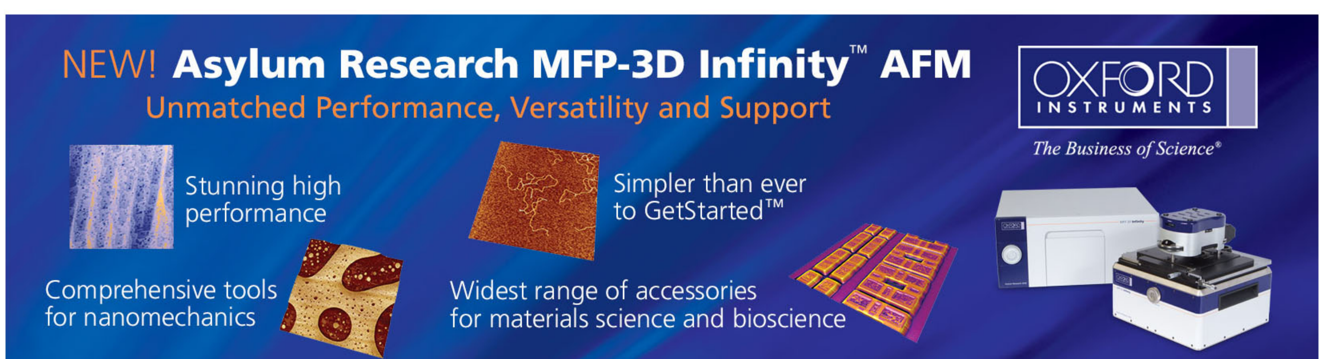

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Nonvolatile memory characteristics influenced by the different crystallization of Ni–Si and Ni–N nanocrystals

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The formation of Ni–Si and Ni–N nanocrystals by sputtering a $Ni_{0.3}Si_{0.7}$ target in argon and nitrogen environment were proposed in this paper. A transmission electron microscope analysis shows the nanocrystals embedded in the nitride layer. X-ray photoelectron spectroscopy and x-ray diffraction also offer the chemical material analysis of nanocrystals with surrounding dielectric and the crystallization of nanocrystals for different thermal annealing treatments. Nonvolatile Ni–Si nanocrystal memories reveal superior electrical characteristics for charge storage capacity and reliability due to the improvement of thermal annealing treatment. In addition, we used energy band diagrams to explain the significance of surrounding dielectric for reliability. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2841049]

Recently, nonvolatile memory devices (NVM) are moving toward high density cell array, low operation voltage, and good reliability. Although conventional flash memories do not require refreshing currently, they have some drawbacks that must be solved for further high performance memory application, such as quantum effect under thin tunnel oxide situation (<4 nm) and data retention time for reliability test.[1–4] For the development of next-generation NVM technique, devices fabrication should be required to be compatible with current manufacture process of the integrated circuit manufacture. Therefore, the silicon-oxide-nitride-oxide-semiconductor (SONOS) type and nanocrystals (NCs) memory structures have been proposed and demonstrated to lead to an improvement in retention time compared with conventional NVM because of employing discrete traps or quantum wells served as charge storage media.[5,6]

To alleviate the tunnel oxide design trade off for NVM devices, we proposed the memory structure that was combined with SONOS-type and metal nanocrystals to obtain better charge storage ability and strong coupling with conduction channel. In this letter, a simple process for nickel-silicide (Ni–Si) and nickel–nitride (Ni-N) nanocrystals embedded in nitride layer was formed by sputtering a commixed target in argon (Ar) and nitrogen (N_2) environment. It is found that the crystallization of nanocrystals and the quality of surrounding dielectric were distinct with different temperature annealings, thus, the annealing temperature was really a key parameter for the charge storage properties of NVM.

This memory structure was fabricated on a 4 in. *p*-type silicon (100) wafer which the resistivity was 10 Ω cm in this letter. After a standard clean process and native oxide removing, a 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace. Afterward, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer served as the charge trapping layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ commixed target in Ar/N_2 [24/10 SCCM (SCCM denotes cubic centimeter per minute at STP)] environment at room temperature, and the dc sputtering power was set to 80 W (deposition pressure ~7.6 mtorr). Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition system at 300 °C. In our work, the charge trapping layer was annealed at 500 and 600 °C for 100 s using a rapid thermal annealing system to improve the shape and crystallization of nanocrystals. In addition, the standard device (STD) is no use of annealing process, which this device also has the formation and NVM effect of NCs.[7] Finally, Al gate electrodes on back and front sides of the sample were deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Electrical characteristics, including the capacitance-voltage (*C-V*) hysteresis, retention and endurance characteristics were also performed. The *C-V* characteristics were measured by a HP4284 Precision LCR Meter with high frequency of 1 MHz. In addition, transmission electron microscope (TEM), x-ray photoelectron spectroscopy (XPS), and x-ray diffraction (XRD) were adopted for the microstructure analysis, chemical material analysis, and crystallization of NCs.

Figure 1 exhibits a cross-sectional TEM image of the STD (a) and after annealing temperature 600 °C (b) that all contain separated NCs embedded in the nitride layer. It was

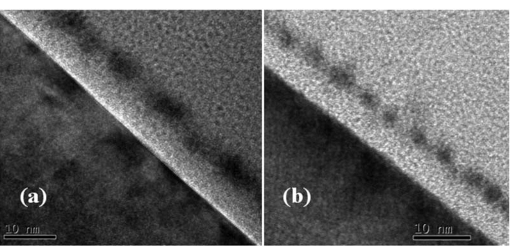

FIG. 1. The cross-sectional transmission electron microscope analysis of the STD (a) and after annealing temperature 600 °C (b) that all contain separated NCs embedded in the nitride layer.

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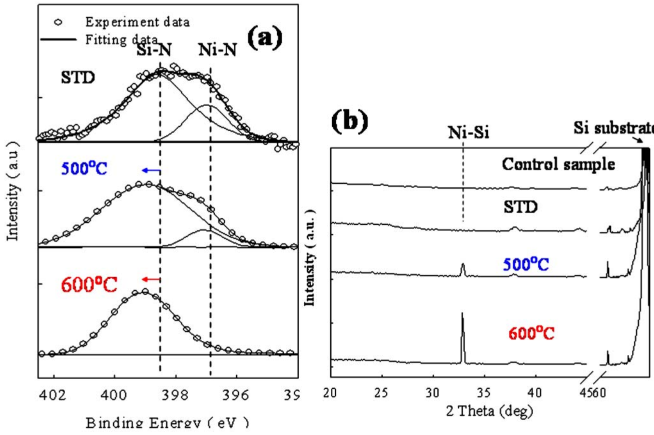

FIG. 2. (Color online) (a) N 1*s* x-ray photoelectron spectroscopy (XPS) analysis of the nanocrystals (Empty circles and straight line indicate experimental and fitting results, respectively). (b) X-ray diffraction (XRD) analysis of the nanocrystals during different thermal annealing temperature.

found that the roundness and isolation of NCs (600 °C) were better than STD simple because of the congregation of Ni atoms during thermal treatment. According to the previous theoretical model about the probability of an electron escaping from the NC back to the channel, the spherical NCs can reduce the Weinberg impact frequency that is affected by geometry effect.[8] Moreover, the more separated NCs can restrain electrons lateral migration effect under retention test because the electrons stored in the NC rise the energy level of NC conduction band that increase escaping probability.

To further analyze the chemical state and crystallization of NCs varied by thermal annealing temperature, XPS and XRD were performed to assay the chemical compositions, as shown in Figs. 2(a) and 2(b). Figure 2(a) shows the XPS N 1*s* core-level photoemission spectra which consists of two main peaks, Si–N (398.5 eV) and Ni–N (396.8 eV).[9,10] After the rapid thermal annealing at 500 and 600 °C, the peak signal of Si–N bonding shifted toward higher binding energy and the peak signal of Ni–N was decayed gradually to disappear. Besides, the XRD data can exhibit the crystallization situation of NCs and it is found the peak of Ni–Si is appeared at 32.8° after annealing temperature of 500 °C,[11] as shown in Fig. 2(b). (Control simple is only Si substrate with tunnel oxide structure.) We considered that the quality of surrounding dielectric SiN_x had been improved by a reducible reaction of Ni–N during thermal annealing treatment for the XPS analysis and the compound of NCs could be changed form Ni–N to Ni–Si after annealing process, which these results would affect charge storage ability for NVM application.

The typical *C-V* hysteresis obtained with gate voltage from accumulation to inversion and in reverse was measured to investigate the charge storage abilities of nonvolatile Ni–N and Ni–Si NCs memories. Figure 3(a) shows *C-V* hysteresis of STD with Ni–N NCs and it is clearly observed that memory windows of 1.5 and 3.5 V can be obtained under ±10 and ±12 V operations, respectively. However, the MOIOS structure with Ni–Si NCs has larger memory window of 4.0 V under ±10 V operation, as shown in Fig. 3(b). In addition, the difference of flatband voltage between Figs. 3(a) and 3(b) is due to coupling effect with conduction channel by the crystallizations of Ni–Si and Ni–N NCs.

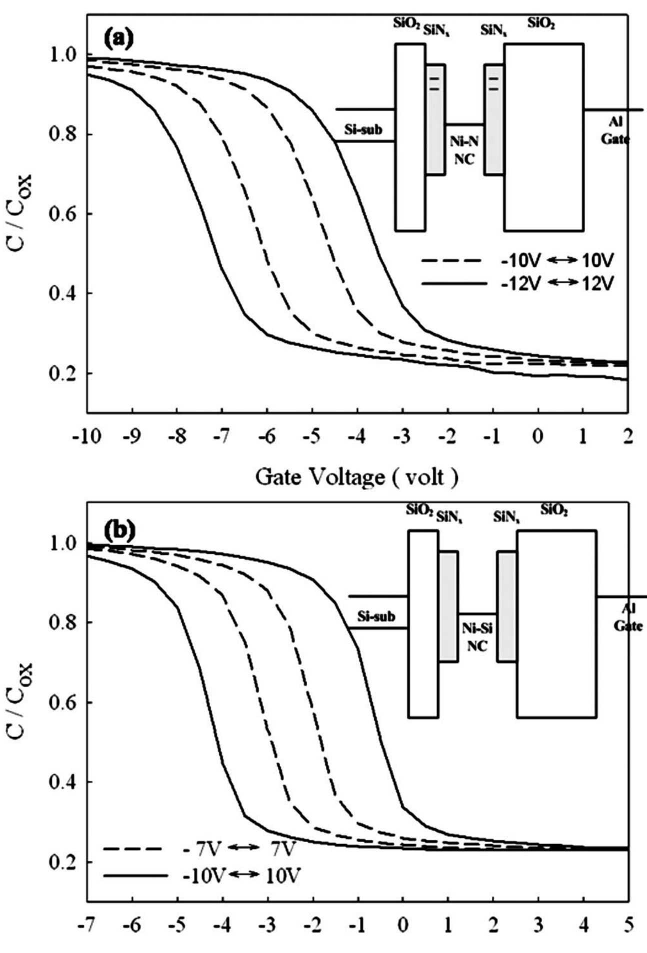

FIG. 3. (a) *C-V* hysteresis of nonvolatile Ni–N NCs memories. The memory window was 1.5 V under ±10 V operation and the inset was a simple energy band diagram. (b) *C-V* hysteresis of nonvolatile Ni–Si NCs memories. The memory window was 4.0 V under ±10 V operation and the inset was a simple energy band diagram.

The comparisons of electronic characteristics, such as memory window, retention, and endurance, are presented in Table I. We also clearly find that the memory window of Ni–Si NC is two times larger than Ni–N NC by adjusted *C-V* measurement for flatband voltage. This result could be considered that the resistivity of Ni–Si NCs (14–20 $\mu\Omega$ cm) is smaller that Ni–N NCs (151.7 $\mu\Omega$ cm)[12] because the resis-

TABLE I. Comparison table for the memory window, retention, and endurance. The initial memory window was fixed the same value for retention and endurance test.

	Memory window	Memory window after 10 years (retention)	Memory window after 10^6 P/E cycles (endurance)
Ni–N NC	1.5 V (−10↔10 V)	1.4 V (50%)	1.0 V (degradation 50%)
Ni–Si NC	2.8 V (−7↔10 V)	1.8 V (66%)	2.0 V (degradation 0%)

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tivity is inverse with density of state which is a property that affects the number of storage charges. Moreover, the initial memory window was fixed at the same value for retention and endurance test. The memory window of retention was obtained by comparing the *C-V* curves from a charged state (write/erase state) and the quasineutral state, which we used an extrapolation to give a long-term predictable result (ten years) after 1000 s (stable region of retention), as shown in Table I. Hence, it is clearly found that the reliability of nonvolatile Ni–Si NCs memory is better than Ni–N NCs. We considered that the quality of surrounding dielectric SiN_x was a major factor to influence the reliability. The insets of Figs. 3(a) and 3(b) were simple energy band diagrams to explain this phenomenon. Because of the nitride layer of STD simple deposited at low temperature environment, its density of traps was more than the memory cell after annealing process. From the inset of Fig. 3(a), the charges stored in the shallow traps of nitride layer were unstable and easy leaked into silicon substrate under retention test. Furthermore, the nonvolatile Ni–Si NC memory had stronger nitride layer than Ni–N NC memory to defend the interface between oxide and nitride under endurance test because this interface state generated by carries transportation would induce traps assisted tunneling effect resulting in lower charge storage ability.

In conclusion, the nonvolatile memory characteristics were influenced by the crystallizations of Ni–Si and Ni–N NCs. The nonvolatile Ni–Si NC memory shows the better charge storage ability and reliability than nonvolatile Ni–N NCs memory, since Ni–Si NC have higher density of state and stronger surrounding dielectric than the other one. Hence, the MOIOS structure needed a rapid thermal annealing process to obtain a high performance nonvolatile NC memory in this work.

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