A 40-MHz Double Differential-Pair CMOS OTA With −60-dB IM3

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***Abstract*—A configuration of a linearized operational transconductance amplifier (OTA) for low-voltage and high-frequency applications is proposed. By using double pseudodifferential pairs and the source-degeneration structure under nano-scale CMOS technology, the nonlinearity caused by short channel effect from a small feature size can be minimized. A robust common-mode control system is designed for input and output common-mode stability and thus reduces distortion caused b y common-mode voltage variation. Tuning ability can be achieved by using MOS transistors in the linear region. The linearity of the OTA is about −60-dB third-order inter-modulation (IM3) distortion for up to 0.9 $V_{\rm pp}$ at 40 MHz. This OTA was fabricated by the TSMC 180-nm deep n-well CMOS process. It occupies a small area of 15.1×10^{-3} mm^2 and the power consumption is 9.5 mW under a 1.5-V supply voltage.**

***Index Terms*—Operational transconductance amplifier (OTA), pseudodifferential structure, short channel effect, source degeneration.**

I. Introduction

THE operational transconductance amplifier (OTA) is one of the most important building blocks in analog and mixed-mode circuits, including multipliers [1], [2], continuous-time G_m-C filters [3], [4], voltage-controlled oscillators (VCOs) [5], and continuous-time sigma-delta modulators [6]. Its main idea is to convert the input voltage into the output current with a linear transformation factor. The active device is used for replacing passive devices owing to power and area consideration with the tradeoff of linearity. However, as the feature size of CMOS technology scales down with power supply voltage, the dynamic range, bandwidth, and power consumption will be limited by the linearity performance. A variety of linearization techniques have been reported in recent years [7]. Most of them exploit the ideal square-law behavior of the MOS transistor in the saturation region to obtain high-linearity conversion. Unfortunately, this concept is not quite suitable for small feature sizes of MOS transistors due to the influence of second-order effects like velocity saturation and mobility reduction. Thus, highly linear OTAs should be designed by taking short channel effects into consideration under nano-scale CMOS technology.

The use of multiple-input floating-gate (MIFG) MOS transistors was also presented recently [8], [9]. The natural attenuation could be obtained from the designed capacitor ratio. The MIFG circuit would act as a voltage divider and thus result in a large linear input swing range. However, the technique would need extra fabrication processes, and it would not be useful in standard CMOS technology. Moreover, large transconductances would be hardly achieved owing to the voltage attenuation of the input node. The linear OTA based on the flipped voltage follower (FVF) would be another useful technique [10], [11]. However, the linearity performance would be dependent on the circuit feedback loop gain, and the condition of stability should be carefully designed.

In this paper, we present a high-linearity and high-speed OTA. It makes use of two input transistor pairs with their source terminals connecting to resistor loads and the drain terminals cross-coupled to each other. In the approach, high linearity can be achieved by choosing different values of loading resistors. The model of the short channel effect and the nonlinearity analysis of CMOS transistors are described in Section II, and the proposed OTA implementation is presented in Section III. The analysis of non-ideal effects such as mismatch and noise performance of the proposed circuit are discussed in Section IV. Section V shows the measured performance of fabricated implementation. Finally, conclusions are drawn in Section VI.

II. Nonlinearity Analysis of Saturated MOS Transistors

A. Linearized V–I Characteristic

The relationship of the voltage-to-current conversion could be described as $i_o = f(v_{\rm in})$, where $v_{\rm in}$ and i_o are the input voltage and the output current, respectively. The ideal assumption of the linearized transformation is $f(v_{\rm in}) = k \times v_{\rm in}$, where k is a constant within the applied input voltage range. Unfortunately, the V–I conversion is not possible to be perfectly linear in real circuit implementation, and the conversion can be investigated by a Taylor series expansion. If the differential structure is applied with well-matched implementations, which means the even-order terms can be cancelled out, the current conversion can be expressed by

$$I_O = I_{D1} - I_{D2} = a_1 V_{\rm in} + a_3 V_{\rm in}^3 + a_5 V_{\rm in}^5 + a_7 V_{\rm in}^7 + \cdots \quad (1)$$

where the a_i coefficients are determined from the circuit implementation. If the nonlinear factor is suppressed, that is, the parameters $a_{i,i>2}$ are minimized, the V–I conversion would be close to a linear function, as demanded.

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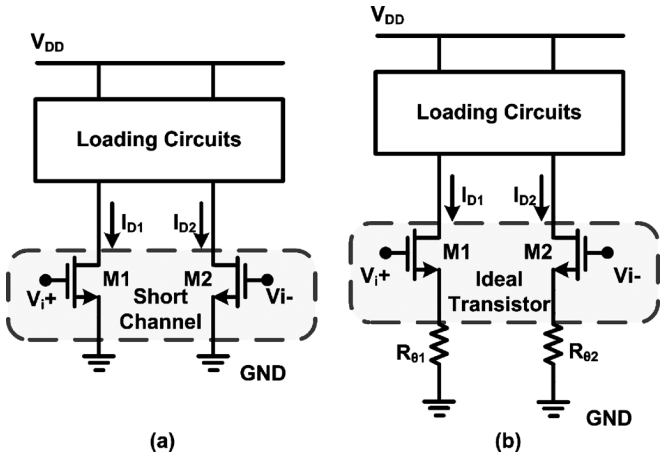

Fig. 1. Pseudodifferential circuit by taking short-channel effects into consideration.

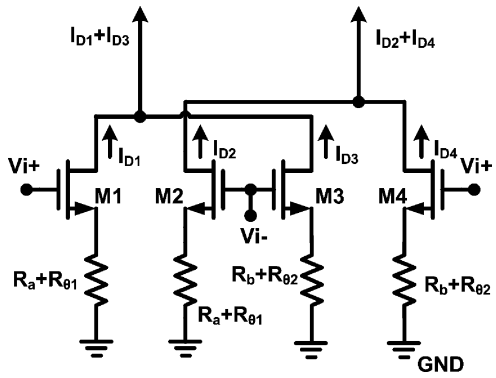

Fig. 2. Nonlinearity cancellation using double pseudodifferential pairs with degeneration resistors.

B. Saturated MOS Transistor Under Nano-Scale CMOS Technology

Linear V–I conversion is usually developed based on the basic square-law behavior of the MOS transistor in the saturation region [1] as

$$I_{D,\text{long}} = \frac{1}{2}K\left(V_{\text{GS}} - V_{\text{thn}}\right)^2 \tag{2}$$

where $K = \mu_n C_{\text{ox}}(W/L)$, W and L are the width and length of the device, respectively, C_{ox} is the oxide capacitance per unit channel area, μ_n is the low-field mobility, and V_{thn} is the nMOS threshold voltage. However, this condition only holds for the large length of MOS transistors. As the device size is scaled down towards nano-scale CMOS technology, the short-channel effect occurs due to the transversal and longitudinal electric fields. Thus, with the enhancement of speed and area for small device length, the linearity of V–I conversion based on the ideal square-law equation becomes deteriorated. Fig. 1(a) shows the circuit of the pseudodifferential input pair [12]. If the length of the MOS transistors is chosen to be the minimum feature size under nano-scale CMOS technology, the output drain current can be modeled by

$$I_{D,\text{short}} = \frac{K\left(V_{\text{GS}} - V_{\text{thn}}\right)^2}{2\left[1 + \theta\left(V_{\text{GS}} - V_{\text{thn}}\right)\right]} \tag{3}$$

where θ is the mobility reduction coefficient. From the equation shown above, the mobility reduction coefficient can be modeled by a resistor R_θ connected to the source terminal of an ideal MOS transistor, as shown in Fig. 1(b). The value of the equivalent resistor is equal to θ/K. Moreover, the linearity performance degrades for larger θ. This is confirmed by the results presented in [13], where tunable resistors are introduced in the source terminals of the pseudodifferential pair for the use of transconductance tuning ability with the expense of additional distortion. In this paper, in order to resist the nonlinearity which occurs by the short-channel effect, the double differential pairs with a source-degeneration structure are adopted, as shown in Fig. 2. In the proposed structure, two different values of resistors R_a and R_b are used for each differential pair, and the source-degenerated resistors are added up to simplify the expression. Assume that transistors M1–M4 are operated in the saturation region and that V_{i+} and V_{i-} are the input differential signals, which would be composed of common-mode and differential-mode voltages

$$\begin{aligned} V_{i+} &= V_{\text{cm}} + \frac{V_{\text{id}}}{2} \\ V_{i-} &= V_{\text{cm}} - \frac{V_{\text{id}}}{2} \end{aligned} \tag{4}$$

where V_{cm} is the input common-mode voltage and V_{id} is the input differential-mode voltage. Then, the output current of each transistor could be given by

$$\begin{aligned} I_{D1} &= \frac{K_1\left(V_{i+} - V_{\text{thn}}\right)^2}{2\left[1 + K_1\left(R_a + R_{\theta 1}\right)\left(V_{i+} - V_{\text{thn}}\right)\right]} \\ I_{D2} &= \frac{K_2\left(V_{i-} - V_{\text{thn}}\right)^2}{2\left[1 + K_2\left(R_a + R_{\theta 2}\right)\left(V_{i-} - V_{\text{thn}}\right)\right]} \\ I_{D3} &= \frac{K_3\left(V_{i-} - V_{\text{thn}}\right)^2}{2\left[1 + K_3\left(R_b + R_{\theta 3}\right)\left(V_{i-} - V_{\text{thn}}\right)\right]} \\ I_{D4} &= \frac{K_4\left(V_{i+} - V_{\text{thn}}\right)^2}{2\left[1 + K_4\left(R_b + R_{\theta 4}\right)\left(V_{i+} - V_{\text{thn}}\right)\right]} \end{aligned} \tag{5}$$

where $K_1 = K_2, K_3 = K_4, R_{\theta 1} = R_{\theta 2}$, and $R_{\theta 3} = R_{\theta 4}$. Thus, under ideal matching, the differential output current would be the function of the input signals

$$\begin{aligned} I_o &= (I_{D1} + I_{D3}) - (I_{D2} + I_{D4}) \\ &= f(V_{\text{id}}) \\ &= \left(a_{1,(1,2)} - a_{1,(3,4)}\right) V_{id} + \left(a_{3,(1,2)} - a_{3,(3,4)}\right) V_{id}^3 + \cdots \end{aligned} \tag{6}$$

where $a_{j,i}$ is the jth-order harmonic component provided by the ith transistor of the proposed structure, $a_{j,1} = a_{j,2} = a_{j,(1,2)}$, and $a_{j,3} = a_{j,4} = a_{j,(3,4)}$. Although the resistors connected to the source of a single pseudodifferential pair degrade the linearity performance, the third-order harmonic component could be cancelled out by proper sizing of the double pseudodifferential pairs through a Taylor series expansion of (6) to yield

$$a_{3,(1,2)} - a_{3,(3,4)} = 0. \tag{7}$$

This expression can be obtained by giving

$$\frac{\left(\frac{W_{(1,2)}}{L_{(1,2)}}\right)^2\left(R_a+R_{\theta(1,2)}\right)}{\left[2+\left(R_a+R_{\theta(1,2)}\right)g_{m(1,2)}\right]^4}=\frac{\left(\frac{W_{(3,4)}}{L_{(3,4)}}\right)^2\left(R_b+R_{\theta(3,4)}\right)}{\left[2+\left(R_b+R_{\theta(3,4)}\right)g_{m(3,4)}\right]^4} \tag{8}$$

where W_i, L_i, and g_{mi} is the width, length, and transconductance of the ith transistor, respectively, and $R_{\theta i}$ is the ith short-channel equivalent resistance. Under the minimization of the third-order harmonic component, the transconductance of the proposed structure is given by

$$G_{m,\text{total}}=\frac{g_{m(1,2)}\left[2+\left(R_a+R_{\theta(1,2)}\right)g_{m(1,2)}\right]}{2\left[1+\left(R_a+R_{\theta(1,2)}\right)g_{m(1,2)}\right]^2}-\frac{g_{m(3,4)}\left[2+\left(R_b+R_{\theta(3,4)}\right)g_{m(3,4)}\right]}{2\left[1+\left(R_b+R_{\theta(3,4)}\right)g_{m(3,4)}\right]^2}. \tag{9}$$

The transconductance decreases because of introducing the double differential pairs and the source-degeneration resistors. This implies higher linearity with the tradeoff of higher power consumption.

C. Design Methodology

In order to obtain high-linearity performance for the double differential pair structure under optimal transconductance efficiency, a simple approach is used by giving the ratio of parameters to represent the circuit operation. Thus, by giving

$$\frac{\frac{W_{(1,2)}}{L_{(1,2)}}}{\frac{W_{(3,4)}}{L_{(3,4)}}}=P;\quad \frac{R_a+R_{\theta(1,2)}}{R_b+R_{\theta(3,4)}}=Q;\quad V_{cm}=\frac{V_{\text{DD}}}{2} \tag{10}$$

we can find that the ratios of (10) would be used to define the transconductance efficiency compared with the single differential-pair circuit and the third-order harmonic component of the proposed circuit. In addition, the ratio values should be designed within practical implementation boundary. Bandwidth, noise performance, and matching are also taken into consideration.

The optimization procedure starts from the reduced transconductance value. We define that less then 30% of the transconductance should be reduced with respect to that of a single differential-pair circuit with the same size and current consumption. From Fig. 3, we can find that, if the value of Q is set to 3 under large P, we can obtain less than 30% reduction of the transconductance. Moreover, if the value of 4 for Q is used, less than 25% reduction of the transconductance would be obtained. Fig. 4 shows the third-order distortion component of the proposed design. In order to obtain minimized distortion components, the ratio P is chosen as 9 while Q is set to 3. If Q is set to 4 for less transconductance reduction, P should be set to 16, but such a large ratio would degrade the bandwidth performance owing to the large parasitic capacitance of input transistors. After the optimization procedure, the optimal ratios of the proposed circuit would be given by

$$P=9;\quad Q=3. \tag{11}$$

The optimization procedure concludes that the third-order distortion component is ideally cancelled out with the expected transconductance value, as shown in Fig. 5. The linearity performance is actually robust to process variation owing to the flat distribution in Fig. 4. Thus, the small reduction of the transconductance value makes high linearity and high speed possible under about 30% of extra power consumption.

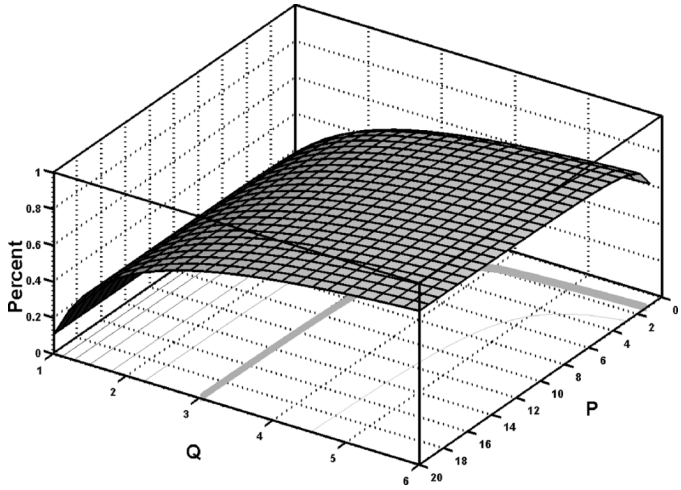

Fig. 3. Optimal parameter evaluation for the reduced transconductance.

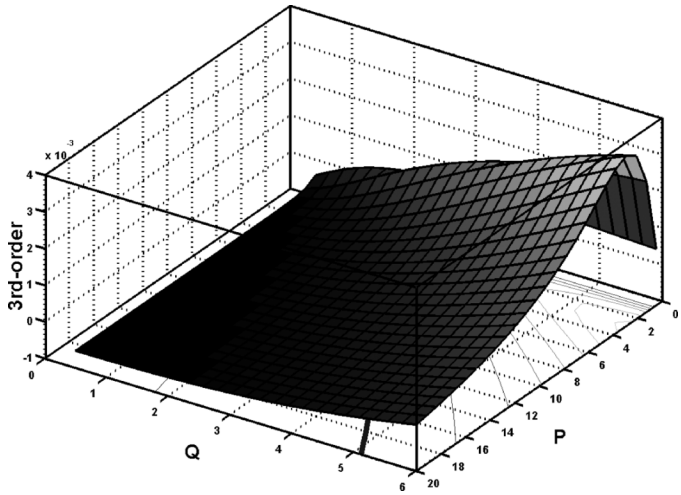

Fig. 4. Optimal parameter evaluation for the third-order harmonic component.

Transconductance tuning would be another important issue in the OTA design. The main idea of the transconductance tuning is to compensate for the variation caused from fabricated process and temperature. Fig. 5 shows the contour plot of the third-order harmonic component under transconductance tuning, resulted from Fig. 4. We can find that, if Q is changed from 1 to 4 when P is set to 9, it implies more than 300% of the transconductance tuning range, as shown in Fig. 3, and the third-order harmonic component value of less than 0.001 can be guaranteed, as illustrated in Fig. 5.

III. Proposed OTA Circuit

A. Implementation of the Linearization Technique

Fig. 6 shows the proposed OTA design. Two differential pairs M1–M2 and M3–M4 are used in order to cancel the nonlinearity component, as described in the previous section. For continuous

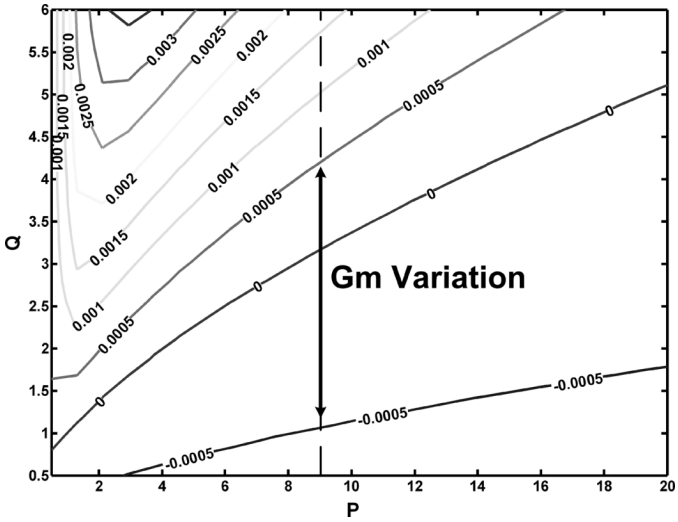

Fig. 5. Contour plot for the third-order harmonic component under transconductance tuning.

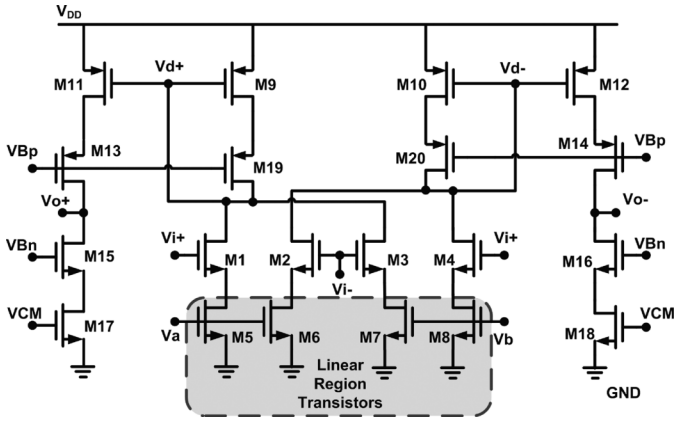

Fig. 6. Proposed OTA circuit.

transconductance tuning strategy, transistors M5–M8 operating in the linear region are used to replace the resistors. The equivalent resistance is given by

$$R_{\rm eq}^{-1} = K(V_G - V_{\rm thn}) \tag{12}$$

where V_G is the gate voltage of the transistor. Therefore, we can obtain the required equivalent resistance by applying the voltage V_a and V_b to yield

$$R_a^{-1} = K_{(5,6)}(V_a - V_{\rm thn}) \tag{13}$$

$$R_b^{-1} = K_{(7,8)}(V_b - V_{\rm thn}). \tag{14}$$

The linearity can be maintained by proper sizing of the degenerated transistors and the control voltage. In addition, the tuning ability of the proposed circuit can be achieved by adjusting the control voltages V_a and V_b. Fig. 7 shows the simulated large-signal transconductance of the differential OTA operating in a 1.5-V supply voltage. The proposed circuit can be tuned from 360 to 470 μS. It can be noticed that the transconductance tuning range is limited by the linear-region operation of transistors M5–M8. Besides, the speed of the proposed OTA is mainly limited by the parasitic capacitors caused by the current mirror circuits.

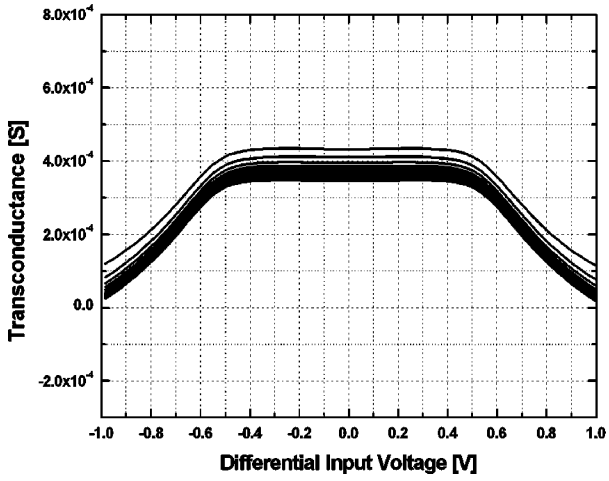

Fig. 7. Simulated transconductance tuning range.

B. Common-Mode Stability

The OTA shown in Fig. 6 requires a proper common-mode control system due to the pseudodifferential structure [14], [15]. The common-mode control system includes the common-mode feedforward (CMFF) circuit and the common-mode feedback (CMFB) circuit. The CMFF circuit should be used with the CMFB circuit for output common-mode voltage stabilization. Fig. 8 shows the circuit of the common-mode control system. For the CMFB circuit, the input transistors MF1–MF4 perform the tasks of the common-mode detection and reference comparison. If the common-mode voltage of the OTA output signal equals the desired common-mode voltage Vref, then the total current through MF7 will be constant and the common-mode bias voltage VCM is fixed. On the other hand, if the common-mode voltage of the OTA output signal is not the same as Vref, a current will be mirrored by MF9 to change VCM adaptively. Thus, the feedback mechanism adjusts the output common-mode voltage to the desired value.

Furthermore, the input common-mode control circuitry is formed by transistors MF14–MF18 that constitute the CMFF circuit. The combination of transistors MF14 and MF15 generates a scaled copy of input common-mode currents, which is subtracted at the OTA output stage through the use of current mirror MF17–MF18. Thus, the input common-mode signal could be suppressed out and only the differential-mode signal appears at the output stage. As the mechanism shown above, it is demonstrated the common-mode control circuit can be implemented to achieve excellent stability over the tuning range. Moreover, linearity could be maintained by the robust and stable common-mode control system.

The common-mode rejection (CMR) depends on matching. We can define a matching factor of $(1 + \Delta)$ between the CMFF path and the signal path, where Δ is the mismatch ratio. We can emulate the CMFB circuit as a small resistor of value $1/g_{\rm CMFB}$, and then the common-mode gain of $A_{\rm CM} = G_{m,\rm total}(g_o - \Delta \times g_{m(17,18)})/(g_{m(17,18)} \times g_{\rm CMFB})$ at low frequency can be obtained, where $G_{m,\rm total}$ is obtained from (9), $g_{m(17,18)}$ is the transconductance of transistors M17 and M18, and g_o is the output conductance of the OTA. This is the result of the combined CMFB and CMFF systems. Because $g_{\rm CMFB}$ is large and $A_{\rm CM}$ is much less than unity, even mismatch problems occur so that high CMR can be obtained.

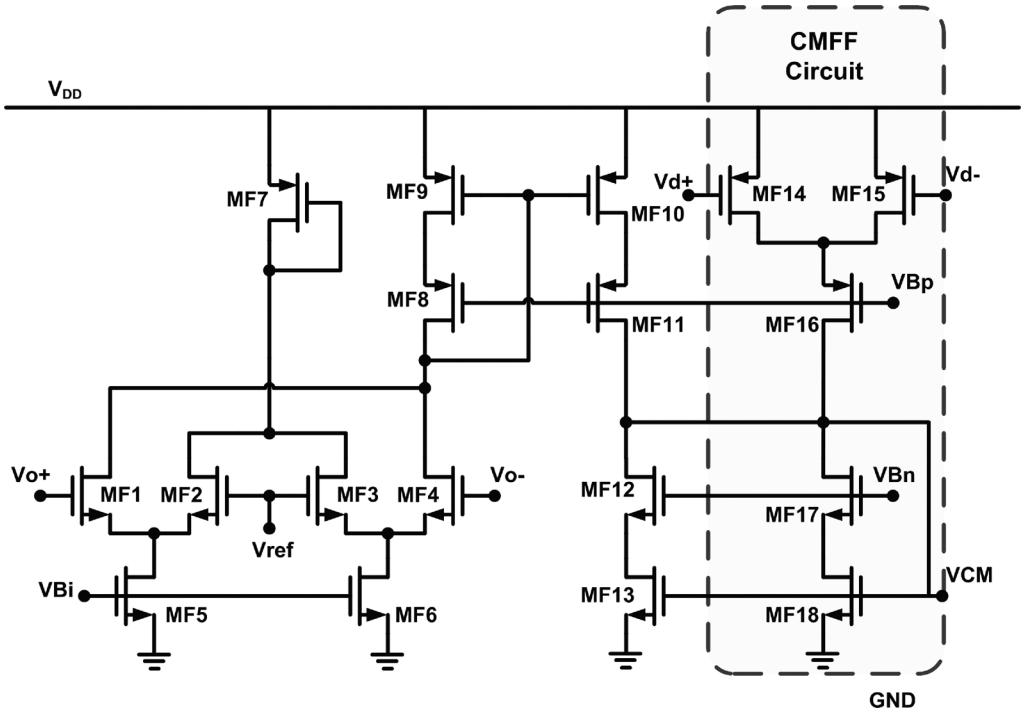

Fig. 8. Common-mode control system.

IV. NonIdeality Analysis of the Implementation

A. Mismatch

Owing to the nonideal matching phenomena of MOS transistors, the nonlinearity cancellation is not perfect and second-order harmonic distortion components would still appear at the differential output nodes. For the double differential-pair structure, it is assumed that there are mismatches of $K_{(1.2)} \pm \varepsilon_a K_{(1,2)}$ for transistors M1 and M2 and $K_{(3,4)} \pm \varepsilon_b K_{(3,4)}$ for transistors M3 and M4. Repeating the analysis of (6), we can find that the second-order distortion component resulted from mismatch is given by

$$a_2 \approx \frac{\varepsilon_a K_{(1,2)}}{\left[1+\left(R_a+R_{\theta(1,2)}\right) g_{m(1,2)}\right]^3} + \frac{\varepsilon_b K_{(3,4)}}{\left[1+\left(R_b+R_{\theta(3,4)}\right) g_{m(3,4)}\right]^3}. \quad (15)$$

Therefore, the distortion components caused by transistor mismatch could be minimized by applying large degenerated resistors and gate overdrive voltage. Besides, the current mirrors M9–M12 would also contribute second-order distortion components under the proposed degenerated structure, and thus large device sizes and small aspect ratios would be designed. From the simulation with 2% transistor mismatch, the highest even-order components remain lower than odd-order components by at least 5 dB. In addition, careful layout was taken while the device match is required. The error output current contributed by transistor mismatch can be divided by the overall transconductance to model an equivalent offset voltage, and it could be removed by applying an offset voltage of input differential signals.

B. Thermal Noise

For the high-speed circuit, the most significant noise source of a single transistor is the thermal noise rather than the flicker noise. The channel noise can be modeled by a current source connected between the drain and source with a spectral density

$$\overline{I_n^2} = 4kT\delta g_{ms} \quad (16)$$

where k is the Boltzmann constant, T is the absolute temperature, g_{ms} is the source conductance, and the device noise parameter δ depends on the bias condition [16]. Using the thermal noise model, the total output-referred noise spectral density of the double differential pairs with degeneration structure is derived as

$$\begin{aligned}\overline{I_{n,\text{out}}^2} \approx 8kT \Bigg[& \delta_s g_{m(9,10)} + \delta_s g_{m(1,2)} \left(\frac{1}{1+g_{m(1,2)}R_a}\right)^2 \\ & + \delta_l R_a \left(\frac{g_{m(1,2)}}{1+g_{m(1,2)}R_a}\right)^2 \\ & + \delta_s g_{m(3,4)} \left(\frac{1}{1+g_{m(3,4)}R_b}\right)^2 \\ & + \delta_l R_b \left(\frac{g_{m(3,4)}}{1+g_{m(3,4)}R_b}\right)^2 \Bigg] \left(\frac{g_{m(11,12)}}{g_{m(9,10)}}\right)^2 \\ & + 8kT\delta_s g_{m(17,18)} \end{aligned} \quad (17)$$

where δ_s and δ_l would be the noise parameter at saturation and linear regions, respectively. The input-referred noise spectral density could be calculated by dividing the output-referred noise

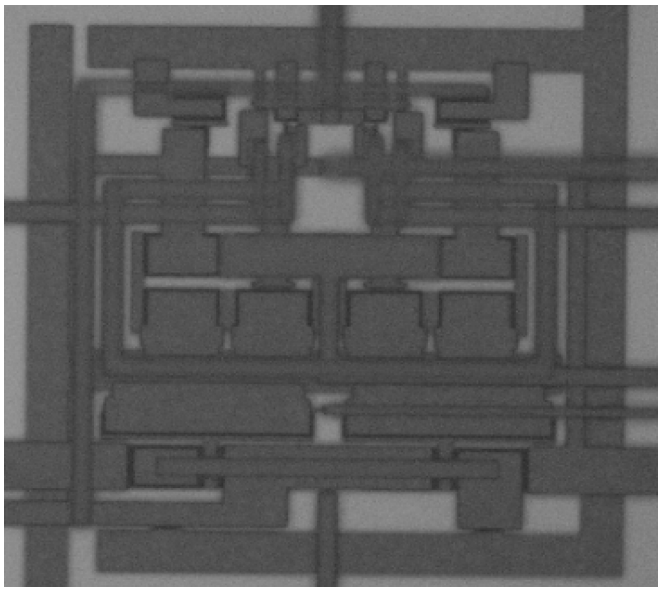

Fig. 9. Die microphotograph.

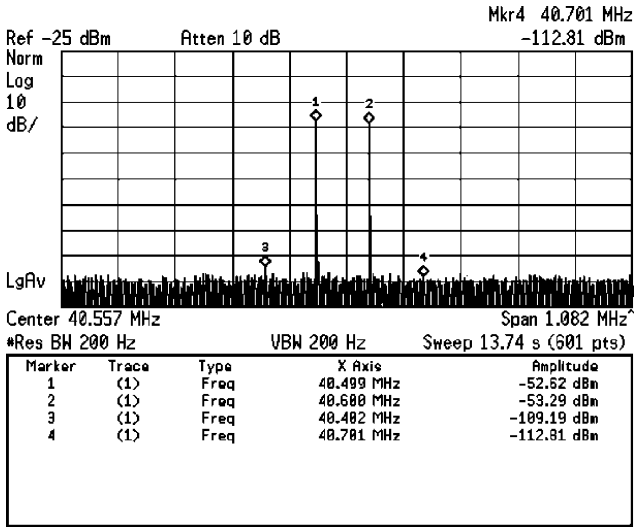

Fig. 10. Measured two-tone inter-modulation distortion.

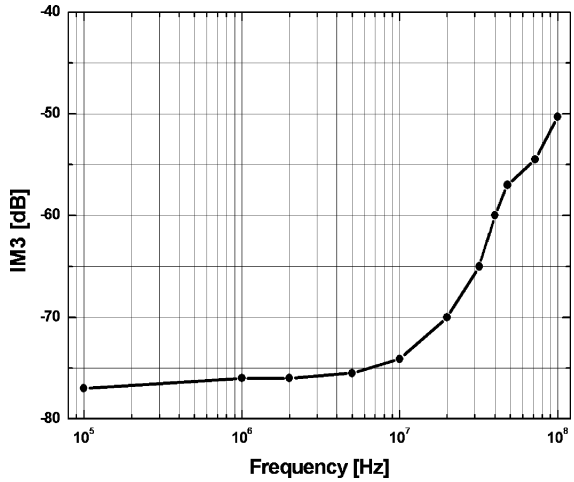

Fig. 11. Measured two-tone inter-modulation distortion with respect to input signal frequency.

spectral density by the overall OTA transconductance. From the noise analysis, large aspect ratios of input transistors and small aspect ratios of load transistors should be designed. The input-referred noise of the proposed circuit is higher than the single differential-pair circuit owing to the fact that the noise contribution is the combination of two input differential pairs. Moreover, the degenerated MOS resistors contribute additional noise sources to the proposed circuit.

V. Experimental Results

The proposed OTA has been fabricated with TSMC 180-nm deep n-well CMOS process. It has been measured to verify its operation and to evaluate the linear V–I characteristics. A microphotograph of the linear OTA is depicted in Fig. 9, and the occupied area is 15.1×10^{-3} mm^2. A supply voltage of 1.5 V was employed in the measurements, and the nominal static power consumption of the OTA is 9.5 mW. The required supply voltage for the circuit is $V_{\rm GS}+2V_{\rm DS}$ (saturation region), and 1.5 V is sufficient for this circuit to operate under 180-nm CMOS process.

For the measurement setup, the output signal of the signal generator was past through a low pass filter for the spectral purity of the input signal. The transformers were used before and after the input and output terminals for single-to-differential and differential-to-single conversion for the differential circuit. The output signal was measured with a spectrum analyzer. The third-order inter-modulation (IM3) distortion measured with two sinusoidal tones of 0.9-V_{pp} amplitude is shown in Fig. 10. The IM3 is shown to be about −60 dB at a speed of 40 MHz. Fig. 11 shows the nonlinearity behavior with respect to the frequency under the same input swing range. At low frequencies, the IM3 of -75 dB could be obtained. Moreover, IM3 less than -55 dB could be achieved for a frequency up to 60 MHz. The increment of the IM3 is due to the different high frequency behaviors of the two input differential pairs. The measured input referred noise spectral density at 40 MHz is 23 nV/$\sqrt{}$Hz. Table I summarizes this work with recently reported works. In order to compare with different implementations of OTAs, the defined figure of merit (FOM), which takes the transconductance value, linearity performance, speed of the implemented circuit, input swing range, and power consumption into account, is expressed as follows:

$$\mathrm{FOM} = 10\log\left(\frac{G_m \times V_{\rm id} \times IM3_{\rm linear} \times f_o}{\rm power}\right). \qquad (18)$$

Therefore, our high-speed linear OTA compares favorably with the literature.

VI. Conclusion

An approach to enhance the OTA linearity under nano-scale technology has been proposed, and the experimental result proves the same linear characteristic by the fabricated chip.

TABLE I
COMPARISON WITH PREVIOUSLY REPORTED WORKS

Reference	2005 CAS-I [9]	2005 CAS-I [11]	2003 JSSC [12]	2006 CAS-II [17]	2004 CAS-II [18]	2005 JSSC [19]	This work
Technology	0.8 μm CMOS	0.8 μm CMOS	0.5 μm CMOS	0.18 μm CMOS *Simulation	0.35 μm CMOS	0.5 μm CMOS	0.18 μm CMOS
Tranconductance Value	0.08μS	266μS	1065μS	20μS	100μS	100μS	470μS
Linearity	-40dB THD at 100Hz	-43dB HD3 at 1kHz	-43dB HD3 at 30MHz	-65dB HD3 at 1MHz	-65dB IM3 at 20MHz	-66.5dB THD at 100kHz	-60dB IM3 at 40MHz
Input swing range	1.1 V_{pp}	0.4 V_{pp}	0.9V_{pp}	0.6V_{pp}	1.3V_{pp}	2V_{pp}	0.9V_{pp}
Supply Voltage	1.5V	2V	3.3V	1.8V	3.3V	2.6V	1.5V
Power consumption	1μW	150μW	10.7mW	145μW	10.5mW	1.7mW	9.5mW
Figure of merit (FOM)	29	50	84	82	86	74	93
Input-referred noise spectral density	-	-	9.8nV/$\sqrt{}$Hz	-	75nV/$\sqrt{}$Hz	-	23nV/$\sqrt{}$Hz

By taking the short-channel effect into consideration under small feature sizes, this approach is based on the nonlinearity cancellation scheme with two pseudodifferential pairs of the source-degeneration structure, and the circuit performs well at high frequencies. The MOS transistors working in the linear region were used to replace the poly resistors. It not only saves the chip area but also adds the tuning ability. A common-mode control circuitry, including the CMFF and CMFB circuits, is used for the input and output common-mode stability. The measurement results show about −60-dB IM3 with 40-MHz 0.9-$V_{\rm pp}$ input signals under a 1.5-V supply voltage.

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