On-Chip Transient Detection Circuit for System-Level ESD Protection in CMOS Integrated Circuits to Meet Electromagnetic Compatibility Regulation

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***Abstract*—A new on-chip transient detection circuit for system-level electrostatic discharge (ESD) protection is proposed. The circuit performance to detect different positive and negative fast electrical transients has been investigated by the HSPICE simulator and verified in a silicon chip. The experimental results in a 0.13-μm CMOS integrated circuit (IC) have confirmed that the proposed on-chip transient detection circuit can be used to detect fast electrical transients during the system-level ESD events. The proposed transient detection circuit can be further combined with the power-on reset circuit to improve the immunity of the CMOS IC products against system-level ESD stress.**

***Index Terms*—Electrical transient detection, electrostatic discharge (ESD), system-level ESD test, transient noise.**

I. Introduction

THE ELECTROSTATIC discharge (ESD) event has become an important reliability issue to integrated circuits (ICs). To meet the component-level ESD reliability, on-chip ESD protection circuits have been added to the input/output (I/O) cells and power (V_{DD} and V_{SS}) cells of CMOS ICs [1], [2]. Besides the component-level ESD stress, system-level ESD is an increasingly significant reliability issue in CMOS IC products. This tendency results from the strict requirements of reliability test standards, such as the system-level ESD test for electro magnetic compatibility (EMC) regulation. In the system-level ESD test standard of IEC 61000-4-2 [3], the electrical/electronic product must sustain the ESD level of +8 kV (+15 kV) under contact discharge (air discharge) test mode to meet the immunity requirement of "level 4." Such high-energy ESD-induced noises often cause damage or malfunction of CMOS ICs inside the equipment under test (EUT). It has been reported that some CMOS ICs are very susceptible to system-level ESD stress [4]–[6], even though they have passed the component-level ESD specifications, such as a human body model (HBM) of ±2 kV [7], machine model (MM) of ±200 V [8], and charged-device model (CDM) of ±1 kV [9].

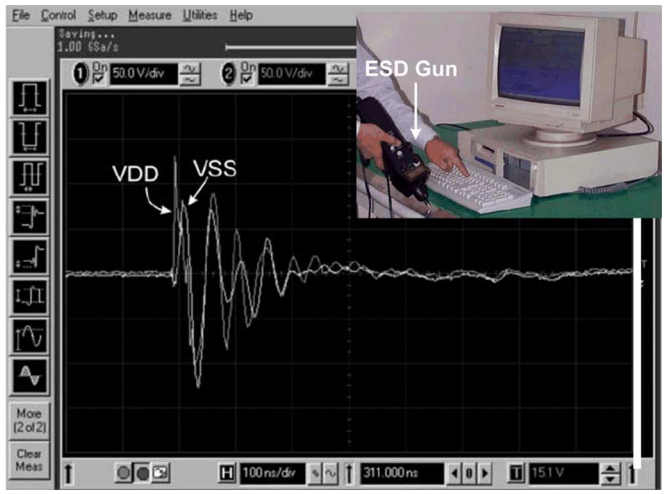

Fig. 1. Measured V_{DD} and V_{SS} waveforms of the microcontroller ICs inside the keyboard with an ESD voltage of +1000 V zapping on the HCP under system-level ESD test.

The inset in Fig. 1 shows an EUT (keyboard), which was stressed by an ESD gun with a charged voltage of +1000 V zapping on the horizontal coupling plane (HCP). During the system-level ESD test, the power and ground lines of the microcontroller IC in the keyboard no longer maintain their normal voltage levels, but an underdamped sinusoidal voltage with the amplitude of several hundred volts occurred, as shown in Fig. 1. This ESD-generated transient is quite large and fast, which can randomly couple to the power, ground, or I/O pins of the microelectronics system. Such a high-voltage-level fast transient causes the keyboard to be upset or frozen after the system-level ESD zapping [4]. Such fast transients also cause transient-induced latchup events in CMOS ICs [10].

To meet the system-level ESD specifications, two useful methods have been reported and investigated [11]–[13]. One effective method is to add some discrete noise-decoupling components or board-level noise filters into the CMOS IC products to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD test [11], [12]. Different types of noise filter networks can be used to improve the system-level

Manuscript received November 16, 2006; revised April 16, 2007, July 25, 2007, and September 14, 2007. This work was supported in part by the National Science Council, Taipei, Taiwan, R.O.C., under Contract NSC 96-2221-E-009-182, and in part by Himax Technologies Inc., Tainan, Taiwan, R.O.C.

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Digital Object Identifier 10.1109/TEMC.2007.911911

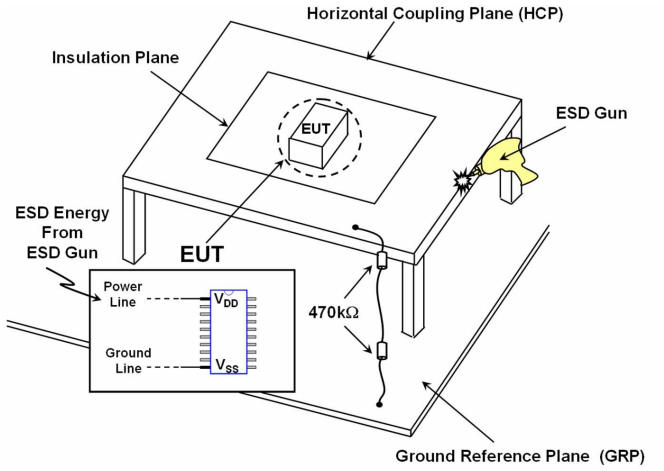

Fig. 2. Measurement setup for system-level ESD test with indirect contact-discharge test mode [3].

ESD immunity, including capacitor filter, ferrite bead, transient voltage suppressor (TVS), and several high-order noise filters such as LC-like (second-order) and π-section (third-order) filters. It has been proved that the system-level ESD immunity of CMOS ICs under system-level ESD test can be greatly improved by choosing proper components in noise filter networks [13]. The other method to improve the system-level ESD immunity of CMOS ICs is to regularly check the system abnormal conditions by using an external hardware timer, such as a retriggerable monostable multivibrator [11]. The additional discrete noise-bypassing components substantially increase the total cost of a microelectronic product with CMOS ICs. Therefore, an on-chip solution integrated into the CMOS ICs, but without adding the additional discrete noise-decoupling components on the printed circuit board (PCB), is strongly requested by the IC industry.

In this paper, an on-chip transient detection circuit is proposed to detect the fast electrical transient under the system-level ESD test [14]. The new proposed transient detection circuit can be combined with the power-on reset circuit to provide a hardware/firmware codesign solution for system-level ESD stress. The circuit operation to detect different positive and negative fast electrical transients has been investigated by the HSPICE simulation. The experimental results verified in a 0.13-μm CMOS IC have confirmed that the proposed on-chip transient detection circuit can successfully detect the fast electrical transients during system-level ESD zapping.

II. System-Level ESD Test

In the test standard of IEC 61000-4-2 [3], two test modes have been specified: air-discharge test mode and contact-discharge test mode. Fig. 2 shows the measurement setup of the system-level ESD test with indirect contact-discharge test mode. The system-level ESD measurement setup consists of a wooden table on the grounded reference plane (GRP). In addition, an isolation plane is used to separate the EUT from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470-kΩ resistors in series.

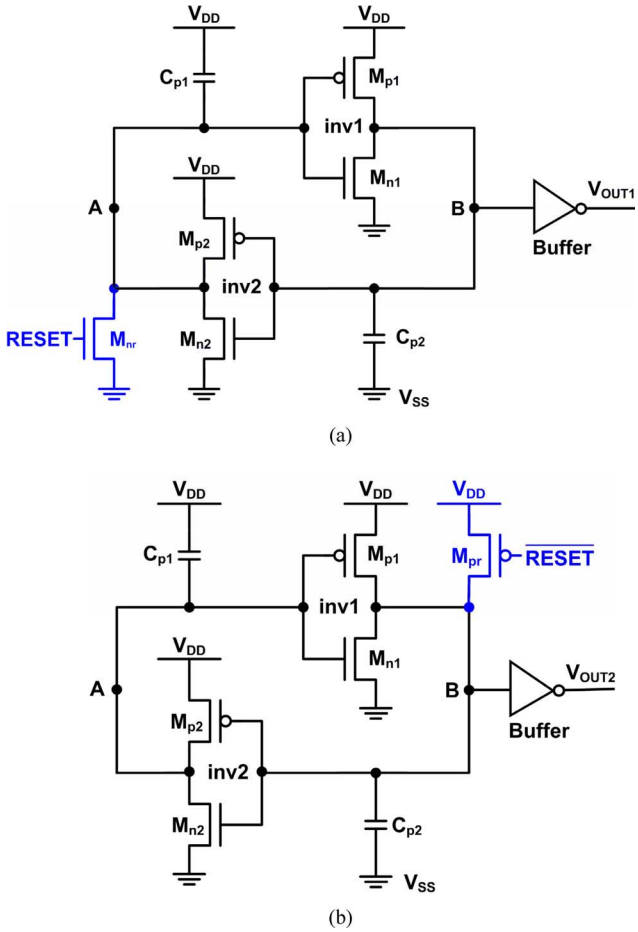

Fig. 3. Proposed on-chip transient detection circuits realized with (a) NMOS-reset, and (b) PMOS-reset functions.

With the measurement setup in Fig. 2, the immunity of CMOS IC products against the system-level ESD stress can be evaluated. When the ESD gun zaps to the HCP, all CMOS ICs inside the EUT could be disturbed due to the high ESD-coupled energy, as the waveforms show in Fig. 1. By using the digital oscilloscope, the transient responses on power lines of CMOS IC products can be recorded and further analyzed. Thus, the circuit performance of the proposed transient detection circuit can be evaluated through this measurement setup.

III. Transient Detection Circuit

A new on-chip transient detection circuit is proposed to detect the fast electrical transient under the system-level ESD zapping. By adding two coupling capacitors into a latch with two cascaded CMOS inverters, the proposed transient detection circuit can be designed to memorize the occurrence of system-level ESD events.

A. Circuit Structure

The proposed transient detection circuits realized with NMOS-reset and PMOS-reset functions are shown in Fig. 3(a) and (b), respectively. The detection circuits, comprised of one latch and two coupling capacitors, are designed to memorize the

occurrence of system-level ESD and to sense the fast electrical transient on the power ($V_{\rm DD}$) and ground ($V_{\rm SS}$) lines. The detection circuits shown in Fig. 3(a) and (b) are realized with 3.3-V devices in a 0.13-μm CMOS process for the circuit with 3.3-V power-supply voltage.

In order to increase the sensitivity of the detection circuit in Fig. 3(a) and (b) during fast electrical transient under the system-level ESD zapping, the device *W/L* ratios of latch should be well designed. In order to effectively pull down the voltage level at the node B, the NMOS ($M_{\rm n1}$) in the inverter1 (inv1) is designed with a larger *W/L* than that of the PMOS ($M_{\rm p1}$). On the contrary, to effectively pull up the voltage level at the node A easily, the PMOS ($M_{\rm p2}$) in the inverter2 (inv2) is designed with a larger *W/L* ratio than that of the NMOS ($M_{\rm n2}$). The sensitivity of the transient detection circuit can be increased by adjusting the device *W/L* ratios in the latch.

In order to enhance the sensitivity of the detection circuit to the electrical transient, two coupling capacitors ($C_{\rm p1}$ and $C_{\rm p2}$) are added between the input nodes (A, B) and the power lines ($V_{\rm DD}$ and $V_{\rm SS}$). The capacitor $C_{\rm p1}$ is placed between the $V_{\rm DD}$ and the input node of inv1 in order to sense the fast electrical transient from $V_{\rm DD}$. The capacitor $C_{\rm p2}$ is placed between the $V_{\rm SS}$ and the input node of inv2 in order to sense the fast electrical transient from $V_{\rm SS}$. The NMOS ($M_{\rm nr}$) in Fig. 3(a) and the PMOS ($M_{\rm pr}$) in Fig. 3(b) are used to provide the initial reset function in order to avoid the metastable operation of the latch circuit. With the reset signal of 3.3 V (0 V) applied to the gate of $M_{\rm nr}$ ($M_{\rm pr}$), the node A (B) of the detection circuit, shown in Fig. 3(a) and (b) can be initially set at 0 V (3.3 V). In normal circuit operations, the output nodes ($V_{\rm OUT1}$ and $V_{\rm OUT2}$) of the proposed transient detection circuits will be kept at logic 0. When a system-level ESD event occurs, the fast transient noises injecting into the power lines ($V_{\rm DD}$/$V_{\rm SS}$) will change the output state from logic 0 to logic 1. Therefore, the system-level ESD event can be detected by the proposed detection circuits. The sensitivity of the proposed transient detection circuit can be further enhanced by adjusting the device *W/L* ratios in the latch or changing the value of coupling capacitors ($C_{\rm p1}$ and $C_{\rm p2}$).

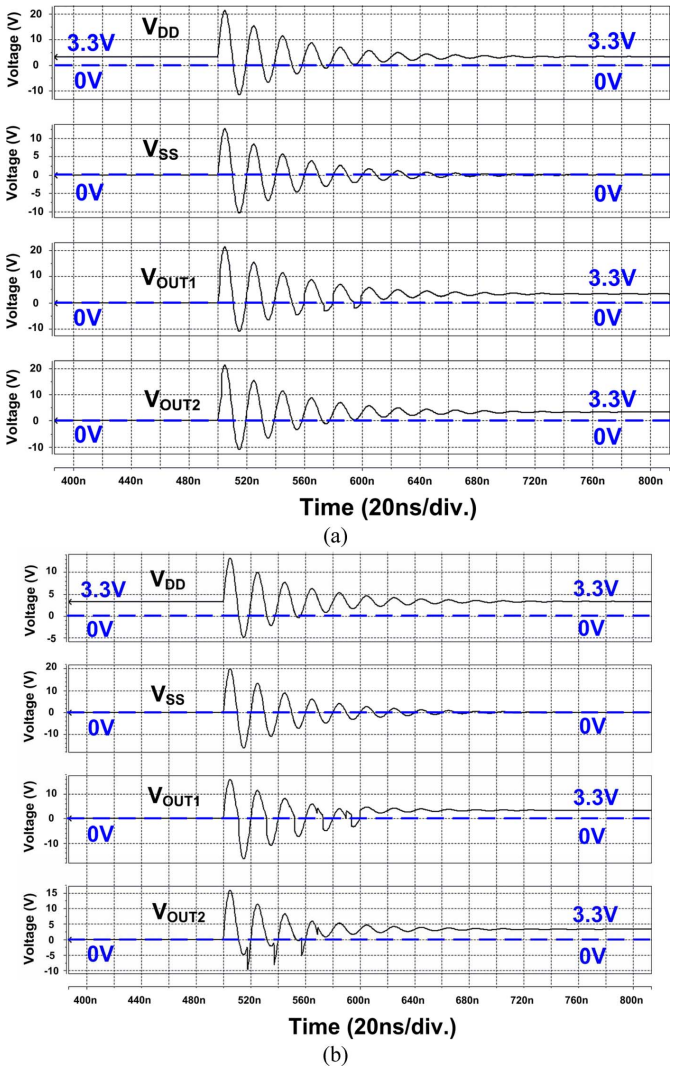

Fig. 4. Simulated $V_{\rm DD}$, $V_{\rm SS}$, $V_{\rm OUT1}$, and $V_{\rm OUT2}$ waveforms of the proposed transient detection circuits under system-level ESD test with larger overshooting voltage coupled on (a) $V_{\rm DD}$ and (b) $V_{\rm SS}$.

B. Simulation

From the measured fast electrical transient waveforms, shown in Fig. 1, the underdamped sinusoidal waveforms on $V_{\rm DD}$/$V_{\rm SS}$ during the system-level ESD stress have been observed. Thus, a specific time-dependent voltage source given by

$$V(t) = V_0 + V_a \sin(2\pi f(t - t_d)) \exp(-(t - t_d)D_a) \quad (1)$$

is used to generate an underdamped sinusoidal voltage on the power lines of the proposed transient detection circuits in the simulation. With the proper parameters, such as the applied voltage amplitude V_a, initial dc voltage V_o, damping factor D_a, damping frequency f, and time-delay t_d, the intended underdamped sinusoidal voltage can be constructed for simulation. In the following HSPICE simulation with positive or negative underdamped sinusoidal waveforms, the same parameters of $D_a = 2 \times 10^7\ {\rm s}^{-1}$, $f = 50\,{\rm MHz}$, and $t_d = 500$ ns are used (which is corresponding to the measured transient waveform in Fig. 1), whereas the only difference is positive V_a for positive-going underdamped sinusoidal waveform and negative V_a for negative-going underdamped sinusoidal waveform. In addition, V_o of 3.3 and 0 V are used for fast electrical transient waveforms on the $V_{\rm DD}$ and $V_{\rm SS}$, respectively.

Under the positive system-level ESD zapping condition, the simulated $V_{\rm DD}$, $V_{\rm SS}$, $V_{\rm OUT1}$, and $V_{\rm OUT2}$ waveforms of the proposed transient detection circuit with a positive-going underdamped sinusoidal voltage on $V_{\rm DD}$ and $V_{\rm SS}$ are shown in Fig. 4(a) and (b). Due to different coupling paths or filter networks from the ESD source to the $V_{\rm DD}$ and $V_{\rm SS}$ pins of the chip, there could be different ESD levels on $V_{\rm DD}$ and $V_{\rm SS}$. Thus, two different simulations are taken into consideration. The positive-going underdamped sinusoidal voltages with V_a of $+20$ V on $V_{\rm DD}$ and with V_a of $+12$ V on $V_{\rm SS}$ are used to simulate the larger overshooting voltage coupled on $V_{\rm DD}$ under the system-level ESD test, as shown in Fig. 4(a). The positive-going underdamped sinusoidal voltages with V_a of $+12$ V on $V_{\rm DD}$ and with V_a of

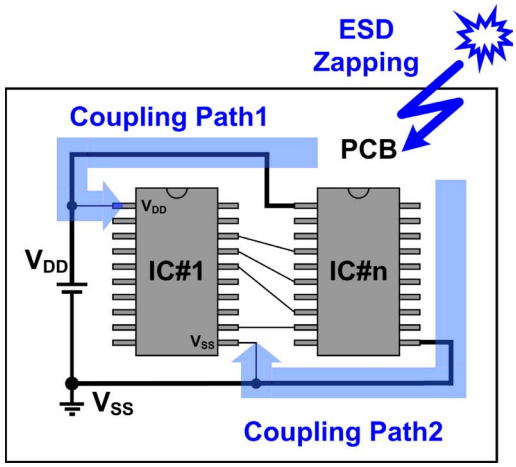

Fig. 5. Different coupling paths from ESD stress source to V_{DD} and V_{SS} pins of the IC on the PCB.

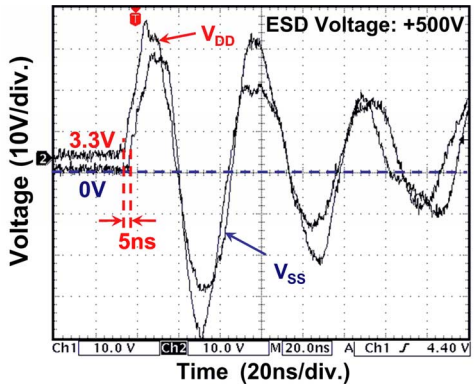

Fig. 6. Measured V_{DD} and V_{SS} transient responses with an ESD voltage of $+500$ V zapping on the HCP under system-level ESD test. There is a delay of 5 ns between the V_{DD} and V_{SS} waveforms in the first ringing period during the fast transient stress.

$+20$ V on V_{SS} are used to simulate the larger overshooting voltage coupled on V_{SS} under the system-level ESD test, as shown in Fig. 4(b). For both simulations, the V_{DD} voltage is initially kept at 3.3 V with a V_{SS} of 0 V. During the fast transient of the ESD stress, V_{DD} begins to increase rapidly from 3.3 V. V_{OUT1} and V_{OUT2} are disturbed simultaneously during the V_{DD}/V_{SS} disturbance. At the same time, the transient detection circuit can detect the occurrence of the disturbance on V_{DD}/V_{SS}. As a result, when V_{DD} finally returns to its normal stable voltage level of 3.3 V, V_{OUT1} and V_{OUT2} will be changed from 0 to 3.3 V to memorize the occurrence of transient events, as shown in Fig. 4(a) and (b). The circuit operation can be analyzed from the voltage derivative on the coupling capacitors. Under the positive system-level ESD zapping condition, a current can be coupled through coupling capacitors, which can be expressed as

$$I_1 = C_{P1}\frac{dV_1}{dt} \tag{2}$$

where V_1 is the voltage across the coupling capacitor C_{p1} and I_1 is the induced coupling current through C_{p1}. The voltage derivative between V_{DD} and V_{SS} can introduce the coupling current. The final logic state of the transient detection circuit will depend on the coupled voltage potential. The logic state of the transient detection circuit can be changed when the voltage potential on node A is charged up to the logic threshold voltage of inv1. The related equation can be expressed as

$$C_{P1}\frac{dV_1}{dt} \times R_1 \geq V_{TH1} \tag{3}$$

where R_1 is the equivalent resistance on node A and V_{TH1} is the logic threshold voltage of inv1.

On the PCB design with CMOS IC products, the trace routing placements may be different for power (V_{DD}) lines and ground (V_{SS}) lines. This will cause different coupling paths from the ESD source to the V_{DD} and V_{SS} pins of the chip, as shown in Fig. 5. The different coupling paths may result in different delays between the V_{DD} and V_{SS} waveforms. Thus, the proposed transient detection circuit should be evaluated in the circuit simulation under different delays in the transient waveforms

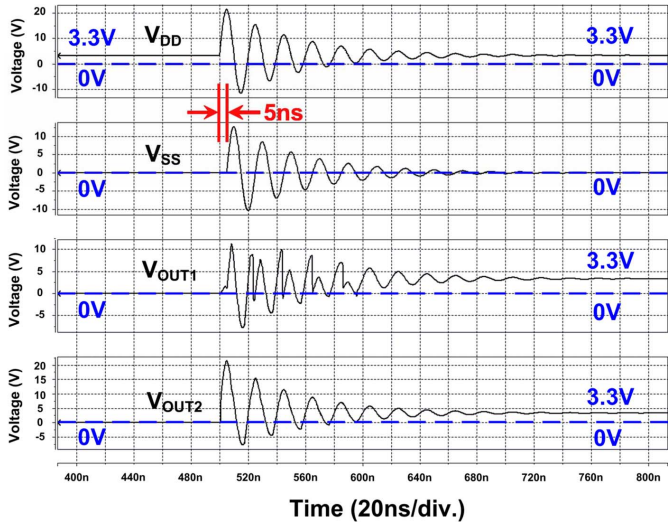

Fig. 7. Simulated V_{DD}, V_{SS}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuit under positive-going underdamped sinusoidal voltage on V_{DD}/V_{SS} power lines with a 5-ns delay condition.

between V_{DD} and V_{SS}. The measured V_{DD} and V_{SS} waveforms of the proposed transient detection circuit with an ESD voltage of $+500$ V zapping on the HCP under system-level ESD test are shown in Fig. 6. A delay of 5 ns between the V_{DD} and V_{SS} in the first ringing period during the fast transient stress has been observed, as shown in Fig. 6.

The simulated V_{DD}, V_{SS}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuit with a delay of 5 ns between the V_{DD} and V_{SS} waveforms are shown in Fig. 7. The positive V_a on V_{DD} and V_{SS} waveforms is used to simulate the positive ESD stress under the system-level ESD test, as shown in Fig. 6. During the period with a fast transient, V_{OUT1} and V_{OUT2} are influenced by the V_{DD}/V_{SS} disturbance. Finally, V_{OUT1} and V_{OUT2} are pulled up to the voltage level of 3.3 V. With a delay between V_{DD} and V_{SS}, the proposed transient detection circuit can still memorize the occurrence of the fast transient of the ESD stress.

TABLE I
DEVICE DIMENSION RATIOS (IN MICROMETERS) AND ELEMENT VALUES OF THE PROPOSED ON-CHIP TRANSIENT DETECTION CIRCUIT

M_{p1}	1/0.35
M_{n1}	2.5/0.35
M_{p2}	2.5/0.35
M_{n2}	1/0.35
C_{p1}	500fF
C_{p2}	500fF

From these simulations, the output states of the transient detection circuits can be changed and kept at logic 1 after the system-level ESD events. Therefore, the proposed transient detection can memorize the occurrence of the system-level ESD and sense the fast electrical transient on the power lines ($V_{\rm DD}$/$V_{\rm SS}$).

C. Design Considerations

By using the HSPICE, the circuit operation of the proposed transient detection circuit to sense fast electrical transients can be analyzed in detail. The sensitivity of the transient detection circuit can be analyzed by changing the coupling capacitors or adjusting the device *W/L* ratios in the latch.

Table I shows the device dimensions and element values in the proposed transient detection circuit, as shown in Fig. 3(a). The purpose of adding the coupling capacitors ($C_{\rm p1}$ and $C_{\rm p2}$) in the proposed transient detection circuit is to enhance the sensitivity to fast electrical transients between power lines ($V_{\rm DD}$/$V_{\rm SS}$) and latch logic gates (node A and node B). Under the delay of 5 ns between $V_{\rm DD}$ and $V_{\rm SS}$, coupling capacitors ranging from 150 to 400 fF are used to investigate their sensitivity improvements on the transient detection circuit with device ratios listed in Table I. With higher coupling capacitors, the minimum positive amplitude to cause output ($V_{\rm OUT1}$ and $V_{\rm OUT2}$) logic state transition of transient detection circuits can be greatly reduced. For example, the minimum positive amplitude of the transient on $V_{\rm DD}$ to cause transition at the output ($V_{\rm OUT1}$/$V_{\rm OUT2}$) of the detection circuits can be significantly reduced from +84 V (with a coupling capacitor of 150 fF) to +2.1 V (with a coupling capacitor of 400 fF), as shown in Fig. 8(a). Thus, by choosing the coupling capacitors with a proper value, the sensitivity to fast electrical transients under system-level ESD test can be improved, regardless of the positive or negative transient levels.

By changing the device *W/L* ratios in the latch, the switching threshold voltage of the inverters (inv1 and in2) can be adjusted, and the driving capabilities of the PMOS and NMOS transistors can be modified. Under the delay of 5 ns between the $V_{\rm DD}$ and $V_{\rm SS}$, the device widths of $M_{\rm n1}$ ranging from 1.75 to 2.8 μm are used to investigate the sensitivity improvement on the transient detection circuit with $C_{\rm p1} = C_{\rm p2} = 200$ fF and device ratios listed in Table I. With a larger device *W/L* ratio of NMOS ($M_{\rm n1}$) in inverter1, the transient detection circuit can pull down the voltage at node B more efficiently. For example, the minimum positive amplitude of the transient on $V_{\rm DD}$ to cause transition at the output ($V_{\rm OUT1}$/$V_{\rm OUT2}$) of detection circuits can be significantly reduced from +82 to +17 V by adding the device width of $M_{\rm n1}$ from 1.75 to 2.8 μm, as shown in Fig. 8(b). From these

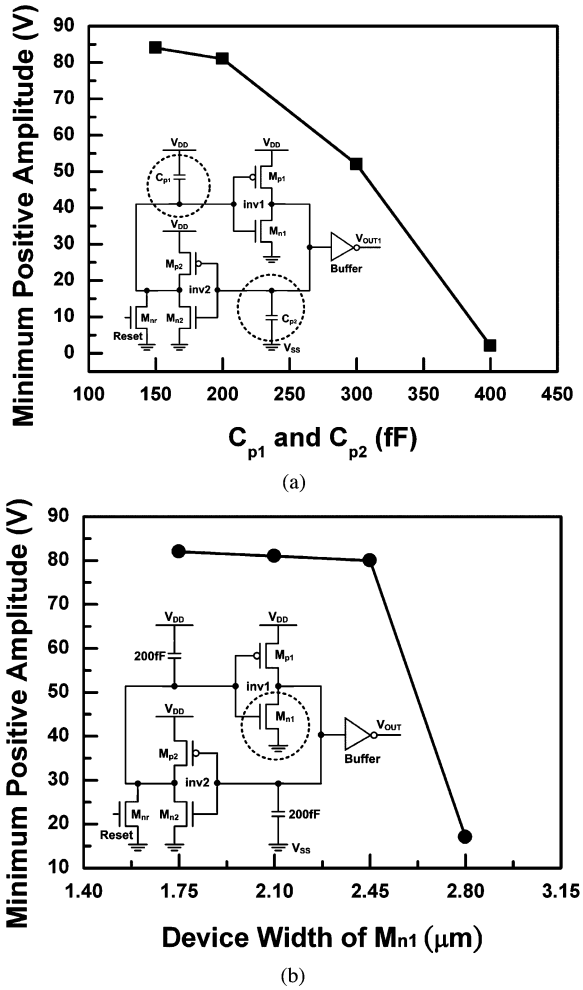

Fig. 8. Minimum positive amplitude to change the output logic state of the transient detection circuit under (a) different coupling capacitors ($C_{\rm P1}$ and $C_{\rm P2}$) with channel width of $M_{\rm n1} = 2.5$ μm, and (b) different channel widths of $M_{\rm n1}$ with $C_{\rm P1} = C_{\rm P2} = 200$ fF. The channel length of $M_{\rm n1}$ is kept at 0.35 μm.

design considerations, the HSPICE simulation can be used to fine-tune the device sizes in the proposed transient detection circuits to detect different transient electrical levels.

From the measured fast electrical transient waveforms in Fig. 1, the underdamped sinusoidal waveforms on $V_{\rm DD}$ and $V_{\rm SS}$ during the system-level ESD stress have been observed. The frequency of the underdamped sinusoidal waveforms on $V_{\rm DD}$ and $V_{\rm SS}$ is about several tens of megahertz. The detection frequency of the proposed transient detection circuit should cover such a range in order to detect fast electrical transients during the system-level ESD test. With a delay of 5 ns, the relationship between the damping frequency and minimum positive voltage to change the output logic state of the transient detection circuit is shown in Fig. 9. The relationship between the frequency factor and the underdamped sinusoidal waveforms has been analyzed in [15]. The frequency determines how fast the underdamped sinusoidal waveform will be attenuated within its first duration (cycle). The underdamped sinusoidal voltage waveform will become a unipolar overdamped voltage waveform if the damping

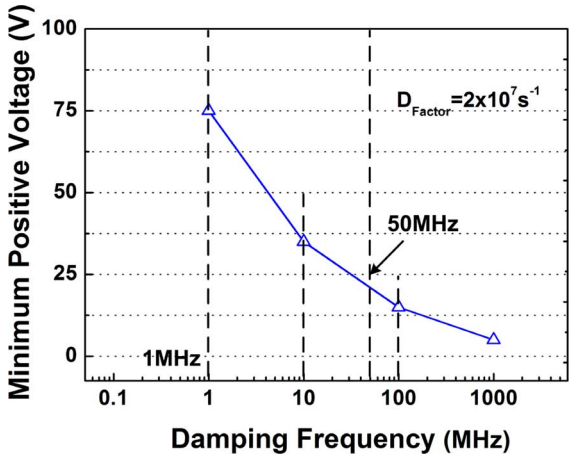

Fig. 9. Relationship between damping frequency and minimum positive voltage to change the output logic state of the transient detection circuit.

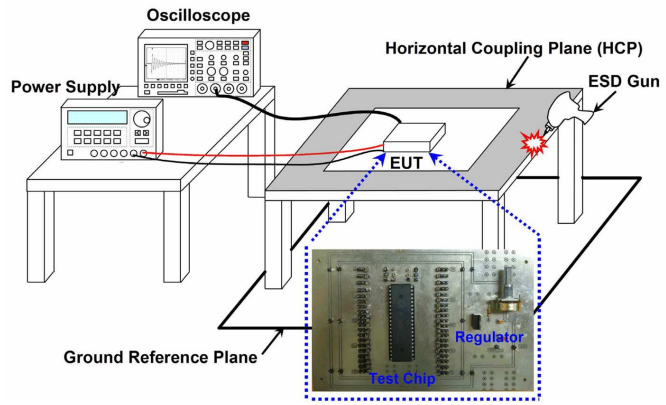

Fig. 10. Measurement setup to verify the detection function of the transient detection circuit under system-level ESD test.

frequency is too low [15]. From the simulated results in Fig. 9, the transient detection circuit can detect fast electrical transients with the frequency of several tens of megahertz, which will be typically generated during the system-level ESD test.

D. Discussion

In order to improve the system-level ESD immunity of CMOS ICs, the watchdog timer is often designed with a microelectronic system to regularly check the system abnormal conditions. A watchdog timer is a computer hardware timing device to reset the operation system if the main program is locked or frozen due to some fault conditions. The intention is to recover the system from the frozen state to normal operation. Under normal operation conditions, a watchdog timer maintains itself in the counting state. The firmware periodically sends a reset signal to the watchdog timer. The watchdog timer can be implemented with a counter working with a clock signal. Most watchdog timers are used in embedded systems, where this specialized timer is often a built-in unit of the microcontroller. If the main program is locked or frozen in an infinite state, the watchdog will not receive the reset signal. Then, the watchdog timer will send a signal into firmware to reset the main program. However, the logic states of a watchdog timer are stored in the registers or flip flops. It has been investigated that the logic states stored in the registers or flip flops can be destroyed or changed during system-level ESD tests to cause malfunction or frozen state on the main operation program [4].

The microcontroller with the watchdog timer can avoid the continued frozen state due to some fault conditions. However, the circuit implementation of a watchdog timer is more complicated than the proposed transient detection circuit. The watchdog timer should be implemented with registers or flip flops to store logic states and combined with counter or other embedded systems to provide the reset function. Moreover, complicated circuit implementation will result in more current consumption.

IV. Experimental Results

The proposed on-chip transient detection circuits in Fig. 3(a) and (b) had been fabricated in a 0.13-μm 1.2/3.3-V 1P8M CMOS process. The system-level ESD test with indirect contact-discharge test mode is used to verify the performance of the proposed transient detection circuit. Both positive and negative fast electrical transient waveforms are recorded by the oscilloscope to clearly indicate whether the detection circuit works correctly during the system-level test.

To verify the function of the transient detection circuit under the system-level ESD test, the measurement setup is shown in Fig. 10. The voltage waveforms on both the V_{DD} and output pins of the transient detection circuit are simultaneously monitored by a digital oscilloscope. The power supply provides the dc voltage and the regulator on the EUT provides the voltage of 3.3 V to the test chip. After the system-level ESD test with indirect contact-discharge mode, the output voltage of the transient detection circuit is observed to see whether it changed from 0 to 3.3 V.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuit under the system-level ESD test with an ESD voltage of $+1500$ V zapping on the HCP are shown in Fig. 11. V_{DD} begins to increase rapidly from the normal voltage ($+3.3$ V). Meanwhile, V_{OUT1} and V_{OUT2} show great increase under such high-energy ESD stress. During the period with disturbance on V_{DD}, V_{OUT1} and V_{OUT2} are disturbed simultaneously. Finally, the output voltage of the transient detection circuit has been changed from 0 to 3.3 V. The measured V_{DD}, V_{OUT1}, and V_{OUT2} transient waveforms of the proposed transient detection circuits under the system-level ESD test with an ESD voltage of -1500 V zapping on the HCP are shown in Fig. 12. During V_{DD} disturbance, V_{OUT1} and V_{OUT2} are disturbed simultaneously. Obviously, V_{OUT1} and V_{OUT2} are finally pulled up to the 3.3 V after the fast electrical transient. The experimental results are consistent with the HSPICE simulation results under positive and negative system-level ESD zapping conditions. The first nanoseconds of the data shown in Figs. 11 and 12 might be influenced by direct coupling into the probing system. However,

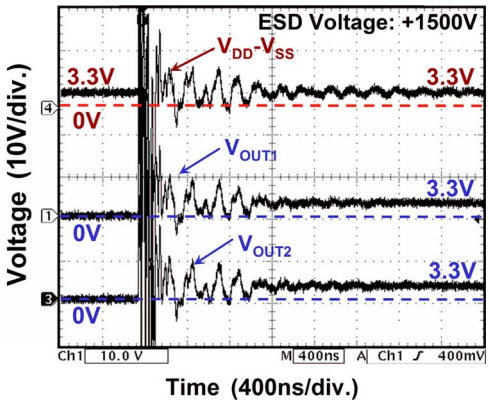

Fig. 11. Measured V_{DD}, V_{OUT1}, and V_{OUT2} transient responses under system-level ESD test with ESD voltage of +1500 V zapping on the HCP.

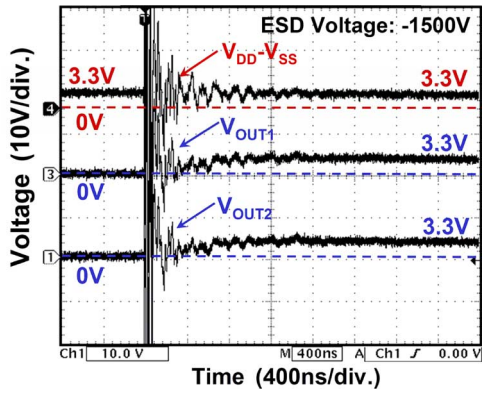

Fig. 12. Measured V_{DD}, V_{OUT1}, and V_{OUT2} transient responses under system-level ESD test with an ESD voltage of −1500 V zapping on the HCP.

the functionality of the detection circuit can be clearly seen from the change of the output level as a result of the ESD.

The circuit performance of the transient detection circuit under the system-level ESD test had been proven by both the experimental results and the HSPICE-simulated results. From the experimental results, the proposed transient detection circuit can indeed memorize the occurrence of the system-level ESD stress under both positive and negative fast electrical transient zapping conditions.

V. Applications in CMOS ICs

The proposed transient detection circuit can be codesigned with firmware to provide a system solution to solve the system-level ESD issue of microelectronic products realized with CMOS ICs. It has been proven that the hardware/firmware can be codesigned and can be used effectively to improve the system-level ESD robustness of the CMOS IC products [4].

As shown in the flowchart in Fig. 13, the detection results (V_{OUT}) from the on-chip transient detection circuits can be temporarily stored as an ESD flag for firmware check. The states in the transient detection circuit and the ESD flag are initially cleared to logic 0 by the power-on reset. The reset procedure is executed through the normal firmware reset procedure when the ESD flag has a state of logic 0. When the fast electrical transient

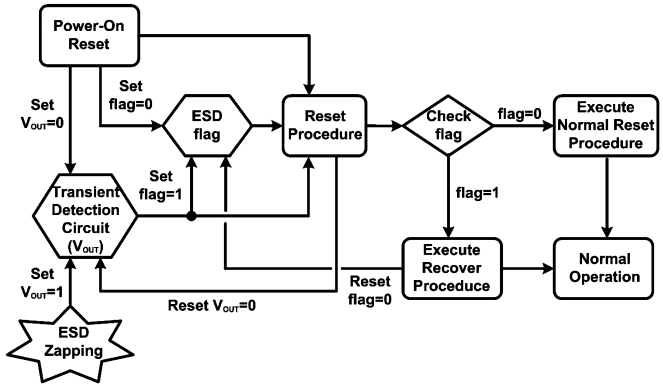

Fig. 13. Firmware flowchart to reset or recover the system if the on-chip ESD transient detecting circuit detects the electrical transient during the system-level ESD stress.

happens, the on-chip transient detection circuit can detect the fast electrical transient to change the output states V_{OUT} to logic 1. At the same time, the ESD flag is restored at logic 1, and the firmware executes the recover procedure to recover all system functions to a stable state as soon as possible. After the reset and recover procedures, the states in the transient detection circuit and the ESD flag are reset to logic 0 again for detecting the next ESD events.

To realize system-level ESD protection function, a hardware/firmware codesign solution combined with the transient detection circuit and the power-on reset circuit have been analyzed. Under the normal power-on condition, the V_{DD} power-on voltage waveform has a rise time of the order of milliseconds (ms). As there is no input signal except the V_{DD} power-on voltage waveform, the power-on reset circuit should be designed with the same internal delay as the order of milliseconds. Thus, the output signal of the power-on reset circuit can set the ESD flag to logic 0, as shown in Fig. 14(a). However, there are some mistriggered conditions in the power-on reset circuit. For example, the fast power-up time (in the range of microseconds) may create difficult situations for the power-on reset circuit to work properly. Therefore, a transient detection circuit is designed to sense fast electrical transients on power lines and combined with the power-on reset circuit so as to provide hardware/firmware codesign solutions for system-level ESD issues.

Due to the difference in the rise times between the ESD voltage and the V_{DD} power-on voltage, the on-chip transient detection circuit is designed to sense fast electrical transients and set the flag signal to logic 1, as shown in Fig. 14(b). Then, the firmware can execute the recover procedure to recover all the electrical functions to a stable state as soon as possible. After the reset and recover procedures, the ESD flag is reset to logic 0, again, for detecting the transient ESD events.

By including the on-chip transient detection circuit and an additional ESD flag into the chip, the firmware flowchart, shown in Fig. 13, can be used to improve the system-level ESD robustness of microelectronic products. Such an hardware/firmware codesign method can provide an effective system solution to solve the system-level ESD issues in a microelectronics system realized with CMOS ICs.

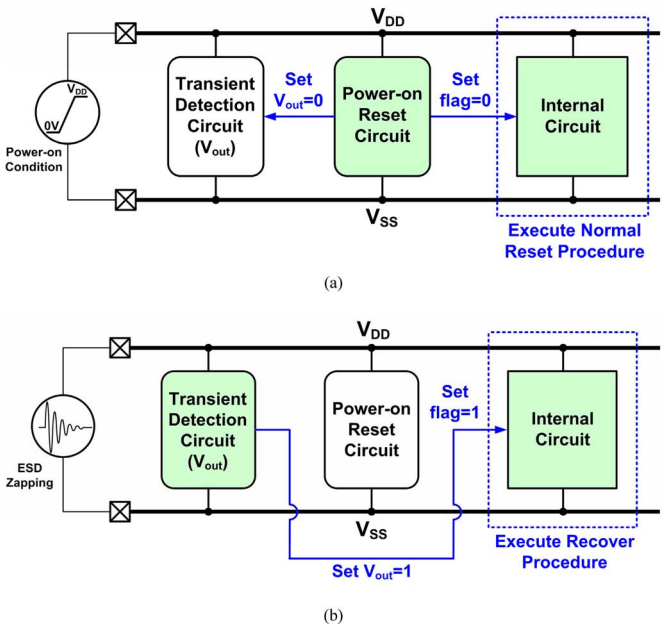

Fig. 14. Hardware/firmware operation during (a) power-on reset condition and (b) system-level ESD stress.

VI. Conclusion

A new transient detection circuit for system-level ESD protection has been fabricated in a 0.13-μm CMOS process. By using one latch logic gate and two coupling capacitors, the on-chip transient detection circuit can be designed to detect the fast electrical transients during the system-level ESD zapping. The circuit performance under different positive and negative fast electrical transients had been also investigated by the HSPICE. The experimental results on silicon chip have confirmed that the proposed on-chip transient detection circuit can be used to detect fast electrical transients during system-level ESD zapping. The proposed transient detection circuit can be further combined with firmware design and power-on reset circuit to provide an effective solution to the system-level ESD issue in microelectronics systems realized with CMOS ICs.

Acknowledgment

The authors would like to thank Mr. C.-C. Tsai, Dr. T.-Y. Chen, and Mr. W.-Y. Lo of Himax Technologies Inc., Taiwan, for their valuable technical discussions.

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