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Electrical Enhancement of Polycrystalline Silicon Thin-Film Transistors Using Fluorinated Silicate Glass Passivation Layer

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Polycrystalline silicon thin-film transistors (poly-Si TFTs) with a fluorinated silicate glass (FSG) passivation layer are proposed and demonstrated in this study. Experimental results reveal that the electrical characteristics can be improved by the incorporation of appropriate amounts of fluorine in the poly-Si film. The poly-Si TFTs with a FSG passivation layer show a high on-current, a low off-state gate-induced drain leakage (GIDL) current, a high field-effect mobility, and a suppressed kink effect, compared with the poly-Si TFTs with an undoped SiO_2 passivation layer. The presence of incorporated fluorine atoms from the FSG passivation layer in the poly-Si channel film can passivate the trap states at the grain boundaries. Furthermore, the incorporation of fluorine atoms can form stronger Si–F bonds near the source and drain sides to enhance the immunity against hot-carrier stress. In addition, the proposed poly-Si TFTs are easy to fabricate, have a low production cost, and are realized using a process compatible with modern TFT manufacturing technology. [DOI: 10.1143/JJAP.47.847]

KEYWORDS: fluorinated silicate glass (FSG), fluorine passivation, thin-film transistors (TFTs), solid phase crystallization (SPC)

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in many applications, including active matrix liquid crystal displays (AMLCDs).[1,2] High-performance and superior-reliability poly-Si TFTs are have the potential to enable the integration of peripheral driving circuits and pixel switching elements on a single glass substrate, and to satisfy the requirements of system-on-panel (SOP) technology.[3] To achieve high-performance poly-Si TFTs, low-temperature technology is required for realizing flat-panel displays (FPDs) owing to the maximum process temperature being limited to 600 °C. The solid-phase crystallization (SPC) process is a widely applied method for phase transformation from amorphous to polycrystalline due to its low cost and fine grain-size uniformity. However, the electrical characteristics of SPC poly-Si TFTs are strongly dependent on the microstructure of poly-Si channel film. In particular, the intra-grain defects and grain boundaries in the poly-Si film act as scattering centers, and midgap trap states can degrade the carrier's transport properties and increase the off-state leakage current of the SPC poly-Si TFTs.[4–6] Appling hydrogen-based plasma treatment is a widely used method to reduce the trap states at the grain boundaries in modern TFT manufacturing.[7,8] The reduction of trap states may contribute to the decrease in the unfavorable off-state leakage current, thereby leading to improved electrical characteristics in poly-Si TFTs. Although hydrogen-based plasma treatment can improve the electrical performances, it is difficult to control the optimal processing time for satisfactory performance improvements.[7,8] In addition, hydrogenated poly-Si TFTs also suffer from a serious instability of electrical characteristics under long-term electrical stress due to the weak Si–H bonds at the grain boundaries.[9]

Recently, alternative technologies for passivating the trap states of poly-Si TFT have been developed.[10–12,16] Several research studies have demonstrated the application of fluorine ion implantation techniques to improve the electrical characteristics of poly-Si TFTs by eliminating the trap states at the grain boundaries.[10–12] It was found that the fluorine atoms in the poly-Si film and piled up at the interface of gate oxide and poly-Si (gate oxide/poly-Si) can passivate the dangling bonds and release the strain bonds. In addition, the fluorine-implanted poly-Si TFT has stronger Si–F bonds that are more stable than weaker Si–H and Si–Si bonds in the poly-Si channel, and exhibits superior electrical reliability under long-term electrical stress, compared with the poly-Si TFT without fluorine implantation. However, it is worth pointing out that an additional thermal annealing process is required to activate the fluorine ions and cure the damage created by fluorine ion implantation.[10–12] Therefore, the fluorine ion implantation technique is not suitable to large-area glass substrates.

Fluorinated silicate glass (FSG) films have also been utilized in the intermetal dielectric (IMD) layer, and in the fluorinated gate dielectric for integrated circuit (IC) manufacturing technology.[13,14] It has been demonstrated that the addition of fluorine atoms into SiO_2 can reduce the film dielectric constant to 3.2 or lower, which leads to reduced cross-talk, RC time delay, and power consumption. Using FSG film to serve as IMD can meet the requirement of multilevel interconnection in ultralarge-scale integrated circuit (ULSI) applications. Moreover, the fluorinated gate dielectric can improve the gate oxide/Si substrate interface immunity against hot-carrier impact, and exhibits better dielectric breakdown characteristics.[15] On the other hand, Kim *et al.* have proposed using the FSG film to serve as a diffusion source to introduce fluorine atoms into the poly-Si film.[16] However, this fluorine incorporation technique is a complicated manufacturing process including additional FSG film deposition and etching steps. To date, although the fluorine passivation was a well-know technology for improving the device characteristics, it is still lacking a process-compatible technique for effectively introducing fluorine atoms into poly-Si films.

In this study, we propose a simple and effective fluorine passivation technique that involves the use of a FSG passivation layer embedded in the poly-Si TFT. In the proposed fluorine passivation method, we introduce the fluorine atoms into the poly-Si channel from the FSG passivation layer. The incorporated fluorine atoms can

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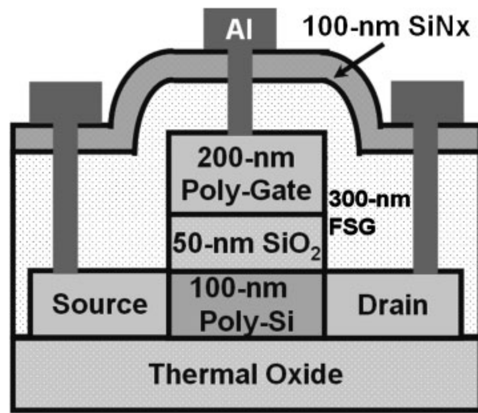

Fig. 1. Cross section of the proposed poly-Si TFT with FSG passivation layer.

passivate the trap states at the grain boundaries and also release the strain bonds at the gate oxide/poly-Si interface.[15] Consequently, the poly-Si TFTs with a FSG passivation layer are expected to exhibit high device performance and reliability. Moreover, the source/drain activation and fluorine passivation can be simultaneously accomplished without additional fabrication processes. Therefore, the proposed fluorine passivation method is very simple, low cost, and suitable for poly-Si TFT applications.

2. Experimental Procedure

The cross section of the proposed poly-Si TFTs with a FSG passivation layer is illustrated in Fig. 1. The fabrication process flow is described as follows. First, a 100-nm-thick undoped amorphous silicon (a-Si) film was deposited on a thermally oxidized Si wafer by the decomposition of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550 °C. Then, SPC was performed at 600 °C for 24 h in N_2 ambient for phase transformation from amorphous to polycrystalline. Individual active regions were patterned and defined. After a cleaning process, 50-nm-thick tetraethylorthosilicate (TEOS) oxide and 200-nm-thick poly-Si films were deposited to serve as the gate dielectric and gate electrode, respectively. After patterning and etching the poly-Si gate electrode, the gate oxide on the source and drain region (S/D) was removed in diluted HF solution to ensure the exposure of the S/D poly-Si region. A self-aligned phosphorous ion implantation was preformed to dope the S/D and gate with dosage and energy values of 5×10^{15} cm^{-2} and 40 keV, respectively. A 300-nm-thick FSG film was deposited to serve as a premetal dielectric (PMD) passivation layer in a plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C with SiH_4, N_2O, and CF_4 as precursor gases. For comparison, the undoped SiO_2 passivation layer was deposited only with the SiH_4 and N_2O precursor gases at flow rates of 20 and 60 sccm, respectively. To investigate the effect of various fluorine contents on the device performances, the SiH_4 and N_2O flow rates were adjusted at 20 and 60 sccm, and a variety of flow rates 10, 20, and 30 sccm were used to introduce CF_4 into the PECVD chamber and deposit various FSG passivation layers. The various CF_4 flow rates of 10, 20, and 30 sccm correspond to the FSG 1, FSG 2, and FSG 3 passivation layers, respectively. Since the FSG film shows poor thermal stability and the fluorine atoms may diffuse out of the FSG film during post thermal annealing, a 100-nm-thick SiN_x capping layer on the FSG film was successively deposited by PECVD clusters to improve the thermal stability of the FSG film and avoid the diffusion of fluorine atoms out of the FSG film.[17] Dopants at the source/drain and gate regions were activated at 600 °C for 12 h in N_2 ambient, followed by a definition of contact holes. Finally, a 400-nm-thick aluminum (Al) electrode was deposited and patterned. To focus on revealing the effect of fluorine content on the device performance, all samples were not prepared with an additional thermal sintering process and hydrogen plasma treatment.

3. Results and Discussion

Figure 2 illustrates the transfer characteristics (I_{DS}–V_{GS}) of the poly-Si TFTs with undoped SiO_2 passivation and various FSG passivation layers. The measurements were performed at a drain voltage of $V_{DS} = 5$ V. The drawn channel length (L) and channel width (W) of the poly-Si TFT are 0.8 and 0.8 μm, respectively. The poly-Si TFTs with various FSG passivation layers, including FSG 1, FSG 2, and FSG 3, exhibit an improved on-state characteristic, as shown in the inset of Fig. 2, and a reduced off-state leakage current compared with those with an undoped SiO_2 passivation layer. It should be noted that the off-state leakage current of the poly-Si TFT with FSG passivation layers is at least three times lower than that with an undoped SiO_2 passivation layer, especially under voltages of $V_{GS} = -10$ and $V_{DS} = 5$ V. These major device improvements can be ascribed to the fact that the fluorine-passivated poly-Si film can be achieved by the incorporation of fluorine atoms from the FSG film, and thus there must be fewer trap states at the grain boundaries in the poly-Si TFT with a FSG passivation layer.[15]

Many studies indicate that the phenomenon of moisture (H_2O) absorption in the plasma-deposited FSG film has been observed, because the Si–F bonds present are highly reactive with moisture.[18] Moreover, the amount of moisture absorbed from the atmosphere was markedly increased with increasing fluorine content in the plasma-deposited FSG film,[18,19] and thus the device performance was degraded owing to the moisture absorbed by the FSG film. Therefore,

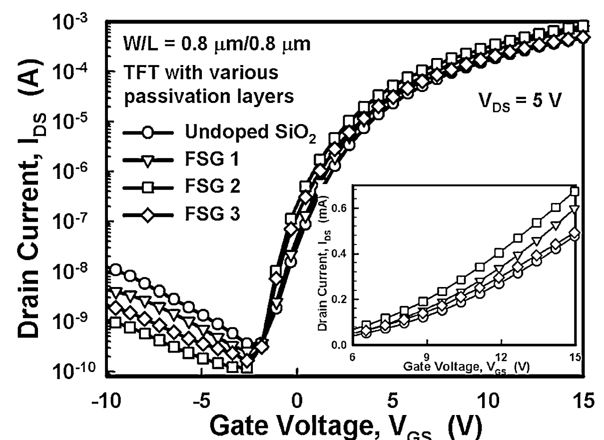

Fig. 2. Transfer characteristics of the poly-Si TFTs with undoped SiO_2 and various FSG passivation layers at $V_{DS} = 5$ V.

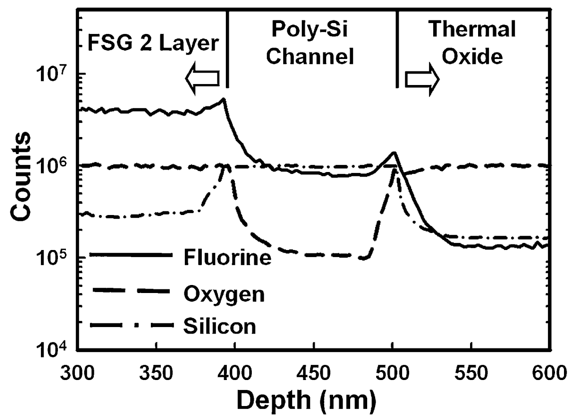

Fig. 3. SIMS depth profiles of a FSG-passivation-layer-capped poly-Si film.

in this study, we employed a SiN_x capped FSG passivation layer to prevent moisture penetration into the FSG film, the degradation of device reliability caused by the absorption of moisture from the atmosphere after device fabrication can be excluded. Nevertheless, the poly-Si TFT with a FSG 3 passivation layer still shows a detrimental effect on the electrical characteristics of the fabricated devices. The major reason may be ascribed to the following mechanism. A small number of OH bonds may exist in the FSG film, because the precursor gases of SiH_4, N_2O, and CF_4 were utilized to deposit the FSG film in the PECVD chamber,[20] As the amount of fluorine in the FSG film increases, the OH bonds can react with fluorine atoms to form HF, which corrodes the devices and degrades the electrical performance.[21] Therefore, in this study, we choose the poly-Si TFT with a FSG 2 passivation layer as the optimal structure to be compared with that with an undoped SiO_2 passivation layer.

Secondary-ion mass spectrometry (SIMS) analysis is used to verify the incorporation of fluorine atoms in the poly-Si film. A test sample with a SiN_x capped FSG 2 passivation layer on a poly-Si film was used to simulate the actual device process with dopant activation annealing carried out at 600 °C for 12 h. Figure 3 shows the SIMS profiles of the fluorine, silicon, and oxygen atoms for the poly-Si film with a FSG 2 passivation layer. It is clearly observed that a considerable number of fluorine atoms can be introduced into the poly-Si film by the FSG passivation layer technique. Moreover, the SIMS analysis also shows fluorine atoms at a high concentration appearing at the top interface of the FSG 2/poly-Si layers and at the bottom interface of the poly-Si/thermal oxide layers. This indicates that the fluorine atoms tended to accumulate at the interface of the poly-Si/SiO_2 layers after the thermal annealing process. These piled-up fluorine atoms located at the top interface of the FSG 2/poly-Si layers and at the bottom interface of the poly-Si/thermal oxide layers can provide an effective passivation of trap states. Therefore, we believe that the weak and dangling bonds, associated with interface and trap states, at the top interface of the FSG 2/poly-Si layers and in the poly-Si film are passivated by fluorine atoms, leading to the enhanced electrical characteristics.[15)]

The transfer characteristics (I_{DS}–V_{GS}) of the poly-Si TFTs with undoped SiO_2 passivation and FSG 2 passivation layers

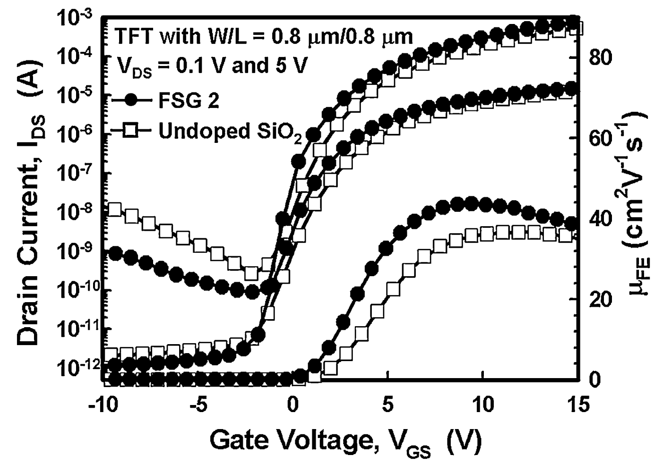

Fig. 4. Transfer and field-effect mobility vs gate voltage characteristics for the poly-Si TFTs with undoped SiO_2 and FSG 2 passivation layers at $V_{DS} = 0.1$ and 5 V.

Table I. Comparison of device characteristics of the poly-Si TFTs with undoped SiO_2 and FSG 2 passivation layers.

	V_{TH} (V)	S.S. (mV/dec)	μ_{FE} ($cm^2 V^{-1} s^{-1}$)	I_{GIDL} (nA)	I_{ON}/I_{OFF} (10^6)
Undoped SiO_2	2.26	845	36.7	12.5	2.47
FSG 2	1.42	747	43.8	1.15	7.54

are compared separately as shown in Fig. 4. The measurements are performed at drain voltages of $V_{DS} = 0.1$ and 5 V. The parameters of the devices, including the threshold voltage (V_{TH}), subthreshold swing (S.S.), and field-effect mobility (μ_{FE}), are extracted at $V_{DS} = 0.1$ V, whereas the maximum off-state gate-induced drain leakage (GIDL) current (I_{GIDL}) is defined at $V_{DS} = 5$ V and $V_{GS} = -10$ V, and the ON/OFF current ratio is defined as the ratio of maximum on-state current to minimum off-state current at $V_{DS} = 5$ V. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of $I_{DS} = (W/L) \times 100$ nA. The extracted device parameters are summarized in Table I.

Accordingly, the electrical performances of the poly-Si TFT with a FSG 2 passivation layer are significantly improved, for example, threshold voltage was decreased from 2.26 to 1.42 V and S.S. was reduced from 845 to 747 mV/dec, as compared with those with an undoped SiO_2 passivation layer. It is known that threshold voltage and subthreshold swing are strongly affected by the Si dangling bonds, associated with the deep trap states, which have energy states near the middle of the silicon bandgap.[8] Therefore, using the FSG passivation layer technique can effectively introduce the fluorine atoms into the poly-Si film to passivate the trap states at the grain boundaries. Moreover, the ON/OFF current ratio and off-state leakage current of the poly-Si TFTs with a FSG 2 passivation layer are better than those of the poly-Si TFTs with an undoped SiO_2 passivation layer. It should be noted that the ON/OFF current ratio of the poly-Si TFT with a FSG 2 passivation layer is approximately three times larger than that of the poly-Si TFT with an undoped SiO_2 passivation layer. The

poly-Si TFT with a FSG 2 passivation layer exhibits a more than one order of magnitude reduction in the maximum off-state GIDL current (I_{GIDL}) compared with that with an undoped SiO_2 passivation layer, especially under a continuously decreasing gate voltage of $V_{GS} = -10$ V and $V_{DS} = 5$ V. As is well known, the off-state GIDL current in the poly-Si TFT mainly results from the field-enhanced emission via the trap states of grain boundaries near the drain side under a high vertical electric field.[22] The result observes that the trap states in the poly-Si film can be eliminated by the incorporation of fluorine atoms from the FSG passivation layer.

Figure 4 also illustrates the field-effect mobility versus gate voltage characteristics of the poly-Si TFTs with undoped SiO_2 passivation and FSG 2 passivation layers. The field-effect mobility is extracted from the value of transconductance at $V_{DS} = 0.1$ V. As can be seen, the maximum field-effect mobility of the poly-Si TFT with a FSG 2 passivation layer is higher than that of the poly-Si TFT with an undoped SiO_2 passivation layer. The poly-Si TFT with the FSG 2 passivation layer shows an approximately 19% enhancement in the maximum field-effect mobility compared with that with an undoped SiO_2 passivation layer. Note that the strain bonds, associated with the tail states near the silicon band edge, in the poly-Si film and at the gate oxide/poly-Si interface will greatly affect the field-effect mobility.[15] The improvement of field-effect mobility can be attributed to the passivated Si dangling bonds and released strain bonds brought about by the incorporation of fluorine atoms.

To verify the effect of fluorine passivation, the effective grain-boundary trap state density (N_{trap}) was calculated from the square root of the slope of $\ln[I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ plots according to the grain-boundary trapping model proposed by Levinson *et al.* and Proano *et al.*[23,24] Figure 5 shows the $\ln[I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ curves at $V_{DS} = 0.1$ V and a high gate voltage for the poly-Si TFTs with undoped SiO_2 passivation and FSG 2 passivation layers. It can be found that the poly-Si TFT with a FSG 2 passivation layer shows a N_{trap} of around 9.2×10^{12} cm^{-2}, whereas the control one possesses a

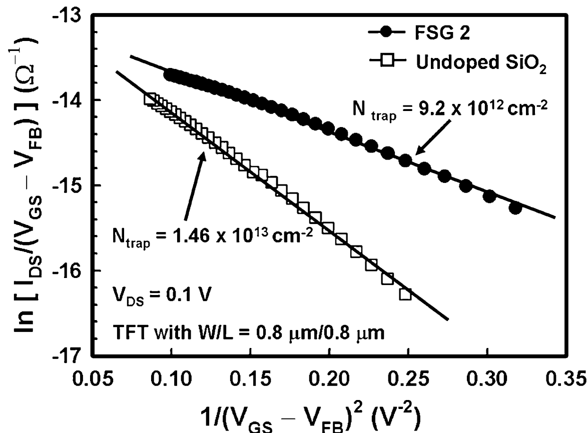

Fig. 5. Plot of $\ln[I_{DS}/(V_{GS} - V_{FB})]$ vs $1/(V_{GS} - V_{FB})^2$ and the extracted effective grain boundary trap state densities of the poly-Si TFTs with undoped SiO_2 and FSG 2 passivation layers. I_{DS} was measured at $V_{DS} = 0.1$ V and high V_{GS}.

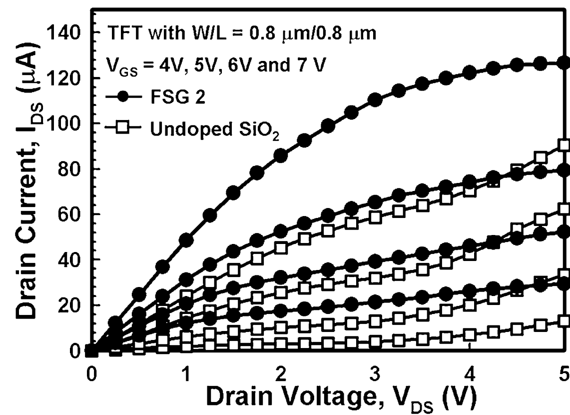

Fig. 6. Output characteristics of the poly-Si TFTs with undoped SiO_2 and FSG 2 passivation layers.

N_{trap} of 1.46×10^{13} cm^{-2}. This result strongly implies that fluorine atoms incorporated from the FSG 2 layer can effectively passivate the trap states of grain boundaries in the poly-Si film.

Figure 6 shows the output characteristics (I_{DS}–V_{DS}) of poly-Si TFTs with undoped SiO_2 passivation and FSG 2 passivaton layers, exhibiting an improvement of the drain current for the poly-Si TFT with a FSG 2 passivaton layer at $V_{GS} = 4$, 5, 6, and 7 V, respectively. This is due to the field-effect mobility and threshold voltage of the poly-Si TFT with a FSG 2 passivaton layer being higher and lower than those of the poly-Si TFT with an undoped SiO_2 passivation layer, respectively. Moreover, as the devices are operated in the saturation region, the drain current markedly increases with increasing drain voltage. This unfavorable phenomenon resulting from the channel avalanche multiplication under a high lateral electric field and a floating body was referred to as the kink effect.[25] The poly-Si TFT with a FSG 2 passivation layer can significantly suppress the kink effect compared with that with an undoped SiO_2 passivation layer, which is attributed to fewer incidences of the channel avalanche multiplication of hot carriers.

The Si dangling bonds, associated with the trap states at the grain boundaries, can be passivated with fluorine atoms to from stronger Si–F bonds instead of weaker Si–H and Si–Si bonds, thereby resulting in the inhibition of the channel avalanche multiplication of hot carriers. Therefore, as the impact ionization rate of hot carriers is suppressed by the formation of stronger Si–F bonds, the kink effect can be suppressed in the poly-Si TFT with a FSG 2 passivation layer.

On the basis of the above results, a schematic cross-sectional diagram the proposed poly-Si TFT with a SiN_x capped FSG passivation layer is illustrated in Fig. 7. After the deposition of the FSG passivation layer and capping SiN_x film, dopants at the source/drain and gate are activated at 600 °C for 12 h in N_2 ambient. Since a SiN_x capping layer can prevent the fluorine atoms from outgassing,[17] the incorporated fluorine atoms would diffuse into the poly-Si film due to the thermal budget. Therefore, using the FSG passivation layer technique, the fluorine atoms can passivate the trap states at the grain boundaries to improve the device performance, and form stronger Si–F bonds to enhance the

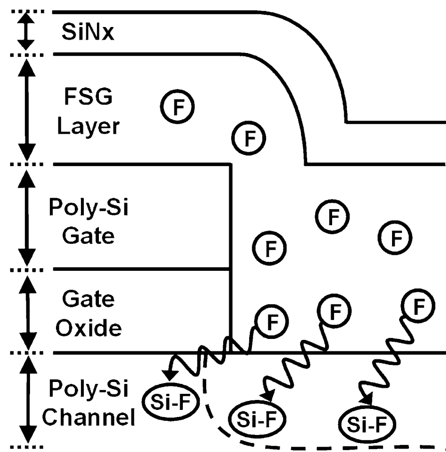

Fig. 7. Schematic cross-sectional diagram of the proposed poly-Si TFT with a SiN capped FSG passivation layer.

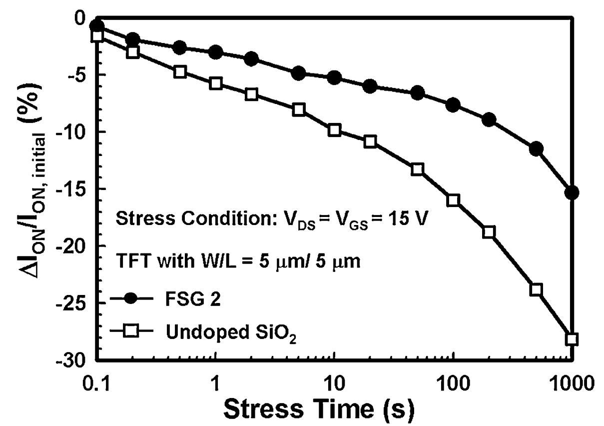

Fig. 9. On-current variation as a function of hot-carrier stress time for the poly-Si TFTs with undoped SiO_2 and FSG 2 passivation layers.

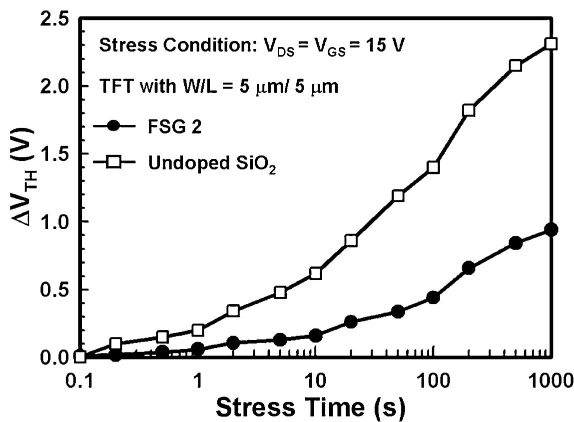

Fig. 8. Threshold voltage variation as a function of hot-carrier stress time for the poly-Si TFTs with undoped SiO_2 and FSG 2 passivation layers.

immunity of hot carrier against channel avalanche multiplication.

Additionally, hot-carrier stress was applied to investigate the electrical reliability of the poly-Si TFT devices. The poly-Si TFTs were bias stressed at $V_{DS} = 15$ V and $V_{GS} = 15$ V for 1000 s, and the devices with dimensions of $W/L = 5\,\mu m/5\,\mu m$ were used to examine the hot-carrier immunity against stress. The shift of threshold voltage (V_{TH}) and variation of on-current (I_{ON}) versus hot-carrier stress time for poly-Si TFTs with undoped SiO_2 passivation and FSG 2 passivation layers are shown in Figs. 8 and 9, respectively. The shift of V_{TH} and variation of I_{ON} are defined as $(V_{TH,\,stressed} - V_{TH,\,initial})$ and $(I_{ON,\,stressed} - I_{ON,\,initial})/I_{ON,\,initial} \times 100\%$, respectively, where the subscripts of "initial" and "stressed" represent the measured data before and after stress application, respectively. Hot carrier multiplication near the drain side causes the degradation of threshold voltage and on-current. A more severe degradation of threshold voltage and on-current is observed in the poly-Si TFT with an undoped SiO_2 passivation layer. Notably, the threshold-voltage shift and the variation of on-current of the poly-Si TFT with a FSG 2 passivation layer after a stress time of 1000 s are found to be 0.95 V and 15.5%, which are superior to those of the poly-Si TFT with an undoped SiO_2 passivation layer (2.3 V and 28%), respectively. It is well known that the threshold voltage and on-current are strongly dependent on the deep trap states, that originate from the weak Si–Si and Si–H dangling bonds at the grain boundaries near the drain side.[26,27] Therefore, in the case of poly-Si TFTs with a FSG 2 passivation layer, the fluorine atoms incorporated near the drain side from the FSG 2 passivation layer will passivate the Si dangling bonds to from Si–F bonds. These results further imply that in poly-Si TFT fabricated with the FSG passivation layer, the bonding energy of formed Si–F bonds is higher than that of weaker Si–Si and Si–H bonds in the poly-Si channel, and Si–F bonds are less easily broken than Si–Si and Si–H bonds under hot-carrier stress, thereby resulting in improved electrical reliability.

4. Conclusions

We have successfully proposed and demonstrated a novel poly-Si TFT with a FSG film as a premetal dielectric (PMD) passivation layer. The poly-Si TFT with an appropriate fluorine incorporation in the FSG passivation layer shows a significant improvement in its electrical performances including a steeper subthreshold swing, a smaller threshold voltage, a higher field-effect mobility, and a lower off-state leakage current than in the case of the poly-Si TFT with an undoped SiO_2 passivation layer. These major electrical performance enhancements may be ascribed to the reduction of trap and interface states in the poly-Si and at the gate oxide/poly-Si interface, respectively, realized using this fluorine passivation layer technique.

Moreover, the poly-Si TFT with an appropriate FSG passivation layer exhibits a suppressed kink effect owing to the reduced impact ionization rate of hot carriers, and promotes better hot-carrier immunity against stress, thereby leading to an on-current saturation behavior and an electrical reliability better than those of the poly-Si TFT with an undoped SiO_2 passivation layer. It is concluded that the FSG premetal dielectric passivation layer technique can provide a simple, effective, and process-compatible method of introducing fluorine atoms into poly-Si film. Fabricating poly-Si TFTs with the FSG passivation layer at an appropriate fluorine content can improve not only the electrical performance but also the electrical reliability.

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