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Electrical Properties of High-κ Praseodymium Oxide Polycrystalline Silicon Thin-Film Transistors with Nitrogen Implantation

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This paper demonstrates the polycrystalline silicon (poly-Si) thin-film transistors (TFTs) with high-κ praseodymium oxide (Pr_2O_3) gate dielectric and nitrogen implantation to achieve high-performance characteristics for the first time. Nitrogen atoms with various dosages are implanted into amorphous silicon (α-Si) film to passivate the grain boundary trap states during solid-phase crystallization (SPC) annealing. From experimental results, the electrical characteristics of the Pr_2O_3 poly-Si TFT implanted with the nitrogen dosage of $5 \times 10^{12}\,cm^{-2}$ could be greatly improved. In addition, a better hot-harrier immunity of high-κ Pr_2O_3 poly-Si TFT could be also obtained. [DOI: 10.1143/JJAP.47.853]

KEYWORDS: polycrystalline silicon (poly-Si) thin-film transistor (TFT), praseodymium oxide (Pr_2O_3), nitrogen implantation, solid-phase crystallization (SPC)

1. Introduction

Recently, polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used for pixel elements and driving circuits in active-matrix liquid-crystal displays (AMLCDs) to realize system-on-panel (SOP) technology.[1–3] Because poly-Si TFTs are fabricated on inexpensive glass substrate, low-temperature process is required for the realization of commercial flat-panel displays (FPDs). The solid-phase crystallization (SPC) process with maximum process temperature limiting to 600 °C is widely used to recrystallize amorphous silicon (α-Si) film due to its low production cost and good grain-size uniformity.[4,5] However, only by using SPC technology, it is difficult to develop a high-performance poly-Si TFT with low threshold voltage, low subthreshold swing, and high driving current to drive the liquid crystal on a large size panel. In order to break through this challenge, integrating high-κ gate dielectric into poly-Si TFT was proposed to increase the gate capacitance density for keeping a high current drivability and a low gate leakage.[6–8]

In addition, trap states at interface and grain boundaries could be rapidly filled up to improve the subthreshold swing by using high-κ dielectric applied on poly-Si TFT.[7,8] However, such high gate capacitance density would contribute to a high electric field at the gate-to-drain overlap area, resulting in rather high field-enhanced emission rates via the grain-boundary trap states.[9,10] Therefore, the poly-Si TFTs with high-κ gate dielectrics would suffer from more undesirable gate-induced drain leakage (GIDL) currents. In order to alleviate the GIDL current issues, the hydrogenated plasma treatment was proposed to introduce the hydrogen atoms into the poly-Si film to effectively passivate the grain-boundary trap states near the drain side.[11–13] Nevertheless, the hydrogenated TFTs suffer from a serious instability issue owing to lots of easily breaking Si–H bonds in poly-Si film.[14]

In this paper, we successfully demonstrated the nitrogen-implanted technique applied on the poly-Si TFTs with high-κ gate dielectric praseodymium oxide (Pr_2O_3). The electrical characteristics and reliability of the Pr_2O_3 poly-Si TFTs could be significantly improved by employing the nitrogen-incorporation technique. Therefore, our proposed Pr_2O_3 poly-Si TFTs with nitrogen-implanted poly-Si films could satisfy the matrix devices and high-speed driving circuit applications.

2. Experimental Procedure

The main fabrication steps are summarized below and shown in Fig. 1. First, the 500-nm thermal oxide was grown on 6-in. Si wafer and used to simulate the glass substrate. And then, an undoped α-Si film with 50 nm thick was deposited by using low-pressure chemical vapor deposition (LPCVD) system at 550 °C. Following, the nitrogen atoms with various dosages of 0 (control sample), $5 \times 10^{12}\,cm^{-2}$, and $5 \times 10^{13}\,cm^{-2}$, were implanted into the 50-nm α-Si film with an ion implantation energy of 10 keV, as shown in Fig. 1(a). The ion implantation energy of 10 keV was chosen so that the projected range of the nitrogen atoms is about 25 nm, the half of the thickness of α-Si film. After nitrogen

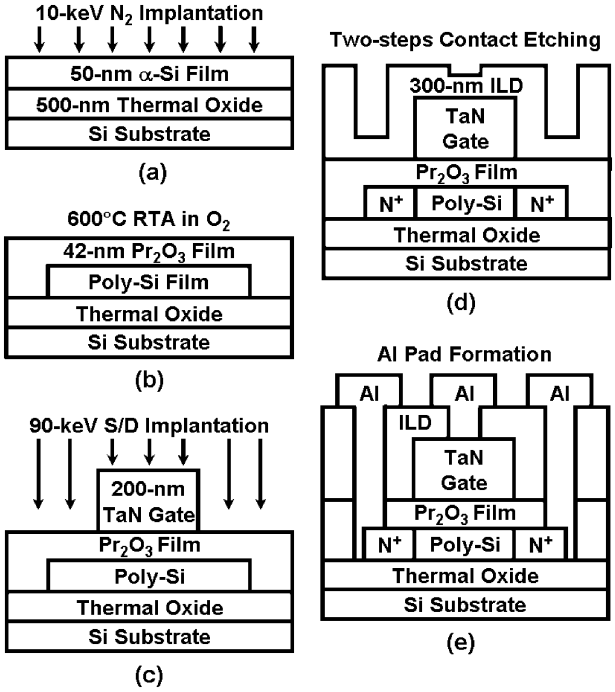

Fig. 1. The main process steps of the Pr_2O_3 poly-Si TFT with nitrogen-implanted poly-Si film.

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implantation, the conventional SPC annealing was processed at 600 °C for 24 h in nitrogen ambient to crystallize α-Si film into poly-Si film. Subsequently, the active regions were defined, and then the Pr_2O_3 gate dielectric film was deposited by physical vapor deposition (PVD) system. Following, the Pr_2O_3 gate dielectric was subjected to rapid thermal annealing (RTA) at 600 °C for 1 min in oxygen ambient to improve the quality of Pr_2O_3 gate dielectric, as shown in Fig. 1(b).

The 200-nm tantalum nitride (TaN) film was deposited by PVD system and used to be metal gate electrode of thin-film transistor. After TaN film was deposited, the chlorine-based plasma etching process capable of stopping on the Pr_2O_3 layer was used to pattern the TaN metal gate electrode. As shown in Fig. 1(c), a self-aligned phosphorus implantation was performed with the dosage and the energy of $5 \times 10^{15}\,cm^{-2}$ and 90 keV, respectively. And then, phosphorus dopants in source and drain regions were activated by RTA process at 600 °C for 1 min in nitrogen ambient. After 300-nm tetraethoxylsilane (TEOS) oxide film used as inter-layer dielectric (ILD) passivation was deposited by plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C, the contact holes were patterned by two-step contact etching process, as shown in Fig. 1(d). The 300-nm ILD passivation and Pr_2O_3 gate dielectric on source and drain regions were sequentially removed by buffered oxide etch (BOE) and $H_3PO_4 : HNO_3 : CH_3COOH : H_2O$ (50 : 2 : 10 : 9) mixed solution. Since such mixed solution has rather high etching selectivity of the Pr_2O_3 film to the ILD passivation, the Pr_2O_3 film could be completely etched away by an excess over etching. After the contact holes were etched, the aluminum (Al) film of 500 nm was deposited by PVD system. Finally, the Al pad was patterned, as shown in Fig. 1(e), and then the nitrogenous poly-Si TFTs with Pr_2O_3 gate dielectric were accomplished. For comparison, the control poly-Si Pr_2O_3 TFT without the nitrogen implantation ($D_N = 0$) was also prepared by the same process flow. In addition, note that all poly-Si TFTs had no plasma treatment in this work.

3. Results and Discussion

The capacitance–voltage (C–V) characteristic and the leakage current density of the Pr_2O_3 film on Si substrate are shown in Fig. 2. The Pr_2O_3 films on Si substrate and on poly-Si film are fabricated at the same process. From the cross-sectional transmission electron microscope (TEM) image of the proposed poly-Si TFT in inset of Fig. 2, the thickness of Pr_2O_3 gate dielectric after RTA treatment in oxygen ambient is about 42 nm and the thickness of poly-Si channel is around 50 nm. The leakage current of the 42-nm Pr_2O_3 gate dielectric on Si substrate is below $1\,\mu A/cm^2$ before the thin-film breakdown about 7 MV/cm. The accumulation capacitance density (C_{acc}) at the applied voltage of $V_{APP} = -4$ V is $432\,nF/cm^2$. Therefore, the equivalent-oxide thickness (EOT) and the effective dielectric constant value (κ) of 42-nm Pr_2O_3 gate dielectric extracted from the accumulation capacitance density are 8 nm and 25, respectively. Such high capacitance density and low leakage current represent that the Pr_2O_3 thin film is a good candidate for gate dielectric application. Therefore, it could be expected that the poly-Si TFT with the Pr_2O_3 gate dielectric has a well gate controllability resulting in better electrical characteristics compared to that with conventional plasma TEOS oxide as gate dielectric.

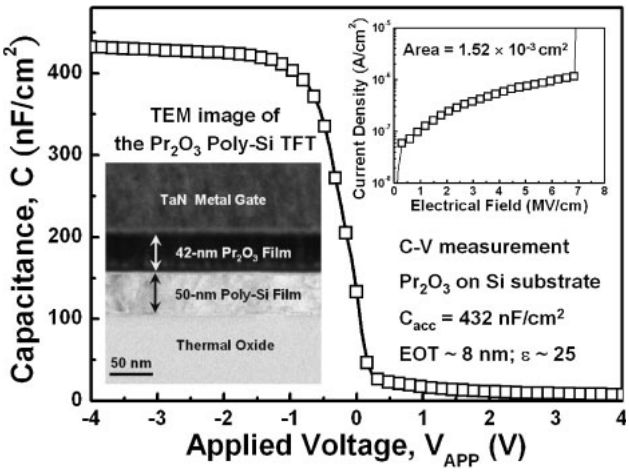

Fig. 2. The C–V characteristic and leakage current density of the Pr_2O_3 film on Si substrate. The insert is the cross-sectional TEM image of the proposed Pr_2O_3 poly-Si TFT.

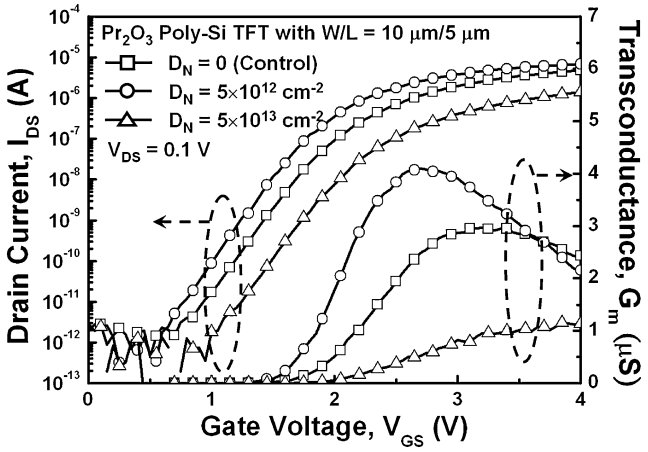

Fig. 3. The transfer characteristics of the Pr_2O_3 poly-Si TFTs with various nitrogen dosages of 0 (control sample), $5 \times 10^{12}\,cm^{-2}$, and $5 \times 10^{13}\,cm^{-2}$ under $V_{DS} = 0.1$ V.

Figure 3 shows the transfer characteristics (I_{DS}–V_{GS}) of the Pr_2O_3 poly-Si TFTs with various nitrogen dosages (D_N) of 0 (control sample), $5 \times 10^{12}\,cm^{-2}$, and $5 \times 10^{13}\,cm^{-2}$, which are measured at $V_{DS} = 0.1$ V. The channel length (L) and the channel width (W) of the Pr_2O_3 poly-Si TFT are 10 and 5 μm, respectively. When the nitrogen dosage is increased to $5 \times 10^{12}\,cm^{-2}$, the performance of the Pr_2O_3 poly-Si TFTs could be improved, including threshold voltage (V_{TH}) and transconductance (G_m). The transconductance is defined as $\partial V_{GS}/\partial \ln I_{DS}$ measured in the switching region. However, the subthreshold swings (S.S.) of the Pr_2O_3 poly-Si TFTs seem no change with various nitrogen dosages. As the papers reported,[15,16] the interface traps states and the grain boundary trap states dominate the electrical characteristics of poly-Si TFT. The deep trap states at grain boundaries mainly affect on threshold voltage but less on transconductance. Besides, the tails states at the interface and grain boundaries mainly contribute to the degradation of transconductance. The subthreshold swing

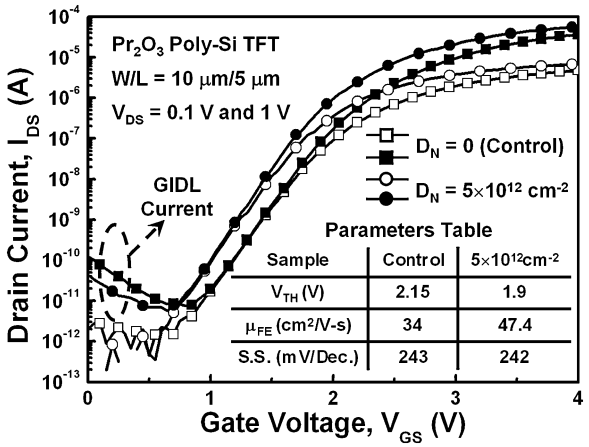

Fig. 4. The transfer characteristics (I_{DS}–V_{GS}) of the Pr_2O_3 poly-Si TFTs with the nitrogen dosages of 0 and $5 \times 10^{12}\,cm^{-2}$ under $V_{DS} = 0.1$ and 1 V. The inset is the table of the electrical parameters.

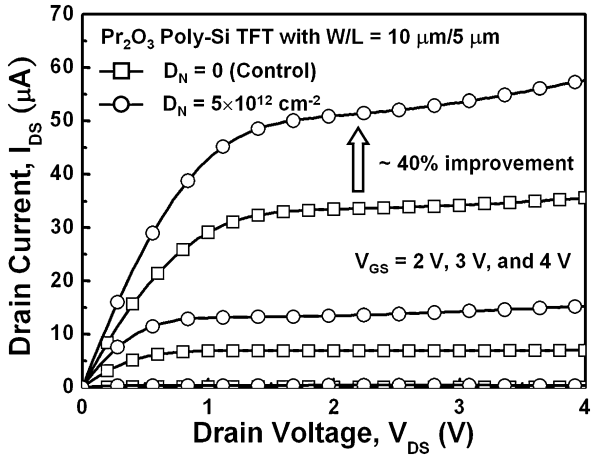

Fig. 5. The output characteristics (I_{DS}–V_{DS}) of the Pr_2O_3 poly-Si TFTs with nitrogen dosages of 0 and $5 \times 10^{12}\,cm^{-2}$.

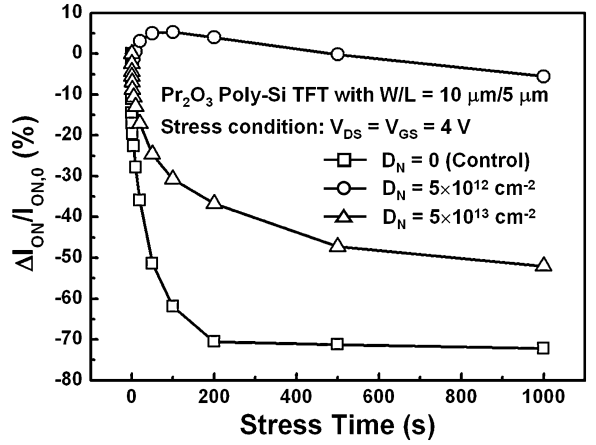

Fig. 6. The drain current degradation for the Pr_2O_3 poly-Si TFTs with and without nitrogen implantation under hot-carrier stress condition.

mainly depends on the deep interface traps states.[16] As shown in Fig. 3, such the same subthreshold swings mean that the interface traps states at the Pr_2O_3 gate dielectric/poly-Si channel interface are not changed with various nitrogen dosages. Therefore, the electrical improvement of the Pr_2O_3 poly-Si TFT by using nitrogen implantation could be attributed to the reduction of the grain boundary trap states within poly-Si film during conventional SPC annealing. However, when the nitrogen dosage is increased to $5 \times 10^{13}\,cm^{-2}$, the electrical characteristics the Pr_2O_3 poly-Si TFT would be degraded. The overdose of nitrogen implantation ($D_N = 5 \times 10^{13}\,cm^{-2}$) in α-Si film would obstruct α-Si film crystallized to poly-Si film compared to that without nitrogen implantation (control sample). Therefore, the turn-on current of the Pr_2O_3 poly-Si TFT without large size of poly-Si grains is decreased.

Figure 4 compares the transfer characteristics (I_{DS}–V_{GS}) of the Pr_2O_3 poly-Si TFTs with nitrogen dosages of 0 and $5 \times 10^{12}\,cm^{-2}$ under $V_{DS} = 0.1$ and 1 V. The insert table summarizes the electrical parameters. The threshold voltage (V_{TH}) is defined as the gate voltage required a normalized drain current of $I_{DS} = (W/L) \times 100\,nA$ at $V_{DS} = 0.1$ V. The ON/OFF current ($I_{ON,\,max}/I_{OFF,\,min}$) ratio is defined as that ratio of the maximum on-state current to the minimum off-state current at $V_{DS} = 1$ V. The threshold voltage (V_{TH}), field-effective mobility (μ_{FE}) could be improved from 2.15 to 1.9 V and 34 to $47.4\,cm^2\,V^{-1}\,s^{-1}$, respectively. However, the S.S. and ON/OFF current ratio of them are almost the same with the value about 242 mV/dec and over the sixth power of ten, respectively. Besides, the GIDL current at $V_{DS} = 1$ V and $V_{GS} = 0$ V could be also suppressed by a half-order magnitude by using nitrogen implantation with suitable dosage of $5 \times 10^{12}\,cm^{-2}$. The GIDL current in poly-Si TFT results from the field-enhanced emission through the trap states near the drain side.[13] Using moderate dosage of nitrogen atoms implanted into the poly-Si film can effectively passivate the trap states at grain boundaries, and thus lead to reduce GIDL current.

The output characteristics (I_{DS}–V_{DS}) of the Pr_2O_3 poly-Si TFTs with nitrogen dosages of 0 and $5 \times 10^{12}\,cm^{-2}$ are shown in Fig. 5. The driving current of the Pr_2O_3 poly-Si TFT with nitrogen implantation has about 40% improvement at $V_{GS} = 4$ V, compared to the control sample. The pervious studies[6–8] have been reported that using various high-κ gate dielectrics on poly-Si TFTs could quickly fill the trap states in poly-Si channel to improve device electrical characteristics due to its well gate controllability. However, in this work, using the nitrogen implantation technique on the Pr_2O_3 poly-Si TFTs will further passivate these trap states in poly-Si film and improve the device performance.

Finally, the hot-carrier reliability on the Pr_2O_3 poly-Si TFTs with and without the nitrogen implantation is investigated in Fig. 6. All devices are biased at $V_{GS} = V_{DS} = 4$ V, which is a hot-carrier stress condition. The degradation of drain current is defined as $\Delta I_{ON}/I_{ON,0}$, where the $\Delta I_{ON} = I_{ON,s} - I_{ON,0}$, $I_{ON,0}$ is initial I_{ON}, and $I_{ON,s}$ is the I_{ON} for each stress time. The degradation of I_{ON} of the Pr_2O_3 poly-Si TFT with nitrogen dosages (D_N) of $5 \times 10^{12}\,cm^{-2}$ is about 5% after 1000-s hot-carrier stress, which is superior to that without nitrogen implantation (control sample). The I_{ON} degradation of control sample would be saturated at −70% after 200-s hot-carrier stress. It is reported that the hot-carrier stress easily breaks the weak Si–Si and Si–H bonds (with the bonding energy of 70 kcal/mol) to generate the interface states and grain boundary states in poly-Si film.[14,17] If the moderate dosage of nitrogen is implanted

into α-Si film during SPC annealing, the stronger Si–N bonds with a higher bonding energy of 81 kcal/mol would replace the weak Si–Si and Si–H bonds to achieve excellent hot-carrier endurance.[17] It would be note that the Pr_2O_3 poly-Si TFT with nitrogen dosages of $5 \times 10^{13}\,cm^{-2}$ even has a higher stress current that is under more serious hot-carrier stress condition than that without nitrogen implantation. On the other hand, for the Pr_2O_3 poly-Si TFT with nitrogen dosages of $5 \times 10^{13}\,cm^{-2}$, its I_{ON} degradation would be saturated at -50% after 400-s hot-carrier stress, which seems better than control sample ($D_N = 0$). This reason could be attributed to that the overdose of nitrogen implantation would restrict α-Si film crystallization and result in the inferior electrical characteristics of the Pr_2O_3 poly-Si TFT, as shown in Fig. 3. The hot-carrier stress condition on device with nitrogen dosages of $5 \times 10^{13}\,cm^{-2}$ is more alleviative than control sample under the same stress biased. In summary, the Pr_2O_3 poly-Si TFT with applicable nitrogen incorporation in poly-Si channel has better immunity on the hot-carrier stress, compared to the control sample.

4. Conclusions

High-performance poly-Si TFTs integrated nitrogen implantation and Pr_2O_3 gate dielectric are demonstrated for the first time. High gate capacitance density and high breakdown electrical field are introduced from the Pr_2O_3 gate dielectric and TaN metal gate. The electrical characteristics and reliability are significantly improved by nitrogen implantation technique into the poly-Si TFT with Pr_2O_3 gate dielectric without additional plasma treatment. Therefore, the proposed Pr_2O_3 poly-Si TFT with nitrogen implantation would be a promising candidate for matrix devices and high-speed driving circuit applications in the future.

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