Analysis of Negative Bias Temperature Instability in Body-Tied Low-Temperature Polycrystalline Silicon Thin-Film Transistors

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***Abstract*—Negative bias temperature instability (NBTI) degradation mechanism in body-tied low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) is analyzed by the charge-pumping (CP) technique. The properties of bulk trap states (including interface and grain boundary trap states) are directly characterized from the CP current. The increase of the fixed oxide charges is also extracted, which has not been quantified in previous studies of NBTI degradation in LTPS TFTs. The experimental results confirm that the NBTI degradation in LTPS TFTs is caused by the generation of bulk trap states and oxide trap states.**

***Index Terms*—Charge-pumping (CP) technique, low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs), negative bias temperature instability (NBTI).**

I. INTRODUCTION

LOW-TEMPERATURE polycrystalline silicon thin-film transistors (LTPS TFTs) are attracting much research interest as potential candidates for the realization of system on panel (SOP). For driving circuit operation, LTPS TFTs must be designed using the CMOS inverter configuration. During operation, p-channel TFT will be subjected to negative bias temperature instability (NBTI) when the input is at a low voltage level and the output is at a high voltage level. In MOSFETs, it is well accepted that the NBTI degradation originates from the breaking of the hydrogenated silicon (Si–H) bonds, resulting in the generation of interface and oxide trap states [1]–[3]. However, in LTPS TFTs, due to the existence of trap states in the grain boundaries and at the poly-Si/SiO$_2$ interface, more Si–H bonds may be found in the channel region than with MOSFETs. Further, due to the poor thermal conductivity of the glass substrate and high operating voltage, NBTI can be an important reliability issue for LTPS TFTs. Therefore, it is important to study NBTI behaviors and the related degradation mechanisms of LTPS TFTs.

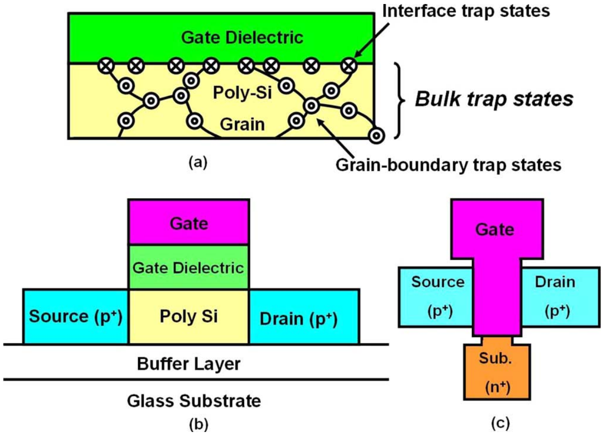

Fig. 1. (a) Schematic cross-sectional view of the critical poly-Si/SiO$_2$ interface showing interface trap states and grain boundary trap states. (b) Cross-sectional and (c) top views of the LTPS TFT used in this letter.

NBTI has been reported to degrade the channel film of LTPS TFTs [4]. In previous studies, the channel properties have been found to be derived from the current–voltage characteristics. However, the channel current is affected through the potential barrier formed by the trap states [5]. Therefore, the bulk trap-state density (N_{bulk}) derived from the channel current does not indicate the real bulk trap-state density, but the effective bulk trap-state density. Koyanagi and coworkers [6], [7] and Balasinski and coworkers [8]–[10] proposed the charge-pumping (CP) technique to directly characterize the bulk trap properties of poly-Si TFTs. Unlike in MOSFETs, in LTPS TFTs, the grain boundary trap states also give rise to the CP current (I_{CP}). Consequently, N_{bulk} as measured by the CP technique consists of both the grain boundary and interface trap states, as shown in Fig. 1(a). N_{bulk} can be revealed from I_{CP} because carriers are observed as the generation–recombination current. As a result, the influence of N_{bulk} is directly evaluated. However, use of this technique to analyze the NBTI effect in LTPS TFTs has not been reported. Given this, the aim of our study is to use the CP technique to investigate the behavior of N_{bulk} during NBTI stress. Further, the role of oxide trap-state generation in the NBTI degradation mechanism is also identified.

II. EXPERIMENT

P-channel LTPS TFTs (W/L = 10 μm/10 μm) were fabricated on glass substrates. A 40-nm-thick amorphous Si layer was deposited by plasma enhanced chemical vapor deposition

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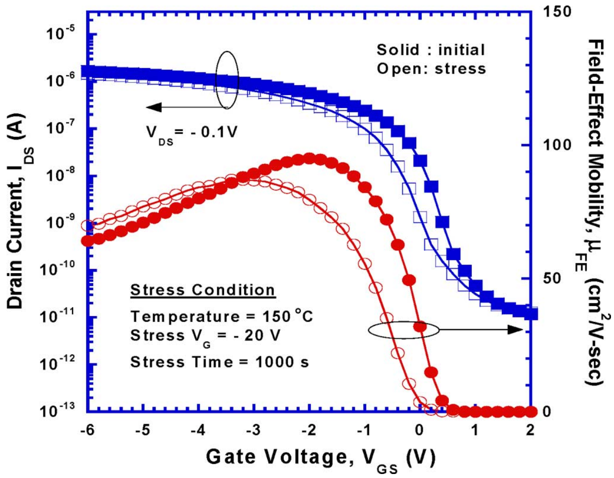

Fig. 2. Transfer characteristics of the LTPS TFT before and after 1000 s NBTI stress at 150 °C with the stress voltage of −20 V.

(PECVD) on a buffer layer and crystallized into poly-Si film by excimer laser annealing. Ion implantation was performed on the extra body terminal to form the heavily doped n^+ region. A 100-nm-thick SiO_2 layer was deposited as the gate dielectric followed by Mo deposition as the gate. After source/drain formation, hydrogenation was performed with NH_3 treatment. Then, the interlayer dielectric was deposited and densified, and the dopants were activated during this step. Finally, interconnection metal was deposited and patterned. The schematic cross sectional and top views of the device are shown in Fig. 1(b) and 1(c), respectively.

The NBTI stress was performed at the temperature ranging from 75 °C to 150 °C, and a gate voltage in the range of −13 to −20 V was applied with the source, drain, and body grounded. During the CP measurement, a pulse train with frequency of 100 kHz and fixed pulse amplitude of 1.5 V were applied to the gate while I_{CP} was measured between the source/drain and substrate contact, and the base voltage was varied to tune the surface condition from inversion to accumulation.

III. RESULTS AND DISCUSSION

Fig. 2 shows the transfer characteristics of the LTPS TFT before and after the NBTI stress. The device shows degradation in the subthreshold swing and field-effect mobility, indicating that interface trap states were generated [11]. Further, the threshold voltage (V_{th}) shifts to the negative direction after the stress. Degradation can be attributed to the generation of bulk trap states and oxide trap states. Detailed analysis of these trap-state generations will be discussed later.

The inset of Fig. 3 shows the I_{CP} of the device before and after 1000 s NBTI stress. The increase in I_{CP} indicates that bulk trap states are generated during NBTI stress. Further, the I_{CP} curve shifts to the negative direction, implying that a net positive charge is clearly generated in the oxide or/and at the interface. Fig. 3 shows the time dependence of the N_{bulk} generation (ΔN_{bulk}), which is calculated from I_{CP}. ΔN_{bulk} follows a power law dependence on the stress time with an exponent factor of 0.37–0.42, implying that diffusion-controlled electrochemical reactions may take part in the process [12], [13].

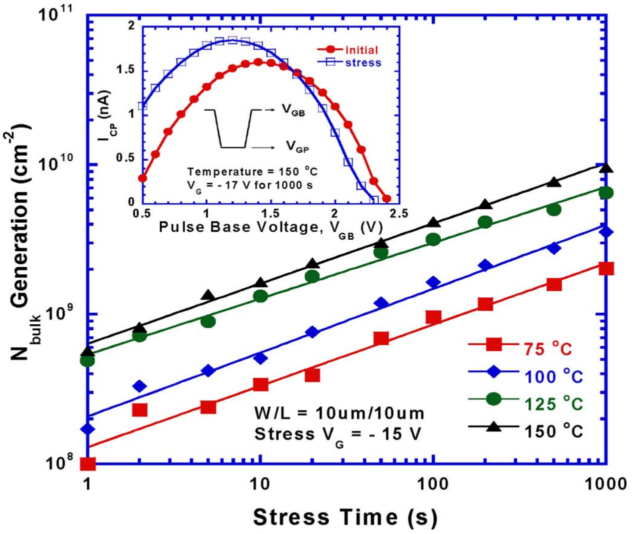

Fig. 3. Time dependence of the bulk trap-state density generation under various stress conditions. The inset shows the I_{CP} before and after 1000 s NBTI stress.

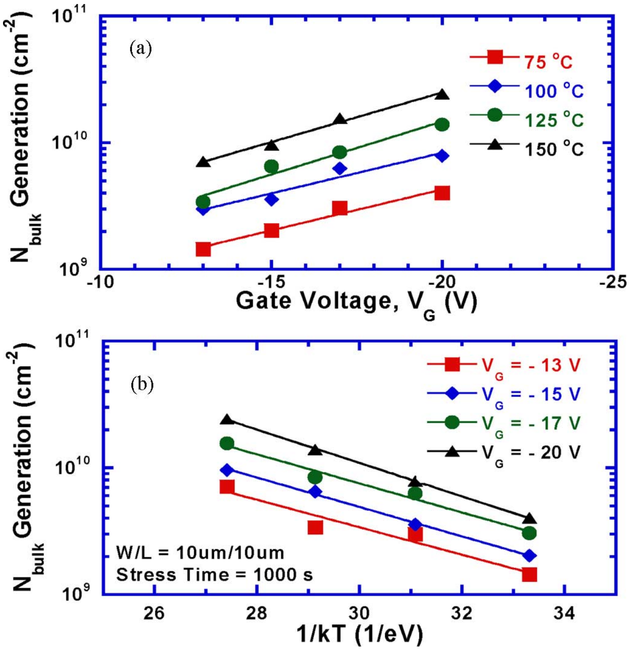

Fig. 4. Dependences of bulk trap-state density generation on the (a) stress voltage and (b) stress temperature of the LTPS TFTs under various stress conditions.

Further, ΔN_{bulk} also exhibits an exponential dependence on the stress voltage (V_G) and the reciprocal of temperature ($1/T$). The experimental results show that the N_{bulk} variation can be expressed as

$$\Delta N_{\text{bulk}} \propto t^n \, e^{(-E_a/kT)} \, e^{C|V_G|}. \tag{1}$$

The parameter C extracted from Fig. 4(a) is between 0.14 and 0.19, which is dependent on the process [14]. The activation energy (E_a) extracted from Fig. 4(b) is between 0.25 and 0.30 eV. ΔN_{bulk} increases with the stress voltage or temperature, implying that N_{bulk} generation can be electrically and thermally activated. On the other hand, the charge-trapping model is unable

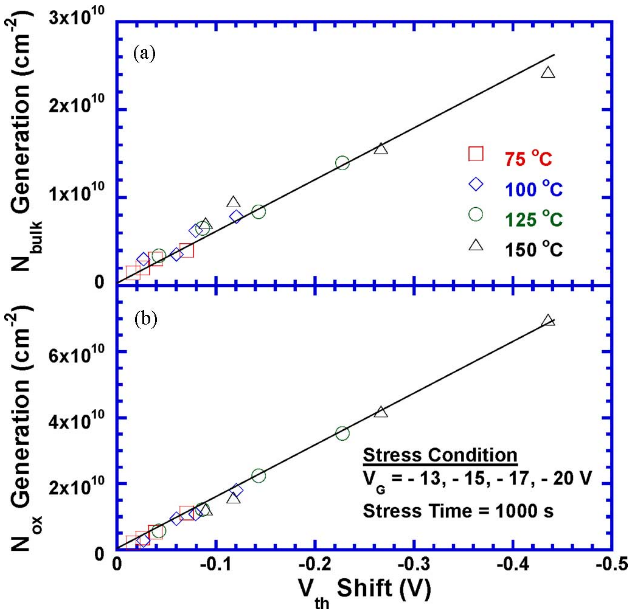

Fig. 5. Correlation between the increases of the (a) bulk trap-state density, (b) oxide trap-state density, and the threshold voltage shift.

to explain the exponential dependence of the V_{th} shift *(*ΔV_{th}*)* on V_G and *1/T* [15], [16]. Furthermore, the electric field across the gate dielectric (below 2 MV/cm) was not high enough to cause hole injection. Therefore, we thus provide further confirmation that the NBTI degradation in LTPS TFTs is attributable to diffusion-controlled electrochemical reactions instead of the charge-trapping model.

Fig. 5(a) presents the correlation between ΔN_{bulk} and ΔV_{th}, in which both these two physical quantities show a linear correlation. Because the degradation can be explained by the diffusion-controlled electrochemical reactions [12], [13], we can assume the ΔV_{th} is caused by the generation of N_{bulk} and oxide trap-state density (N_{ox}). Therefore, the threshold voltage shift (ΔV_{th}) may simply expressed as

$$\Delta V_{\mathrm{th}} = -\frac{q(\Delta N_{\mathrm{bulk}} + \Delta N_{\mathrm{ox}})}{C_{\mathrm{ox}}}. \tag{2}$$

According to (2), ΔN_{ox} can be calculated from the measured ΔV_{th} and ΔN_{bulk}. Fig. 5(b) shows the correlation between ΔN_{ox} and ΔV_{th}. We can conclude that ΔN_{bulk} alone cannot explain the measured ΔV_{th} and that ΔN_{ox} must be taken into account.

By expanding the model proposed for bulk-Si MOSFETs [17], we introduce a model to explain the NBTI degradation mechanism for LTPS TFTs. The Si dangling bonds in the bulk channel region are assumed to be initially passivated by hydrogen atoms. During NBTI stress, the hydrogen atoms react with the holes and dissociate from the Si atoms, resulting in the generation of bulk trap states. The released hydrogen species diffuse or drift into the gate oxide and react with it, forming OH groups bounded to oxide Si atoms and leaving positive oxide trap states in the gate oxide. Finally, the hydrogen species diffuse into the gate oxide, becoming the reaction-limiting factor.

IV. CONCLUSION

For the first time, the CP technique is utilized to analyze the NBTI degradation mechanism in LTPS TFTs. The properties of N_{bulk} can be directly characterized from I_{CP}. In addition, the increase of N_{ox} is also extracted. Our results show that both ΔN_{bulk} and ΔN_{ox} are closely related to ΔV_{th}. This further confirms that ΔN_{bulk} alone cannot explain the measured ΔV_{th} and that ΔN_{ox} must be taken into account. On the other hand, experimental results show that NBTI degradation can be electrically and thermally activated. Therefore, the operating voltage and power consumption have to be carefully designed, and new processes must be developed to suppress NBTI degradation and realize SOP.

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