Impacts of Fluorine Ion Implantation With Low-Temperature Solid-Phase Crystallized Activation on High-κ LTPS-TFT

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***Abstract*—In this letter, fluorine ion implantation with low-temperature solid-phase crystallized activation scheme is used to obtain a high-performance HfO_2 low-temperature poly-Si thin-film transistor (LTPS-TFT) for the first time. The secondary ion mass spectrometer (SIMS) analysis shows a different fluorine profile compared to that annealed at high temperature. About one order current reduction of $I_{\min}$ is achieved because 25% grain-boundary traps are passivated by fluorine implantation. In addition, the threshold voltage instability of hot carrier stress is also improved with the introduction of fluorine. The LTPS-TFT with HfO_2 gate dielectric and fluorine preimplantation can simultaneously achieve low $V_{\mathrm{TH}} \sim 1.32$ V, excellent subthreshold swing $\sim$0.141 V/dec, and high $I_{\mathrm{ON}}/I_{\min}$ current ratio $\sim 1.98 \times 10^7$.**

***Index Terms*—Fluorine implantation, high-κ, hot carrier stress, low-temperature poly-Si thin-film transistors (LTPS-TFTs).**

I. Introduction

HIGH-PERFORMANCE low-temperature poly-Si thin-film transistors (LTPS-TFTs) are recently developed for the employment of active-matrix liquid crystal displays on a glass substrate and for driving integrated circuits for the application of system-on-panel (SOP) [1]–[3]. However, there are many defects at the grain boundary of poly-Si channel film, resulting in the degradation of LTPS-TFTs' performance [4]. In order to make the channel more conductive, grain traps of the poly-Si channel film must be passivated. Therefore, a large operation voltage was needed for the conventional LTPS-TFTs without any defects passivation [5]–[9]. The grain defects of the poly-Si channel film would result in poor subthreshold swing (S. S.), high minimum drain–current ($I_{\min}$), and large threshold voltage (V_{TH}).

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The adopting of high-κ gate dielectric is one of the effective ways to improve the performance of LTPS-TFTs [10]–[12]. A larger gate capacitance with the same physical thickness by using high-κ gate dielectric instead of SiO_2 gate oxide can attract more carriers with a smaller voltage to turn on the LTPS-TFTs. In spite of the employment of high-κ gate dielectrics, the defects of the poly-Si channel film still exist that contribute to high drain leakage current [4]. Therefore, defects passivation is necessary to improve the drain leakage current and $I_{\mathrm{ON}}/I_{\min}$ current ratio. Hydrogen plasma treatment is the most popular approach used to passivate defects and reduce the leakage current [13]–[15]. However, the introduction of hydrogen would degrade the reliability due to the weak Si–H bonds [16], [17]. To solve this problem, fluorine implantation is a promising alternative to create strong Si–F bonds [5]–[9]. Subsequent high-temperature processes ($\geqq$700 °C) after fluorine implantation have been used for the deposition of tetraethylorthosilicate (TEOS) gate dielectric layer and passivation layer at 700 °C over 3 h [6], [7] and the growth of thermal oxide and dopant activation at 850 °C [8], [9], which causes fluorine ions to diffuse to the interfaces of gate-oxide/poly-Si and poly-Si/buried-oxide and pile up in the interfaces. However, fluorine implantation with a low-temperature solid-phase crystallized activation ($\leqq$600 °C) has not been reported yet. In this letter, we found that the distribution of fluorine ions is totally different at high temperatures, the electrical performance can be improved significantly.

II. Experimental Procedure

The fabrication of devices started by depositing a 50 nm undoped amorphous Si (α-Si) layer at 550 °C in a low-pressure chemical vapor deposition system on Si wafers capped with a 500-nm-thick thermal oxide layer. Then, the fluorine atoms were implanted at energy of 11 keV to a dosage of 5×10^{14} cm^{-2}. The α-Si layer was recrystallized by solid-phase crystallization (SPC) process in furnace at 600 °C for 24 h in a N_2 ambient. A 500-nm-thick plasma-enhanced chemical vapor deposition oxide was deposited at 300 °C for the device isolation. The oxide was then patterned and etched to define the active region of device. The source and drain regions in the active device region was implanted with phosphorus (15 keV at 5×10^{15} cm^{-2}) and activated at 600 °C for 24 h annealing in a N_2 ambient. Then, a 75 nm HfO_2 was deposited by electron-beam evaporation system. An O_2 treatment in furnace was applied to improve the gate oxide quality at 400 °C for 30 min. After the patterning of

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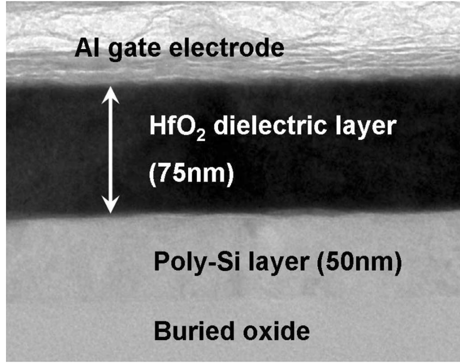

Fig. 1. Cross-sectional transmission electron microscopy (TEM) micrograph of the HfO_2 gate dielectric TFT structure.

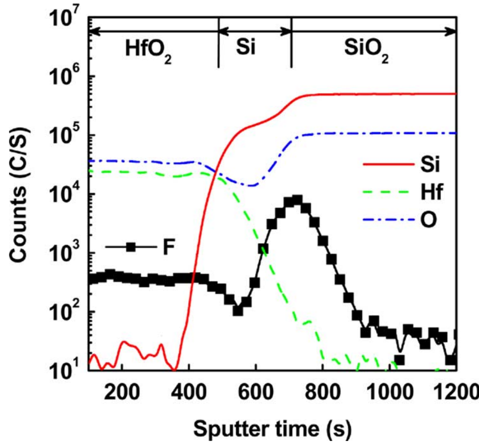

Fig. 2. SIMS analysis of the HfO_2 LTPS-TFT with fluorine preimplantation.

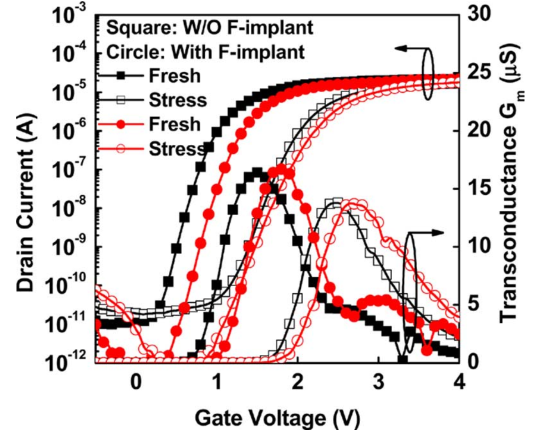

Fig. 3. Transfer characteristics (I_D–V_G and G_m) of the HfO_2 LTPS-TFT at $V_D = 0.1$ V without and with fluorine preimplantation before and after hot carrier stress for 1000 s.

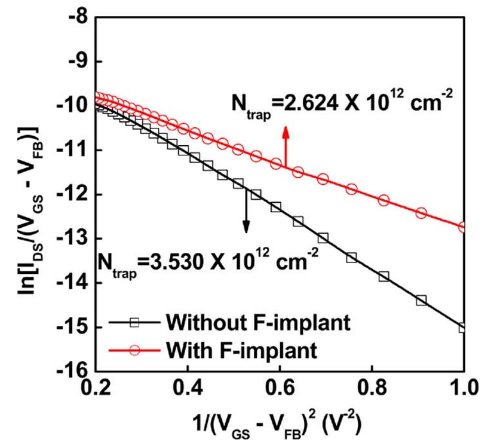

Fig. 4. Plots of ln $[I_{\rm DS}/(V_{\rm GS}–V_{\rm FB})]$ versus $1/(V_{\rm GS}–V_{\rm FB})^2$ curves at $V_{\rm DS} = 1$ V and high $V_{\rm GS}$.

contact holes, aluminum was deposited by thermal evaporation system and patterned as the probe pads to complete the TFT devices. There are no high-temperature processes (≧600 °C) during device fabrication.

Fig. 1 shows the cross-sectional transmission electron microscopy (TEM) micrograph of HfO_2 gate dielectric TFT structure. The measured device has gate length and width of 10 and 100 μm, respectively. The $V_{\rm TH}$ is defined as the gate voltage at which the drain–current reaches 100 nA $\times\ W/L$ under $V_D = 0.1$ V. The field effect mobility $\mu_{\rm FE}$ is extracted from the maximum transconductance (G_m).

III. Results and Discussion

Fig. 2 shows the secondary ion mass spectrometer (SIMS) spectrum of HfO_2 LTPS-TFT with fluorine implantation. We can observe that fluorine ions after postimplanted low-temperature SPC activation are merely piling up at the poly-Si/buried-oxide interface, and are not observed in the HfO_2/poly-Si interface. This distribution of fluorine ions is different from the results of high-temperature annealing that fluorine ions would pile up at the interfaces of both gate-oxide/poly-Si and poly-Si/buried-oxide [6]–[9]. This implies that the SPC activation of α-Si with fluorine preimplantation would not affect the upper part of the channel film. The impacts of fluorine preimplantation with low-temperature SPC activation on the performance of HfO_2 LTPS-TFTs are shown in Fig. 3. High-performance characteristics of HfO_2 LTPS-TFT with low $V_{\rm TH} \sim 1$ V, excellent S. S. ~0.147 V/dec, high mobility ~74.5 cm^2/V · s, and high $I_{\rm ON}/I_{\rm min}$ current ratio ~2.19×10^6 are observed without any treatment. After fluorine implantation, we can observe that the $I_{\rm min}$ is reduced significantly from 9.78 to 1.09 pA at $V_D = 0.1$ V. The $I_{\rm min}$ can be attributed to the junction leakage current that is dominated by the grain-boundary trap-state densities ($N_{\rm trap}$) of poly-Si channel film [4]. The effective grain-boundary trap-state densities ($N_{\rm trap}$) with and without fluorine implantation are also estimated by Levinson and Proano method [18], [19]. Fig. 4 exhibits the plots of ln $[I_{\rm DS}/(V_{\rm GS}–V_{\rm FB})]$ versus $1/(V_{\rm GS}–V_{\rm FB})^2$ curves at $V_{\rm DS} = 1$ and high $V_{\rm GS}$, where the flat-band voltage ($V_{\rm FB}$) is defined as the gate voltage that yields the minimum drain–current from the transfer characteristic. From Fig. 4, it is apparent that the effective grain-boundary trap-state densities decrease from 3.530×10^{12} to 2.624×10^{12} cm^{-2} after fluorine passivation. This indicates that about 25.6% reduction in the effective grain-boundary trap-state densities is achieved due to the passivation of the grain-boundary trap-state densities in the lower part of the channel film. The important parameters of

TABLE I
IMPORTANT PARAMETERS OF THE HfO_2 LTPS-TFT WITHOUT AND WITH FLUORINE PREIMPLANTATION

	V_{TH} (V)	S.S. (V/dec.)	μ_{EF} (cm^2/V-s)	I_{min} (pA)	I_{on} (μA)	I_{on}/I_{min} (10^6)	N_{trap} (10^{12} cm^{-2})	ΔV_{TH} (V)
w/o F-implant	1.01	0.147	74.5	9.78	21.4	2.19	3.530	1.02
with F-implant	1.32	0.141	75.9	1.09	21.6	19.82	2.624	0.89

LTPS-TFTs are listed in the Table I. A slight increase of $V_{\rm TH}$ from 1.01 to 1.32 V is observed after fluorine implantation. This is because lots of fluorine ions are incorporated in the buried oxide to form the negative fixed oxide charges to affect the channel film [20]. This subgate effect would make the channel less conductive, thus increasing the $V_{\rm TH}$ [8]. However, the behaviors of significant $I_{\min}$ reduction and a slight $V_{\rm TH}$ increase of the fluorinated n-channel TFTs cannot be found in previous reports [6]–[9].

In addition to the performance enhancement of HfO_2 LTPS-TFT, the reliability of the devices under hot carrier stress with $V_D = 2(V_G – V_{\rm TH}) = 10$ V for 1000 s is also studied, as shown in Fig. 3. The behavior of about one order reduction of $I_{\min}$ in the fluorinated TFT is still maintained, and shows a better threshold voltage instability $\Delta V_{\rm TH}$ from 1.02 to 0.89 V. It also demonstrates that the treatment method of fluorine preimplantation with low-temperature SPC activation would improve the reliability of LTPS-TFTs, as shown in the previous reports [6]–[9]. Hydrogen treatment can also reduce the $I_{\min}$ effectively. However, the introduction of hydrogen would seriously degrade the reliability of LTPS-TFTs and easily release during mediate temperature process ($\geqq 500\,^\circ$C) [16], [17].

IV. CONCLUSION

High-performance LTPS-TFT with HfO_2 gate dielectric and fluorine preimplantation has been demonstrated. Low-temperature SPC activation of fluorine ions is reported for the first time, and it also provides an improved electrical characteristics and reliability. Thus, it would be useful for the application of SOP.

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