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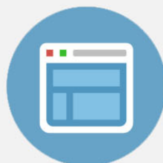

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# Probing a nonuniform two-dimensional electron gas with random telegraph signals

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We observe a sequence of two-level random telegraph signals (RTSs) in the drain/source current of a 1.7 nm gate oxide silicon metal-oxide-semiconductor field-effect transistor. The RTS magnitude is transformed into the *apparent* Debye length around a negatively charged oxide trap. We achieve excellent reproduction of the Debye data (40 down to 5 nm). This leads to the quantified area spanned by the dominant conductive percolation paths in the underlying two-dimensional electron gas (2DEG). We find that most of the 2DEG in inversion is recovered in a largest threshold voltage sample (~0.35 V), while for the lowest threshold (~0.15 V), a certain conductive filament is likely to occur. The gate direct tunneling current further corroborates the percolation picture. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2841725]

## I. INTRODUCTION

Silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely utilized as a test vehicle of random telegraph signals (RTSs).[1–14] In the presence of a certain oxide trap with the energetic level in the proximity of silicon Fermi level, the on and off of the local conduction in a two-dimensional electron gas (2DEG) due to the fluctuating occupancy of the trap give rise to RTS in the drain/source current. This well-known two-level RTS can be characterized by three key factors in terms of the mean capture time, the mean emission time, and the relative amplitude. So far, measurements of the former two switching time constants have exhibited potential applications, such as determination of the energetic level of the trap and its depth into the oxide[1,3,5,7–9,11,14,15] identification of the neutral or attractive-type trap,[7,8] and construction of a configuration coordinate diagram for the electron-lattice system.[2,9,14,15] In addition, analyses of capture/emission time constants obtained at very low temperatures have produced important findings, such as the trapping statistics change due to the interaction between the trap and the 2DEG Ref. 10 and the electron spin properties of the oxide trap.[12,13] The RTS time constant based electron spin resonance has also been experimentally demonstrated.[13] On the other hand, the remaining RTS counterpart, namely, the relative amplitude, can be well described by a screened Debye length model,[6] valid only for the uniform channel case. Owing to the manufacturing process variations, however, the nonuniformity or percolation nature may prevail in the 2DEG beneath the gate oxide and, thereby, affect the RTS magnitude.[3,4,6,16–18] Thus, if the RTS magnitude deviates from that of the screened Debye length model,[6] then the created errors should reflect the relevant information about the dominant conductive percolation paths in the underlying 2DEG. However, little work has been performed in this direction.

In this work, we elaborate on the extraction of the 2DEG percolation area from the MOSFET RTS amplitude. A linkage with the threshold voltage is established. Also presented are the gate direct tunneling current data that can corroborate the percolation picture built in this work.

## II. RTS MEASUREMENT

The device under study was $n$-channel MOSFET fabricated in a state-of-the-art manufacturing process. The following key process parameters were obtained through the capacitance-voltage fitting: $n^+$ polysilicon doping concentration of $1.3\times10^{20}$ cm$^{-3}$, gate oxide thickness of 1.7 nm, and channel doping concentration of $8\times10^{17}$ cm$^{-3}$. A semiconductor parameter analyzer HP4156 was utilized with the source and bulk tied to the ground and the drain connected to a bias of 10 mV. The measurement temperature was 297 K. The probability of finding RTS events across the whole wafer was extremely low. Only a few devices were eventually identified with two-level RTS, as displayed in Fig. 1 for a certain sample. As shown in Fig. 1, the same RTS events in the source current also simultaneously occurred in the drain current. No noticeable change in the gate current was detected, meaning that the trap responsible for the RTS is an atomic-sized trap relative to the 1.7 nm gate oxide used. This trap should be naturally created during the manufacturing process, rather than caused by the electrical stressing in the long-term RTS measurement. On the other hand, the well recognized trap assisted tunneling component was difficult to distinguish in the measured gate current (i.e., high level corresponding to the empty trap state) since the trap itself occupies a very small part of the gate oxide area.

The measured capture time $\tau_c$ associated with the high current level and the measured emission time $\tau_e$ associated with the low current level each was found to be exponentially distributed. The ratio of the mean capture time $\langle\tau_c\rangle$ and the mean emission time $\langle\tau_e\rangle$ is shown in Fig. 2 for several samples labeled as traps A, B, C, and D versus the gate overdrive voltage (that is, gate voltage minus threshold voltage). The zero gate overdrive voltage represents the classical onset of the inversion. From the aspect of electrostatics, the

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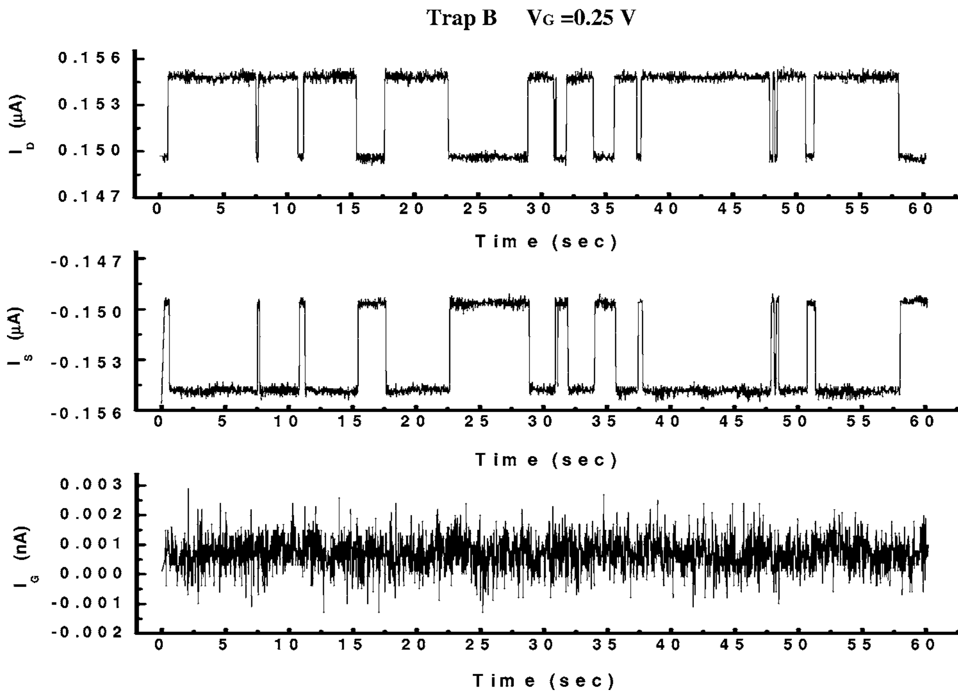


FIG. 1. Time records of the drain, source, and gate currents for the sample of trap B at $V_G$=0.25 V.

use of the gate overdrive term can greatly facilitate the analysis in the case of different samples with different threshold voltages. The measured relative magnitude $\Delta I_D/I_D$ versus gate overdrive voltage is depicted in Fig. 3. To accommodate the comparison, several device parameters are listed in Table I, such as the gate width to gate length ratio $W/L$ and the near-equilibrium carrier mobility $\mu_0$ and threshold voltage $V_{\mathrm{th}}$. Here, $\mu_0$ and $V_{\mathrm{th}}$ were extracted using the standard procedure in the linear regime or the peak transconductance extrapolation technique at a drain voltage of 0.01 V. Other parameters in the table will be interpreted later.

## III. PARAMETER EXTRACTION AND ITS VALIDITY

With the abovementioned process parameters as inputs, a self-consistent Schrödinger-Poisson equation solver was performed to produce the 2DEG carrier density $N_S$ as a function of the gate overdrive voltage. The simulated threshold voltage is 0.278 V. Consequently, the measured RTS relative magnitude in Fig. 3 can be transformed into the *apparent* Debye length designated as $L_t$, as shown in Fig. 4, versus $N_S$. Here, $L_t$ is defined as the square root of the product of the measured RTS relative magnitude times the gate area $WL$, according to the formalism

$$\frac{\Delta I_D}{I_D} = \frac{L_t^2}{WL}. \tag{1}$$

Taking into account the percolation nature, $L_t$ can further be decomposed into two distinct components,

$$\frac{1}{L_t} = \frac{1}{L_S/\gamma_1} + \frac{1}{L_C/\gamma_2}, \tag{2}$$

where $\gamma_1$ and $\gamma_2$ are the coefficients ($\leq 1$) accounting for the percolation areas in the subthreshold and inversion regimes of operation, respectively. The physical meaning of $\gamma_1$ and

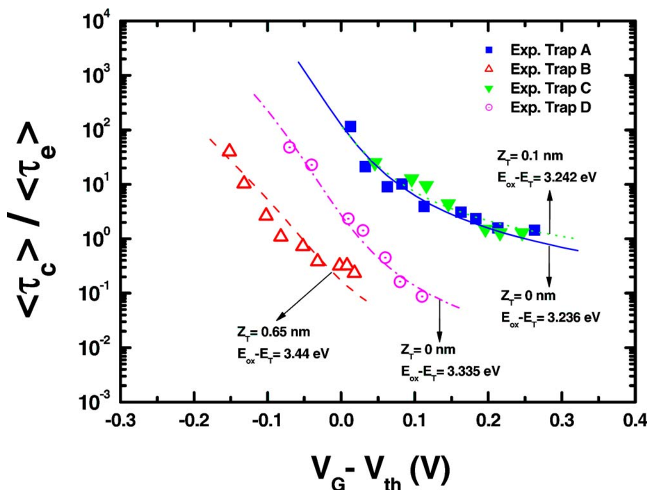


FIG. 2. (Color online) Measured mean capture time to mean emission time ratio vs gate overdrive voltage for four samples. The fitting lines from Eq. (3) are also shown along with the extracted energetic level of the trap and its depth into the oxide.

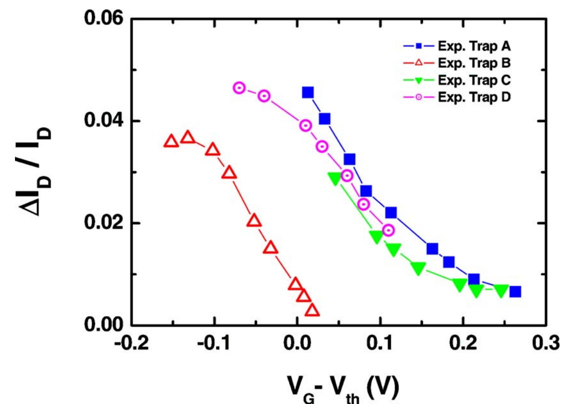


FIG. 3. (Color online) Measured RTS relative amplitude vs gate overdrive voltage corresponding to Fig. 2.

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TABLE I. List of the data obtained from the RTS investigation of four MOSFET samples. $z_T$ is the depth of the trap from the $SiO_2/Si$ interface, $E_{ox}-E_T$ is the trap energetic level below the oxide conduction-band edge, and $\gamma_1$ and $\gamma_2$ are the percolation coefficients in the subthreshold and inversion regimes, respectively. Also listed are the device parameters such as the gate width to gate length ratio $W/L$ and the near-equilibrium carrier mobility $\mu_0$ and threshold voltage $V_{th}$. The measurement temperature is 297 K.

| | | Trap A | Trap B | Trap C | Trap D |
|---|---|---|---|---|---|
| $W/L$ | (nm/nm) | 100/180 | 600/90 | 130/90 | 300/90 |
| $\mu_0$ | ($cm^2$/V s) | 204 | 185 | 150 | 148 |
| $V_{th}$ | (V) | 0.18 | 0.35 | 0.15 | 0.29 |
| $Z_T$ | (nm) | 0–0.1 | 0.65 | 0–0.1 | 0 |
| $E_{ox}-E_T$ | (eV) | 3.236–3.242 | 3.44 | 3.236–3.242 | 3.34 |
| $\gamma_1$ | | 0.42 | 0.36 | 0.63 | 0.45 |
| $\gamma_2$ | | 0.14 | 0.8–1 | 0.22 | 0.1 |

$\gamma_2$, as well as the derivation and validity of Eqs. (1) and (2), will be interpreted later. In Eq. (2), $L_S$ is a double of the critical distance from the trapped electron where the Coulomb potential energy is equal to the carrier average kinetic energy $kT$ in 2DEG (Ref. 6) and can be written as $L_S = q^2/2\pi\varepsilon_{eff}kT$. Here, $\varepsilon_{eff}$ is the effective permittivity and should be a function of both the silicon permittivity $\varepsilon_{Si}$ and the $SiO_2$ permittivity $\varepsilon_{ox}$. One of the expressions, $\varepsilon_{eff}=(\varepsilon_{Si}+\varepsilon_{ox})/2$, whose validity can be testified by comparing the existing sophisticated device simulation results,[18] was adopted here. As for $L_C$, it is the screening length by the 2DEG, and in the quantum limit, it can be written as $L_C = 2^{1.5}\,\varepsilon_{Si}kT/q^2N_S$.[19] With $\varepsilon_{eff}\rightarrow\varepsilon_{Si}$, $\gamma_1\rightarrow 1$, and $\gamma_2\rightarrow 1$, the case of uniform channel, Eqs. (1) and (2) both exactly reduce to those of the existing screened Debye length model.[6] As shown in Fig. 4 for the samples of traps B and D, an excellent reproduction of $L_t$ is achieved over the subthreshold and inversion regimes, leading to the values of $\gamma_1$ and $\gamma_2$. Although the observed RTS of traps A and C is limited to the inversion regime, the subthreshold $\gamma_1$, in addition to inversion $\gamma_2$, can be reasonably obtained through the best fitting technique.

To testify the validity of the above percolation extraction process, the underlying trap must be first identified. It is known that the mean capture time to mean emission time ratio can read as[7,8]

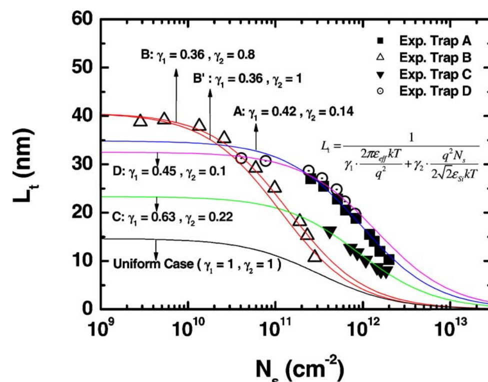


FIG. 4. (Color online) Comparison of experimental Debye length (symbols) vs 2DEG carrier density with those calculated (lines) from Eq. (2). Also shown is the calculated line for the uniform case.

$$\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle} = e^{(E_T-E_F+\Delta E)/k_BT}. \quad (3)$$

Here, the trap level $E_T$ relative to the channel quasi-Fermi level $E_F$ can be readily quantified by the same self-consistent Schrödinger-Poisson equation solving. The Coulomb energy $\Delta E$ required in the charging of the oxide trap can be written as[7,8]

$$\Delta E = Q_G q V_G + Q_{dep}(E_F - E_{vo}) + (Q_{inv} - 1)(E_F - E_0), \quad (4)$$

where $Q_G$, $Q_{inv}$, and $Q_{dep}$ are the normalized image (polarized) charges induced on the gate, the inversion layer, and the silicon depletion region, respectively, $E_0$ is the lowest subband level, and $E_{vo}$ is the valence band edge in the silicon substrate. These fractional charges can be calculated using a trap depth dependent capacitance model.[14] Best fitting was achieved in a wide range of gate overdrive voltage, as shown in Fig. 2, yielding the values of the trap depth $z_T$ and the energetic level $E_{OX}-E_T$ ($E_{OX}$ denotes the oxide conduction-band edge). It can be inferred that an interfacelike neutral trap exists in devices of traps A, C, and D, while a deep neutral trap in oxide prevails in trap B. Therefore, the aforementioned percolation extraction process is validated.

## IV. INTERPRETATIONS AND PERCOLATION PICTURE

Equations (1) and (2) can be derived from the two extreme cases: the subthreshold and the strong inversion. In the former limit, the area of the dominant percolation regime can be approximated as the gate area $WL$ times the square of $\gamma_1$. Uniform conductivity[6] is assumed across the percolation area as implicitly included in $\gamma_1$. Under such situations, one can draw $\Delta I_D/I_D \approx L_S{}^2/\gamma_1{}^2 WL$ accordingly.[6] Another limiting case can apply similarly but with $L_S$ replaced by $L_C$ and $\gamma_1$ by $\gamma_2$. The arrangement of the different percolation coefficients is reasonable since the different operating conditions can encounter different percolation paths, as revealed by the sophisticated device simulations.[16–18] As for the transition regime between the lower and upper limits, it can be readily treated by using one of the expressions such as Eq. (2) as originally cited elsewhere.[6] Therefore, the experimentally determined $L_t$ on the basis of Eq. (1) is able to provide the picture of the nonuniformities, depending on the extracted $\gamma_1$ and $\gamma_2$ through Eq. (2).

Some issues of relevance must be addressed prior to dealing with the extracted percolation quantities. Firstly, if the gate-to-diffusion overlap size is around 6 nm,[20] then the channel length deviates less from the gate length used. In other words, the error due to the direct use of the gate area in Eq. (1), rather than the active channel area, is insignificant. Secondly, the existing device simulations[4] point out that a significant change in the relative amplitude can be seen only for the trap depth critically exceeding around 10 nm, much larger than that (0.65 nm) of the deep trap in our work. Therefore, the trap depth effect on the RTS relative magnitude is negligible for the samples studied. Finally, the device performance parameters such as the carrier mobility in Table I are comparable between the samples, except the threshold voltage that varies in a wide range of 0.15–0.35 V.

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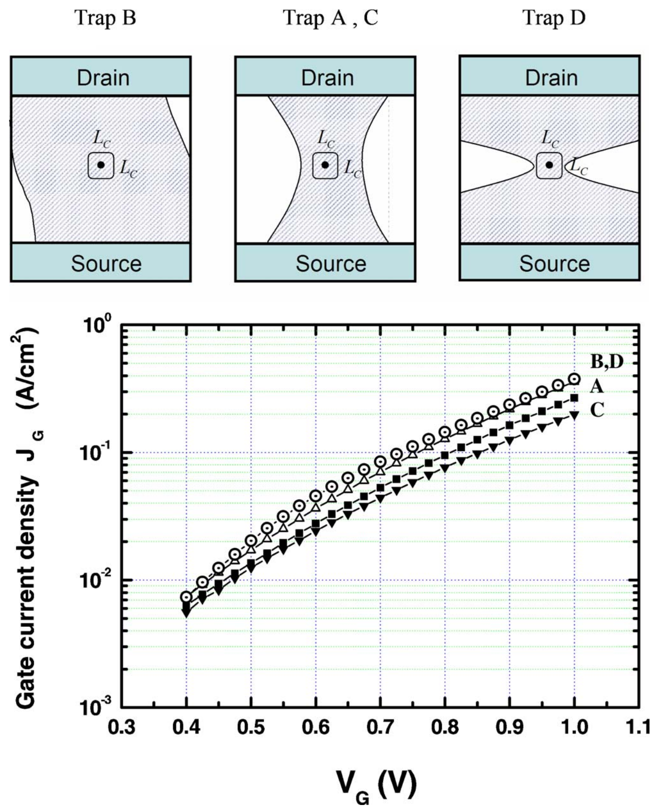


FIG. 5. (Color online) Schematic demonstration of three plausible 2DEG percolation paths for the samples under study. Also shown together is the corresponding measured gate current divided by the gate area *WL* as a function of gate voltage.

A linkage with the threshold voltage is straightforwardly established. For the largest threshold voltage sample, trap B, the extracted $\gamma_2$ ($\approx$0.8–1.0) is also the highest among the samples and is larger than the accompanying $\gamma_1$ ($\approx$0.36). Then, a view of the percolation paths becomes clear: (i) the anomalous threshold voltage means that in the subthreshold, a certain conductive percolation regime with the area of $\gamma_1{}^2 WL$ dominates, and (ii) the conduction of the remaining channel is almost recovered as entering into the inversion regime, which is reflected by the high $\gamma_2$. The same picture in the presence of a large threshold voltage due to random doping can be found in the existing device simulations.[18] In contrast, for both traps A and C, the lowest threshold voltage samples, the corresponding $\gamma_2$ are 0.14 and 0.22, respectively, indicating that a conductive filament is likely to occur in inversion. Indeed, such a narrow percolation path can be physically connected with the lowest threshold voltages (0.18 and 0.15 V, respectively). As for the remaining sample, trap D, the above arguments on the basis of the extracted $\gamma_1$ and $\gamma_2$ remain valid, although the threshold voltage (0.29 V) is normal with respect to the simulated value (0.278 V). We can find a plausible interpretation: A critical percolation bottleneck is located around the trap and its spanned width is comparable with the Debye length. Only with such a hypothesis can the threshold voltage be maintained as close to the nominal value as possible. The picture of the percolation paths as drawn above is schematically shown in Fig. 5. In the figure, the shaded area is conductive, while for the area of $L_C{}^2$, the conduction is blocked upon electron capture. Strikingly, we noticed that the measured gate direct tunneling current divided by the gate area *WL*, as together plotted in Fig. 5, can readily serve as the confirmative evidence of the percolation picture. The gate current density at low gate voltages (close to the RTS measurement range) is comparable between traps B and D, as expected due to comparable percolation areas. This is also the case for the narrow percolation samples of traps A and C. Again, the gate current density of traps A and C each is lower than traps B or D, consistent with the arguments that the narrow percolation paths favor the samples of traps A and C.

## V. CONCLUSION

We have demonstrated how to draw a 2DEG percolation picture beneath the gate oxide by means of the RTS magnitude. A linkage with the threshold voltage of the device has been produced. The gate direct tunneling current measured per unit area has further corroborated the validity of the nonuniformity picture built in this study.

## ACKNOWLEDGMENTS

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