Characteristics of PBTI and Hot Carrier Stress for LTPS-TFT With High-κ Gate Dielectric

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***Abstract*—In this letter, the characteristics of positive bias temperature instability (PBTI) and hot carrier stress (HCS) for the low-temperature poly-Si thin-film transistors (LTPS-TFTs) with HfO_2 gate dielectric are well investigated for the first time. Under room temperature stress condition, the PBTI shows a more serious degradation than does HCS, indicating that the gate bias stress would dominate the hot carrier degradation behavior for HfO_2 LTPS-TFT. In addition, an abnormal behavior of the $I_{\min}$ degradation with different drain bias stress under high-temperature stress condition is also observed and identified in this letter. The degradation of device's performance under high-temperature stress condition can be attributed to the damages of both the HfO_2 gate dielectric and the poly-Si grain boundaries.**

***Index Terms*—High-κ, hot carrier stress (HCS), low-temperature poly-Si thin-film transistors (LTPS-TFTs), positive bias temperature instability (PBTI).**

I. Introduction

LOW-TEMPERATURE poly-Si thin-film transistors (LTPS-TFTs) have been used for active-matrix liquid crystal displays on glass substrate as pixel and driving integrated circuits instead of amorphous silicon [1]–[6]. Therefore, high-performance TFTs with high driving current, low threshold voltage ($V_{\rm TH}$), and subthreshold swing (S.S.) are required urgently for high-speed display driving circuits. In order to achieve high-performance LTPS-TFT, employing high-κ gate dielectric is one of the effective ways to improve the performance of LTPS-TFT [7]–[9]. In addition, low-quality deposited low-temperature SiO_2 [like plasma-enhanced chemical vapor deposition (PECVD), SiO_2] is generally employed as the gate dielectric of the conventional LTPS-TFT. Comparing with low-quality deposited low-temperature SiO_2, low-temperature deposited high-κ gate dielectric could have better quality and be more suitable for the replacement of the conventional low-temperature SiO_2. However, the reliability issue of LTPS-TFT with high-κ gate dielectric is still not deeply studied. In this letter, positive bias temperature instability (PBTI) and hot carrier stress (HCS) of HfO_2 LTPS-TFT are well investigated for the first time.

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II. Experimental Procedure

The fabrication of devices started by depositing a 50-nm-undoped amorphous Si (α-Si) layer at 550 °C in a low-pressure chemical vapor deposition system on Si wafers capped with a 500 nm thermal oxide layer. Then, the 50 nm α-Si layer was recrystallized by solid-phase crystallization process at 600 °C for 24 h in a N_2 ambient. Then, a 500 nm PECVD oxide was deposited at 300 °C for device isolation. The device active region was formed by patterning and etching the isolation oxide. The source and drain regions in the active device region were implanted with phosphorus (15 keV at 5×10^{15} cm^{-2}) and activated at 600 °C for 24 h annealing in a N_2 ambient. A 75 nm HfO_2 with effective oxide thickness 14.7 nm was deposited by electron-beam evaporation system. After the patterning of source/drain contact holes, aluminum was deposited by thermal evaporation system as the gate electrode and source/drain contact pad. Finally, the TFT devices were completed by the contact pad definition.

Devices with gate length (L) and width (W) of 10 and 100 μm were measured. The $V_{\rm TH}$ is defined as the gate voltage at which the drain current reaches 100 nA $\times$ W/L and $V_{DS} = 0.1$ V. The transfer characteristics I_D–V_G of HfO_2 LTPS-TFT are measured at $V_D = 0.1$ V and $V_G = -0.5$ to 4 V. The nominal operating voltage of this LTPS-TFT with HfO_2 gate dielectric is set to be 4 V due to its excellent S.S. and low threshold voltage ($\sim$0.9 V). The PBTI stress was set at $V_G - V_{\rm TH} = 5$ V and $V_D = V_S = 0$ V. Two HCS modes are also investigated, namely HCS-A: $V_G - V_{\rm TH} = V_D = 5$ V, $V_S = 0$ V, and HCS-B: $V_G - V_{\rm TH} = 5$ V, $V_D = 10$ V, $V_S = 0$ V. All measurements were performed at temperature $T = 25$ °C and 125 °C, respectively.

III. Results and Discussion

Fig. 1 shows the transfer characteristics of HfO_2 LTPS-TFT before and after 1000 s of PBTI and HCS-B stresses at 25 °C, respectively. We can observe that the shift of $V_{\rm TH}$, and degradation of S.S. and G_m of device under the PBTI are all more serious than those of devices under HCS-B. The extracted parameters of these HfO_2 LTPS-TFTs are listed in Table I. It reveals that the gate bias stress would be the dominant factor of degradation for the HfO_2 LTPS-TFT under HCS. The difference between HCS and PBTI is the vertical electric field near the drain side. This

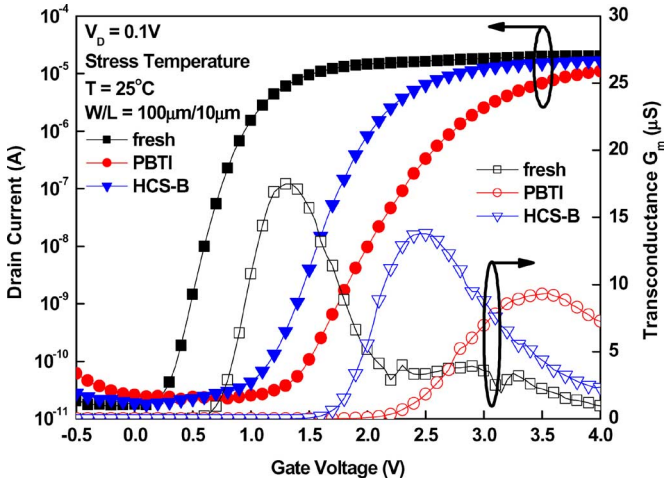

Fig. 1. Transfer characteristics (I_D–V_G and G_m) of the HfO_2 LTPS-TFT before and after 1000 s of PBTI and HCS-B stresses at 25 °C.

TABLE I
IMPORTANT PARAMETERS OF THE HfO_2 LTPS-TFT BEFORE AND AFTER 1000 s OF PBTI AND HCS-B STRESSES AT 25 °C

25°C Stress	V_{TH} (V) initial	V_{TH} (V) final	ΔV_{TH} (V)	G_m (μS) initial	G_m (μS) final	$\Delta G_m/G_{m(initial)}$ (%)	S.S. (V/dec.) initial	S.S. (V/dec.) final	ΔS.S. (V/dec.)
PBTI	0.9	2.7	1.8	17.5	9.35	46.6	0.1232	0.2626	0.1394
HCS-B		2.03	1.13		13.8	21.1		0.1726	0.0494

indicates that the stress of vertical electric field plays a more important role than does the stress of lateral electrical field for HfO_2 LTPS-TFT. Fig. 2 shows the gate leakage current of HfO_2 LTPS-TFT before and after 1000 s of PBTI and HCS-B stresses at 25 °C and 125 °C, respectively. A larger gate leakage current reduction of the PBTI device indicates that more electrons were trapped in HfO_2 under PBTI stress than under HCS-B stress. It shows that applying a drain voltage would decrease the behavior of electrons trapping in HfO_2, indicating that the vertical electrical field could introduce more trapped electrons in HfO_2 than the impact ionization of HCS does. Similar behavior of carrier trapping in HfO_2 gate dielectric during HCS is also observed for complementary metal–oxide–semiconductor Si nanoelectronics [10].

In addition to the degradation of $V_{\rm TH}$, G_m, and S.S., the $I_{\rm min}$ (from Fig. 1) is almost invariant after 1000 s of PBTI and HCS-B stresses, indicating that the poly-Si grain boundaries of channel film are not significantly damaged [11]. This shows that the main degradation of HfO_2 LTPS-TFT at 25 °C under PBTI and HCS-B stresses is due to the damage and electron trapping of HfO_2 gate dielectric.

Fig. 3 shows the transfer characteristics of HfO_2 LTPS-TFT before and after 1000 s stress at 125 °C under PBTI, HCS-A, and HCS-B stresses, respectively. The trend of $V_{\rm TH}$ shift, G_m degradation, and S.S. degradation is the same as measured at 25 °C. However, the behavior of $I_{\rm min}$ at 125 °C is different from the $I_{\rm min}$ at 25 °C. The PBTI device shows the most serious $I_{\rm min}$ degradation (from 2×10^{-9} to 4×10^{-8} A), and the HCS-A device shows a little improvement (from 4×10^{-8} to 1×10^{-8} A) of $I_{\rm min}$ as compared to the PBTI device. The HCS-B device

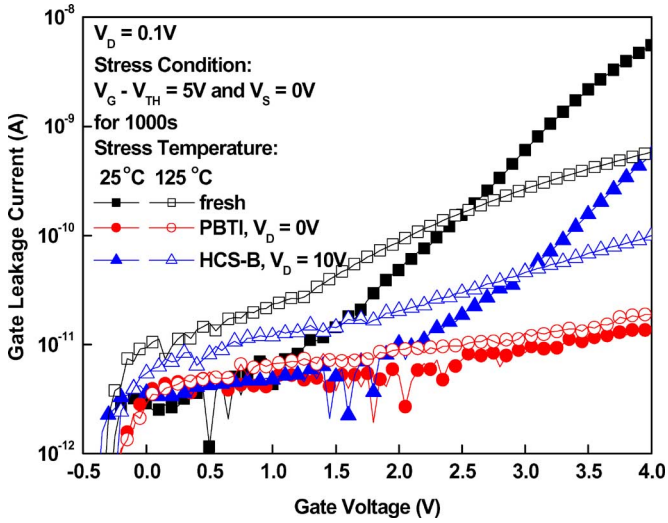

Fig. 2. Gate leakage current of the HfO_2 LTPS-TFT before and after 1000 s of PBTI and HCS-B stresses at 25 °C and 125 °C.

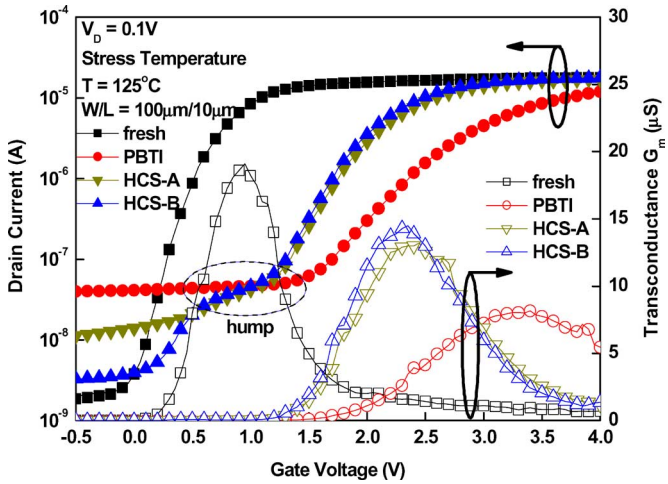

Fig. 3. Transfer characteristics of the HfO_2 LTPS-TFT before and after 1000 s of PBTI, HCS-A, and HCS-B stresses at 125 °C.

shows the smallest degradation of $I_{\rm min}$ among these samples (from 2×10^{-9} to 3.3×10^{-9} A). The $I_{\rm min}$ can be attributed to two sources: one is coming from the gate leakage current and the other is coming from the junction leakage current of drain side [11]. In this case, the gate leakage (from Fig. 2) has been shown to be too low to contribute the $I_{\rm min}$ of devices. Therefore, we can conclude that the $I_{\rm min}$ degradation is coming from the junction leakage current of drain side. However, an increased junction leakage current would be attributed to the degradation of poly-Si and HfO_2/poly-Si interface. We can observe from Fig. 1 that the degradation of HfO_2/poly-Si interface would contribute to a negligible increase of junction leakage current. Therefore, we could conclude that the increased junction leakage would be attributed to the damage of poly-Si grain boundaries. In PBTI device, the highest $I_{\rm min}$ indicates the most serious grain boundaries damage, resulting in significant increase of $I_{\rm min}$. In HCS-A case, drain bias would make the vertical electric field near the drain side lower and improve the $I_{\rm min}$ slightly. When a larger drain bias was applied as in the HCS-B

case, the vertical electric field would be decreased further. During positive gate bias stress, electrons would be accelerated by positive gate voltage and move toward the HfO_2/poly-Si interface. The accelerated electrons would collide with the weak bond of the grain boundaries to damage the poly-Si channel film and the HfO_2/poly-Si interface to generate the trap states to increase the drain leakage current $I_{\min}$, S.S., and reduce the transconductance G_m. Compared with stresses at 25 °C, stresses at 125 °C would result in more serious degradation and a hump behavior of transfer characteristics of HfO_2 LTPS-TFT due to higher carrier energy and lattice collision probability. Applying a drain bias would decrease the vertical field near the drain side and result in less junction damage and fewer electron trapping. The large drain bias would make the device have less $I_{\min}$ degradation and also a varying threshold voltage along the channel due to different degrees of grain boundaries damages and electron trapping, respectively. The local threshold voltage and grain boundaries damage near the drain side would be smaller than the one near the source side. Therefore, a hump in transfer characteristic of the device is observed in HCS-A case, as shown in Fig. 3, and the hump becomes significant in the HCS-B case. Based on the above mentioned results, stresses at 125 °C show that the degradation of HfO_2 LTPS-TFT is attributed to the damages of both HfO_2 and poly-Si grain boundaries.

IV. Conclusion

The PBTI and HCS of HfO_2 LTPS-TFT have been well investigated for the first time. We conclude that the vertical electric field stress dominated the hot carrier degradation behaviors for HfO_2 LTPS-TFT devices. In addition, a hump behavior of the transfer characteristic of HfO_2 LTPS-TFT under high-temperature stress condition was also observed and identified in this letter. The results show that applying a drain bias under stress would obviously impact the reliability of LTPS-TFT with high-κ gate dielectric.

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