# Compact CPW-MS-CPW Two-Stage pHEMT Amplifier Compatible With Flip Chip Technique in V-Band Frequencies

Jen-Yi Su, *Student Member, IEEE*, Chinchun Meng, *Member, IEEE*, Yueh-Ting Lee, and Guo-Wei Huang

***Abstract*—The V-band coplanar waveguide (CPW)–microstrip line (MS)–CPW two-stage amplifier with the flip-chip bonding technique is demonstrated using 0.15 $\mu$m AlGaAs/InGaAs pseudomorphic high electron mobility transistor technology. The CPW is used at input and output ports for flip-chip assemblies and the MS transmission line is employed in the interstage to reduce chip size. This two-stage amplifier employs transistors as the CPW–MS transition and the MS–CPW transition in the first stage and the second stage, respectively. The CPW–MS–CPW two-stage amplifier has a gain of 14.8 dB, input return loss of 10 dB and output return loss of 22 dB at 53.5 GHz. After the flip-chip bonding, the measured performances have almost the same value.**

***Index Terms*—Coplanar waveguide (CPW), flip-chip bonding, microstrip line (MS), pseudomorphic high electron mobility transistor (pHEMT).**

## I. INTRODUCTION

RECENTLY, the flip-chip bonding technique is necessary for packages of millimeter-wave monolithic microwave integrated circuits (MMICs) [1]–[5]. The flip-chip bonding technique has advantages over traditional wire bonding technique because of the shorter interconnect path, better mechanical stability, higher reliability and less parasitic effects [1]–[3]. Coplanar waveguide (CPW) topology [1], [2], [6] is widely employed in the millimeter-wave flip-chip MMICs to provide a smooth electric transition interface between the chip and the substrate carrier while the microstrip line (MS) topology after flip-chip assemblies shows a strong gain degradation for the frequencies above 50 GHz [5] even though the layout of an MS-type topology can save much real estate in the IC technology. The CPW MMIC has less complicated processing steps by eliminating via hole etching, wafer thinning, and backside processing in the MS-type process [1], [5]. Although the CPW circuit has the advantage of simple process, the lower effective dielectric constant and the difficulties in meandering the layout make the CPW MMIC size formidably large. CPW two-stage amplifiers were demonstrated at W-band frequencies, but consumed the large size of 1.9 mm $\times$ 1.25 mm and 2.4 mm $\times$ 1.1 mm, respectively [1], [6]. The compact size of the MS topology results from the higher effective dielectric constant and flexibilities on routing. The cost of the MMIC largely depends on the MMIC size rather than on the processing steps. For a two-stage power amplifier, the highest impedance transformation ratio occurs in the interstage because the input of the power stage has the lowest impedance while the output of the driver stage has the highest impedance. Transistors can function as a transition between MS and CPW circuits. Thus, it is imperative that for a two-stage amplifier the interstage matching circuit should be implemented in the MS topology while the CPW topology should be employed in the input and output ports to be a good compromise between flip-chip bonding compatibility and chip size.

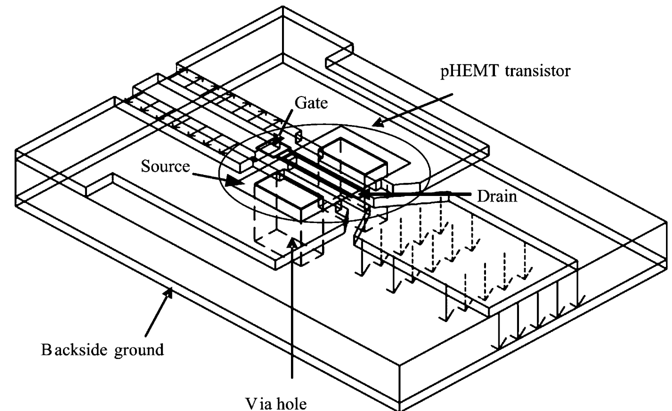


Fig. 1. CPW–MS transition by the pHEMT transistor with via holes at the source terminals.

The purpose of this work is to employ transistors as the area-saving CPW–MS transition. Many CPW–MS passive transitions were investigated [7]–[10]. In order to reduce the mismatch between the CPW and MS lines, a passive transition normally requires a large area and becomes impractical in the MMIC design. Fig. 1 shows the concept of the CPW–MS (MS–CPW) transition by the transistor. The gate (drain) port of the pseudomorphic high electron mobility transistor (pHEMT) is fed by the CPW line and source ports are symmetrically connected to the front side ground of the CPW line. The same via holes are also employed to connect the backside ground of the MS line at the drain (gate) port.

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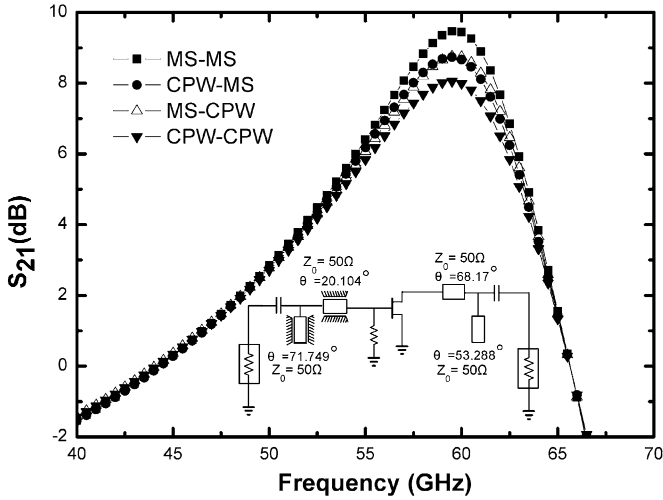



Fig. 2. Gain curves of the MS–MS, CPW–MS, MS–CPW, and CPW–CPW one-stage amplifiers with the same impedance matching.

MS–MS, MS–CPW, CPW–MS, and CPW–CPW one-stage pHEMT amplifiers designed at 60 GHz are employed to study the effect of using the device as a transition. Fig. 2 shows the simulation results for these four designs. All of the four designs have the same impedance matching as shown in Fig. 2. The input/output return loss is better than 10 dB for frequencies from 58.5 to 61.5 GHz for these four designs. Thus, the effect of loss is more pronounced at the resonant matching frequencies as shown in Fig. 2. It is well known that a CPW transmission line suffers more metal loss because the electric field is more concentrated at the metal edge in a CPW transmission line. Thus, the MS–MS one-stage amplifier has the highest peak gain of 9.4 dB while the CPW–CPW one-stage amplifier has the lowest peak gain of 8.0 dB. The metal loss causes 1.4 dB peak gain degradation for the CPW–CPW configuration and 0.7 dB for both CPW–MS/MS–CPW configurations when the MS–MS one-stage amplifier is compared. The loss occurring mostly at the resonant matching frequency band also affects the bandwidth. The 3 dB gain bandwidth is 7.7, 8.4, and 9.2 GHz for MS–MS, MS–CPW/CPW–MS and CPW–CPW configurations, respectively. Consequently, the CPW–MS–CPW two-stage amplifier is a good topology for V-band flip-chip amplifiers in terms of gain, bandwidth, and chip size. In this work, a CPW–MS–CPW two-stage amplifier is demonstrated at V-band frequencies and the resulting amplifier shows no electric performance degradation after flip-chip mounting.

## II. Circuit Design

The schematic of the CPW–MS–CPW two-stage amplifier is shown in Fig. 3 and the die photo is shown in Fig. 4. The size of the chip is $1.75 \times 0.85$ mm $^2$. This size is much smaller than the chip sizes of published [1], [6]. $S$ parameters for both the passive elements and transistors are needed in the amplifier design. The $S$ parameters of the passive elements are obtained through the EM simulator for better accuracy while the measured $S$ parameters of the pHEMT transistors are used. The CPW–MS–CPW two-stage amplifier is designed for the maximum gain because the devices are unconditionally stable at 50 GHz when the voltages of $V_{\rm DS}$ and $V_{\rm GS}$ are 2.0 V and 0 V, respectively. The width of two pHEMT transistors in the amplifier is $2 \times 50$ $\mu$m. In Fig. 3, several the $R$–$C$ series elements and $C$ elements at drain and gate ports are designed to avoid the low-frequency oscillation and to enhance the out-band stability, respectively [6]. As shown in Fig. 4, the quarter-wavelength transmission lines with a characteristic impedance of 90 Ω are applied to the biasing networks at gate and drain terminals of the transistors. This transmission line design aims to isolate the RF signal through dc paths. The matching networks at both input and output of the two-stage amplifier are designed and realized using CPW-type transmission lines for flip-chip assembly. Additionally, the microstrip transmission line, which has a higher effective dielectric constant than CPW line has, is applied to realize the matching network between two transistors for miniaturizing the size of the amplifier.

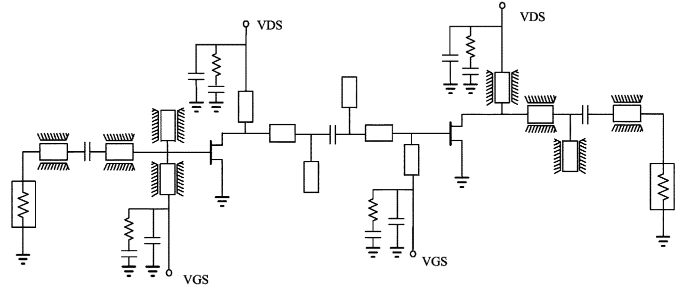



Fig. 3. V-band CPW–MS–CPW two-stage pHEMT amplifier.

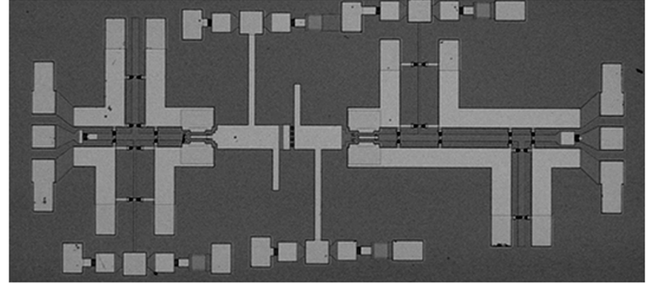


Fig. 4. Die photo of the CPW–MS–CPW two-stage pHEMT amplifier.

## III. Flip-Chip Measurement Results

The $S$-parameter was measured from 2 to 110 GHz by HP Network Analyzer 8510XF. Fig. 5 shows a flip-chip micrograph of the V-band CPW-MS-CPW two-stage amplifier. The substrate carrier is made of alumina. The carrier has the feedline patterns including dc bias lines and 50 Ω CPW transmission lines in Fig. 5. The feedline patterns and chip pads are connected by the flip-chip bonding bumps. The flip-chip bonding bump sizes are 50 $\mu$m in diameter and 30 $\mu$m in height.

As shown in Fig. 6(a) and (b), the measured $S$-parameters of the V-band two-stage amplifier with and without flip-chip bonding are very similar. The $S_{21}$ peak of the amplifier without flip-chip bonding is 14.81 dB at 53.5 GHz. After using the flip-chip bonding technique, the amplitude and frequency of the $S_{21}$ peak are slightly reduced and shifted to 14.52 and 53 GHz, respectively. The $S_{11}$ with and without flip-chip bonding are

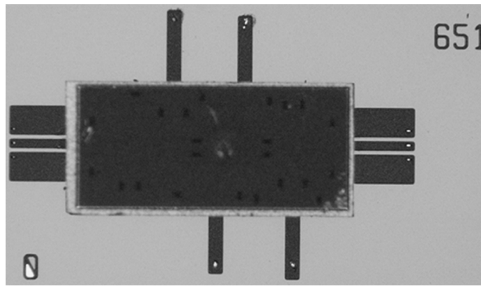
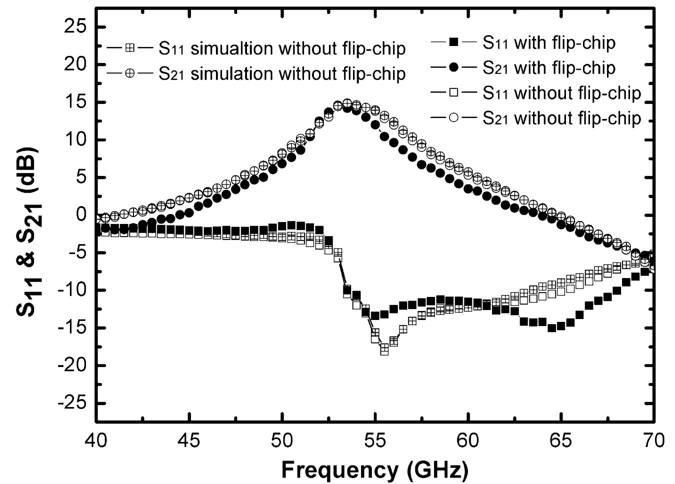


Fig. 5. Flip-chip photograph of the CPW–MS–CPW two-stage pHEMT amplifier.

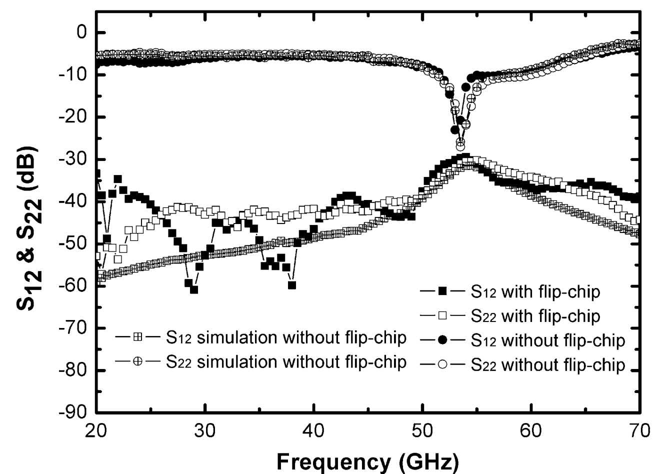
$-13.3$ dB and $-18.1$ dB near the operating frequency of 55 GHz, and the $S_{12}$ of them are lower than $-30$ dB anywhere. Obviously, the reverse isolation $(S_{12})$ of the flip-chip technique is insignificant to the performance of the bare-chip. $S_{22}$ of two curves are almost kept the same. The deepest $S_{22}$ without flip-chip bonding is $-27$ dB at 53.5 GHz, and the lowest $S_{22}$ with flip-chip bonding is $-23$ dB at 53.0 GHz. The measured results show the feasibilities of this design approach utilizing the CPW–MS–CPW topology for flip-chip bonding techniques. Besides, the simulation results and measured results without flip-chip bonding are also shown in Fig. 6(a) and (b) for comparison. The simulation results agree well with the measured results. Thus, the CPW–MS/MS–CPW transitions by the transistor device are wideband in nature.

## IV. Conclusion

The V-band CPW-MS-CPW two-stage amplifier compatible with flip-chip bonding techniques is proposed and demonstrated. The input and output networks of the proposed amplifier are constructed by the CPW-based transmission lines, forming the smooth electric interfaces for the flip-chip bonding package. Additionally, the proposed compact CPW-MS-CPW transition, which effectively integrates the pHEMT transistors, successfully converts the electromagnetic energy from the CPW mode to the MS mode. Such that the transition provides a wide degree of freedom to design the pHEMT amplifier with both CPW and microstrip elements. The prototype is fabricated using AlGaAs/InGaAs 0.15 $\mu$m pHEMT technology. After the prototype is packaged through the flip-chip bonding technology, there is negligible change on the electric characteristics. The measured results demonstrate the feasibility of the proposed CPW-MS-CPW two-stage pHEMT amplifier design for flip-chip bonding techniques.




(a)




**(b)**

Fig. 6. (a) $S_{11}$ and $S_{21}$ and (b) $S_{12}$ and $S_{22}$ of the simulated (without flip-chip bonding) and measured (with and without flip-chip bonding) CPW–MS–CPW two-stage pHEMT amplifier.

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