行政院國家科學委員會補助專題研究計畫成果報告

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※　　適用於無線通訊之互補式金氧半積體電路　　※
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計畫類別：□個別型計畫　　■整合型計畫
計畫編號：NSC 90-2215-E-009-115
執行期間：90 年 08 月 01 日至 91 年 07 月 31 日

計畫主持人：吳重雨 教授
計畫參與人員：周忠昀、徐國鈞、詹歸娣

本成果報告包括以下應繳交之附件：
□赴國外出差或研習心得報告一份
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□出席國際學術會議心得報告及發表之論文各一份
□國際合作研究計畫國外研究報告書一份

執行單位：

中 華 民 國 91 年 08 月 21 日

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中文摘要

由於超大型積體電路技術的微小化，使得電路的操作頻率可增高至射頻區域。而從已經發表的論文中可以看出，在無線通訊的領域中，2.4GHz **已經成為一個熱門而又確實能夠實現的射頻頻段，但在可預見的將來，**5.2 ~ 5.8 GHz **的免付費頻段也即將成為下一個重要的研究里程碑。而在** RF IC **的應用上，靜電保護電路不只需要有高的損壞臨界電壓以確保其良好的性能，還必須擁有低寄生電容和電阻，以降低** RC **延遲。所以一個** RFIC **的完成，實為整合** RFIC **電路設計、**ESD **設計、以及** VLSI **製程三個領域。**

此計劃的目標主要是驗證以0.18 ~ 0.13μm**場效金氧半電晶體的製程來實現**5.2 ~ 5.8 GHz **高頻段無線射頻金氧半電晶體收發機的可行性，配合對半導體製程的改進，經由電路設計加上靜電保護電路，完成一實際可用的** RFIC**。**

關鍵詞：射頻技術，次微米電晶體，射頻收發機，靜電放電(ESD), **靜電放電防護電路**

Abstract

As the VLSI technology continues scaling down, the circuit operation frequency improves and can be used in RF range. However, as various wireless standards continue to populate the 2.4GHz range, the next natural step is to extend the communications to the unlicensed 5.2 ~ 5.8 GHz band. Electrostatic discharge (ESD) phenomena continue to be a main reliability issue in CMOS IC's because of technology scaling and high frequency requirements. For RF IC's, the ESD protection design has some limitations: low parasitic capacitance, constant input capacitance, insensitive to substrate coupling noise, and high ESD robustness. So to implement RF IC's is to integrate the knowledge of VLSI technology、RF IC's circuit design and ESD protection design。

It is the aim of this project to evaluate the 0.18 ~ 0.13μm CMOS process for the development of RF transceiver front end for fixed wireless applications in the 5.2 ~ 5.8 GHz frequency band. Combine the improvement of VLSI technology, RF IC's circuit design and ESD protection design to realize a useful RF IC.

Keywords: RF technology, sub- m MOSFET, RF transceiver, Electrostatic discharge (ESD), ESD Protection Circuit

一、緣由與目的

此三年整合計畫包括一個總計劃與三個子計畫，分別是交通大學電子研究所荊鳳德教授的：Deep Sub-micro meter RF Devices **子計畫，和交通大學電子研究所吳重雨教授的：無線應用的** CMOS Transceiver **前端電路設計**(The design of CMOS Transceiver Front-end for Wireless Applications)**子計畫，與交通大學電子研究所柯明道助理教授的：適用於** GHz **頻段之輸出入靜電放電防護技術與銲墊設計子計畫。此三個子計畫研究核心相同，包含了適用於現今無線通訊的射頻元件製造、電路設計及保護電路。**

二、研究成果

1. 子計畫一

The measured frequency response of H_{21} and G_{max} are summarized in Table 1.

measured/ calculated values	mea. H_{21} (dB) 4GHz	mea. f_T (GHz) H_{21} =1	cal. f_T (GHz) H_{21} =1	mea. f_{max} (GHz) MAG =1	mea. f_{max} (GHz) MSG =1	cal. f_{max} (GHz) MSG =1	mea. G_{max} (dB) 4GHz	cal. G_{max} (dB) 4GHz
0.5-μm	14.7	25	23	20	82	80	13.0	13.9
0.25-μm	19.7	42	38	18	119	127	15.0	15.9
0.18-μm	22.2	58	56	17	161	171	16.3	18.0

H_{21}, f_t, G_{max}, and f_{max} gradually saturate as device scaling down. The saturation rate is faster for G_{max}

and a reducing f_{max} is even observed. Furthermore, the measured H_{21} and f_t are about 50% lower than the calculated value from conventional equation of $g_m/2\ C_{gs}$ or $v_{sat}/2\ \pi L_g$-$2L_{ov}$), where L_{ov} is the gate-drain overlap length. R_{nqs} becomes more important as increasing frequency near f_t. Good matching between measured and simulated f_t in Table 1 can only be obtained by considering the NQS effect. Because of the additional term, f_t increases slower than $1/L_g$ scaling down.

To further analyze the frequency response, we have also derived G_{max} and f_{max} by using the equivalent circuit modeling and including the NQS effect. From derived G_{max}, C_{gd} related pole gives the 10dB/decade G_{max} roll-off in MSG, while the large slope of ~30-40dB/decade in MAG is due to additional poles in K or the NQS effect on g_m.

Good agreement between the measured and calculated $f_{max,MSG=1}$ is achieved and shown in Table 1. The primirary parameter for $f_{max,MSG=1}$ increase is due to the g_m increase and C_{gd} decrease. In fact, C_{gd} is dominated by the C_{gdo} that is difficult to proportionally scale down with L_g.

We have also used numerical device simulation for further analysis. We have studied the NQS effect on G_{max} and f_{max}. The MAG increases with decreasing R_{nqs} and eventually gives G_{max} the same 10dB/decade roll-off as MSG when R_{nqs} equals 0. Therefore, the NQS effect is responsible for the transition from MSG to MAG. Because R_{nqs} is inversely related to C_{gs}, a higher dielectric or thinner gate thickness is required to improve the high frequency gain.

On the other hand, G_{max} has a simple analytical solution in the most useful MSG region for amplifier design. Because the $R_{nqs}(C_{gs}+C_{gd})$ related zeros are effective only at high frequencies, G_{max} in MSG can be further simplified and expressed by $g_m/\ C_{gd}$ or $v_{sat}/\ L_{ov}$. The numerical simulation results show that the reduction of C_{gdo} leads to a higher G_{max} and f_{max}. However, the difference between the ideal $2C_{ox}Wt_{ox}$ and the measured data is larger as scaling down.

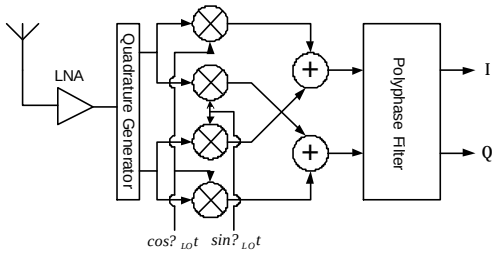
Here, a minimum C_{gdo} of $C_{ox}WL_{ov}$ ($L_{ov}=2t_{ox}$) is required in order to develop a reproducible and manufacturable process, where C_{ox} and t_{ox} are the gate capacitance and oxide thickness, respectively. Although down scaling gives a smaller L_g and a higher C_{ox}, limited G_{max} improvement in MSG is due to the slower scalable L_{ov}. The reason for L_{ov} failing to follow t_{ox} scaling down in deep sub- m devices is due to the lateral diffusion from source and drain impurities. High temperature annealing after source and drain implantation is necessary to reduce the junction leakage but largely increases the lateral diffusion. The formation of silicide junction also requires high temperature RTA. Because of the combined small G_{max} and K factor improvement, limited f_{max} improvement as device scaling down can be expected.

The smaller increase of measured G_{max} than calculated value in Table 1 as down scaling may be due to the parasitic effect neglected in our device model.

This paper has been submitted to IEEE MTT-S 2000.

2. 子計畫二

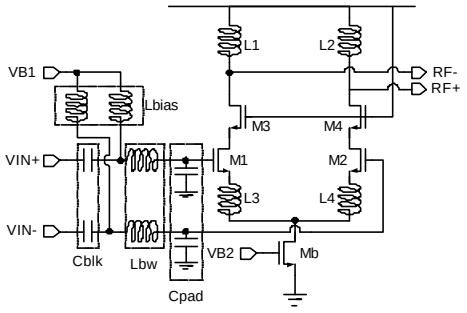
此計畫以 TSMC 018um **的製程來實現操作於** 5-GHz **的收發機前端電路。接收機採用雙正交的架構(如下圖)。此架構利用多相位濾波器來濾除鏡像雜訊，並能避免直接轉換架構的直流電壓問題，具有高整合性的優點；除此之外，將輸入射頻訊號轉成正交訊號後，可降低路徑不匹配的缺點，提高訊雜比。**



雙正交接收機架構圖

在計畫執行期間完成的電路有低雜訊放大器、正交相位調變器、多相位濾波器，其電路及性能如下：

a. **低雜訊放大器**

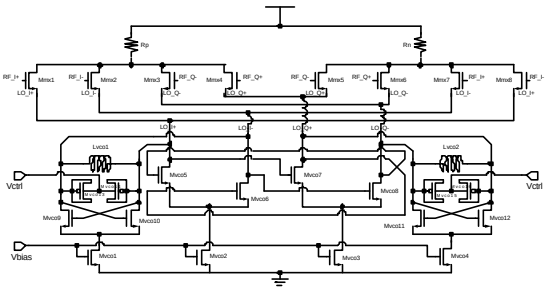


低雜訊放大器

在低雜訊放大器中，對雜訊影響最大的為輸入端的兩個電晶體 M1,M2，在固定功率消耗的考量下(5mW)，選擇最適當的閘極寬度，可得到最佳的雜音指數。Spiral Inductor L1,L2 與位於輸出端的寄生電容產生 5.05 GHz 的自振頻率。而 L3,L4 及 boundwire Inductors Lbw 則提供阻抗匹配以利最大功率傳輸。性能如下：

Gain	18.7 dB
Noise Figure	3.37 dB
IIP3	-5 dBm
Power Dissipation	5 mW

b.正交相位調變器



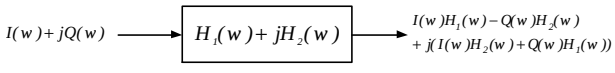
正交混波器及正交電壓控制震盪器

在此電路中 Mvco1~Mvco16 為電壓控制震盪器，Mvco9~Mvco12 產生負電阻抵消掉寄生電阻提供震盪的條件，電感 Lvco1,Lvco2 及 Mvco13~Mvco16 產生的可變電容決定震盪頻率，Mvco5~Mvco8 則產生正交的本地震盪訊號。Mmx1~Mmx8 為混波器，LO 訊號由源極進入，射頻訊號由閘極進入，混波器與 VCO 共用同一電流以節省功率。性能如下：

Power Dissipation	**4.5 mW**
Tuning Range	250 Mega
Conversion Gain	-0.35 dB

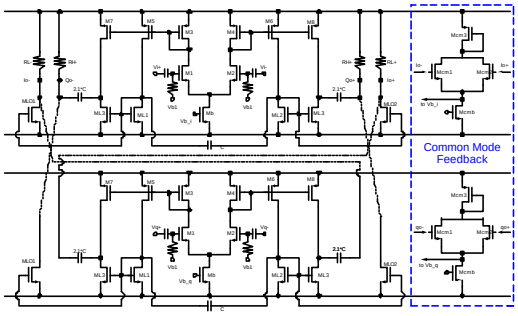
c.多相位濾波器

複數濾波器的操作原理如下圖：



複數濾波器的操作原理

適當的選擇實數濾波器的轉移函數即可以完成對正負頻率作篩選的功能，電路如下：



多相位濾波器電路圖

性能如下：

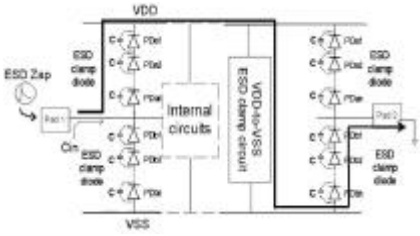
Channel Bandwidth	26 Mega Hz
Gain	9.36 dB
IRR	> 60 dB

此部分的研究成果已撰寫成論文並發表[1]。

3. 子計畫三

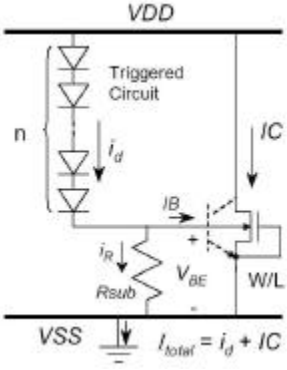
本計畫的研究成果已經整理且發表了二篇 *IEEE Conference* 論文[2][3]以及三篇國際期刊論文[4]-[6]。

在第一部份成果中[2][4]，我們設計了一組可供 *CMOS* 射頻電路所使用的 *ESD* 保護電路，此保護電路主要是由堆疊的複晶二極體作為輸入/輸出的 *ESD* 保護電路以達到減少寄生電容及基板共擾雜訊干擾的影響，如下圖：



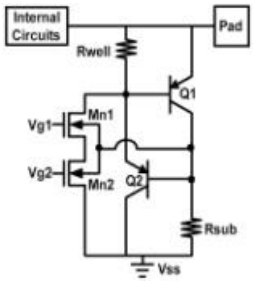
堆疊的複晶二極體作為 *RF ICs* 輸入端的 *ESD* 保護元件

另外搭配電源線間的 *ESD* 箝制電路使用，便可以提高整體的靜電耐受度，電路如下：



電源線間的 *ESD* 防護電路

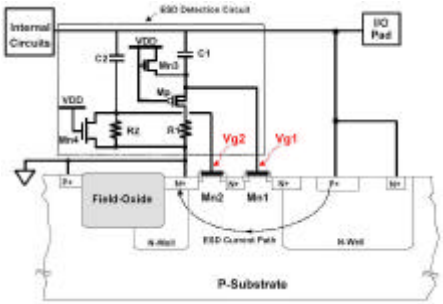
在第二部份成果中[3][5][6]，隨著半導體當電晶體元件尺寸被縮小，其操作電壓也隨之降低以維持元件的可靠性，可是外界傳輸的電路訊號之電壓準位大都依然維持在 5V, 這 5V 的電路訊號不能直接傳入深次微米的積體電路內部，因此在積體電路的輸出入端必需要有混合電壓輸出入界面電路來隔離輸入訊號的高電壓準位，但又必需把輸入訊號的電路訊號送入該積體電路內部。因此我們針對 *5V/3.3V* 混合式電壓輸出入界面電路的需求，提出了一組使用 *SNTSCR* 元件的新穎性 *ESD* 保護電路，如下圖：



SNTSCR 元件的等效電路圖

將堆疊的 NMOS 嵌入 SCR 元件中, 因此 *SNTSCR* 元件在混合式電壓輸出入界面電路中僅需使用薄的閘極氧化層就能避免氧化層可靠度的問題，而且可以減少生產成本。

為了讓 *SNTSCR* 元件更快導通將靜電的能量排掉，在本篇論文中也提出了新的閘極耦合(*gate-coupled*)觸發電路，如下圖：



混合式電壓輸出入界面電路的 *ESD* 防護電路

Vg1 偏壓在 VDD， *Vg2* 偏壓在 VSS，當 *I/O* 端的訊號為 5V 時，此保護電路也不會有氧化層可靠度的問題，而且 *SNTSCR* 元件處於關閉狀態，不會影響內部電路運作。在靜電放電的情況下，透過此閘極耦合觸發電路對堆疊 *NMOS* 的閘極提供大於其 *threshold voltage* 的偏壓，降低 *SNTSCR* 元件的第一次崩潰電壓，使其更快導通以提供內部電路更有效的保護。

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