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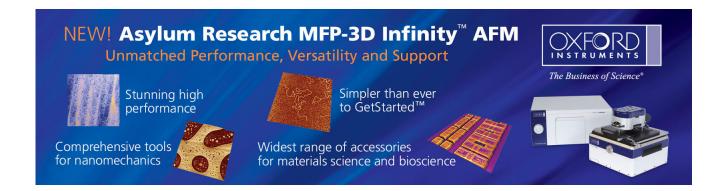
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# Modeling of nitrogen profile effects on direct tunneling probability in ultrathin nitrided oxides

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The dependence of the gate tunneling current ( $J_g$ ) on nitrogen profile (N profile) within an ultrathin silicon oxynitride film is reported. It was found that gate tunneling current is dependent on N profile, even with equal oxide thickness and nitrogen dosage. Gate tunneling current increased with steeper N profile, and it had higher sensitivity for p-type metal-oxide-semiconductor field-effect transistor (MOSFET) than n-type MOSFET. A direct tunneling model based on Wentzel-Kramers-Brillouin approximation has been proposed. The model described the influence of N profiles on gate tunneling current through local change of dielectric constant, band bending, and effective mass. Also, it reasonably explained the different  $J_g$  sensitivity in n-/p-MOSFETs, a phenomenon that has not been addressed in earlier publications. © 2008 American Institute of Physics. [DOI: 10.1063/1.2835706]

Device downscaling was initially achieved by simply reducing the physical thickness of SiO<sub>2</sub>. The downscaling of device thickness, however, causes gate tunneling current to increase exponentially and boron penetration issue to emerge. These issues pose great challenges to the continuation of the device downscaling. To overcome these issues, silicon oxinitride (SiON) was adopted extensively, and downscaling continues with the scaling of physical thickness and the increasing nitrogen concentration within SiON film. Nevertheless, excessive nitrogen concentration poses several other issues on device reliability, such as severe threshold voltage shift, lower mobility, and degraded negative bias temperature instability. Therefore, the control of nitrogen profile (N profile) in the ultrathin SiON becomes specially critical.<sup>2</sup> Successful N-profile engineering will definitely alleviate these issues mentioned, if not solve them completely.

Numerous publications have been reported to suppress the gate tunneling current through the incorporation of nitrogen into the SiON film. For the same effective oxide thickness (EOT), a lower tunneling current is possible to be achieved by increasing the nitrogen concentration. Numerous models also have been proposed to explain the dependence of nitrogen dosage on gate tunneling current. 4-6 In these models, uniformly distributed N profile is normally assumed. Little attention has been paid to study the influence of N profile on the gate tunneling current. Typically, the nitrogen profile is intentionally engineered to optimize the benefits in both device and reliability. In this work, the effects of different N profiles within an ultrathin SiON on the eventual gate tunneling current have been investigated. A model based on Wentzel-Kramers-Brillouin (WKB) approximation has been proposed to explain how the steeper N profile contributes to To investigate the impact of N profile on gate tunneling current, two kinds of SiON samples ("sample A" and "sample B") with different N profiles were fabricated. Sample A had a steeper N profile than sample B, as illustrated in Fig. 1. The N profile was measured using high-resolution angle-resolved x-ray photoelectron spectroscopy (XPS). Both thickness and N dosage were kept equal for the two kinds of samples. The corresponding electrical data in terms of EOT, inversion gate tunneling current ( $J_{\rho}$ ), and  $J_{\rho}$ 

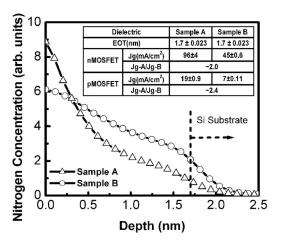
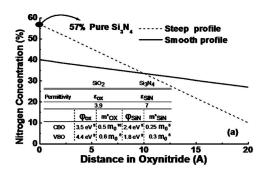


FIG. 1. Comparison of nitrogen depth profile (N profile) and gate tunneling current  $(J_g)$  for two kinds of SiON films with similar thicknesses and nitrogen concentrations. The N profile was measured using high resolution angleresolved XPS. Sample A (open triangle) has a steeper N profile than that of sample B (open circle). Gate tunneling-current density was measured at  $V_g = \pm 1$  V, with other terminals being connected to ground potentials.

the high gate tunneling current  $(J_g)$ . In addition, it well explains the evolution of tunneling current by considering the local variations in dielectric constant, band profile, and effective mass.

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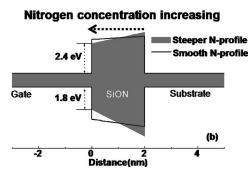


FIG. 2. (a) Schematic showing for two kinds of N profiles: the steep vs the smooth profile. The maximum nitrogen was set to be the pure nitride (N =57%). These two scenarios were used as simulation inputs to assess the impact of N profile to  $J_g$ . The various constants used in simulations are listed as the inset. (b) Simulation output (at  $V_{\rho}=0$  V) for the corresponding energy band diagrams shown in (a). It is assumed that the depth of distributed nitrogen concentration is kept equal. In the inset of Fig. 2(a), CB<sub>0</sub> and VB<sub>0</sub> are conduction band offset and valence band offset, respectively.

ratio (defined as  $J_{g-A}/J_{g-B}$ ) are summarized in the inset of Fig. 1. Two key observations were made from these experimental data. Firstly, sample A exhibits a higher  $J_g$  than that of sample B, for both n- and p-MOSFETs. Secondly,  $J_g$  ratio is higher in p-MOSFET than that in n-MOSFET, indicating that p-MOSFET has a higher sensitivity to  $J_g$  with the change of N profile. Based on the change of tunneling probability, a model arising from the localized band bending is proposed to explain these experimental data. In the model, WKB approximation is adopted to calculate the change of tunneling probability under various biasing conditions. The tunneling probability  $(T_t)$  could be expressed by

$$T_t = \exp\left[-2\int_0^{T_{\text{phy}}} \sqrt{\frac{2m^*(x)}{\hbar}} \left[\Phi_{\text{SiON}}(x) - E\right] dx\right], \qquad (1)$$

where  $T_t \equiv$  tunneling probability,  $T_{phy} \equiv$  physical thickness of dielectric,  $\Phi_{SiON} \equiv SiON/Si$  potential barrier, and  $m^*$  $\equiv$  carrier's effective mass and  $x \equiv$  distance into SiON, determined from the interface of poly Si and SiON.

Two parameters  $\Phi_{SiON}(x)$  and  $m^*(x)$ , under different gate biases, must be extracted first to solve  $T_t$ . Also, several assumptions were made to simplify the model. Firstly, the nitrogen concentration is assumed to vary linearly within the bulk of SiON. Secondly, the bulk of SiON film is assumed to consist of n pieces of very thin SiON strips with uniformly distributed nitrogen in the every strip. Thirdly, the energy barrier height  $(\varphi)$ , dielectric constant  $(\varepsilon)$ , and effective tunneling mass  $(m^*)$  for SiON are assumed to vary linearly with nitrogen dosage between oxide material constants and those for nitride, as reference to Muraoka et al. and Kraus et al. It follows that the various input parameters could be simplified as follows:

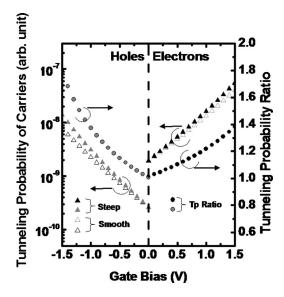


FIG. 3. Tunneling probability (TP) for electrons and holes under various biasing conditions. TP was obtained from simulation result by using our proposed model. The tunneling probability ratio (TP ratio) is defined as TP<sub>steep</sub>/TP<sub>smooth</sub>.

$$N(x) = a_1 x + a_2, \tag{2}$$

$$\varphi(N) = \varphi_{ox} + (\varphi_{SiN} - \varphi_{ox}) \frac{N}{N_{SiN}}, \qquad (3)$$

$$\varepsilon(N) = \varepsilon_{ox} + (\varepsilon_{SiN} - \varepsilon_{ox}) \frac{N}{N_{SiN}},$$
 and (4)

$$m^*(N) = m_{ox}^* + (m_{SiN}^* - m_{ox}^*) \frac{N}{N_{SiN}},$$
 (5)

where  $a_1$  and  $a_2$  are constants, and we can obtain a variety of linear N profile shapes by modifying those values. The N and N<sub>SiN</sub> are nitrogen concentrations at. % in the oxynitride film and the pure nitride film, respectively. The other used constants are summarized in the inset of Fig. 2. Substituting these parameters  $[\varphi(x), \varepsilon(x), \text{ and } m^*(x)]$  into the main expression in Eq. (1), we could simulate the tunneling probability through the different potential barriers. Figure 2(b) shows the simulated band diagram under a gate bias  $(V_p)$  of 0 V.

For  $V_{\varrho} \neq 0$ , Poisson's equation shall be adopted to describe the nonhomogeneous change of dielectric constant within SiON:

$$\frac{d}{dx} \left[ \varepsilon(x) \frac{dV_{SiON}(x)}{dx} \right] = \rho = 0, \tag{6}$$

where  $V_{\text{SiON}}(x)$  and  $\rho$  are representing the potential and free charge density within SiON, respectively. Solving for Poisson's equation, the band diagram of SiON film with different N profiles can be simulated (not shown). Therefore, the corresponding tunneling probability for n-MOSFET under  $V_g$ > 0 V and for p-MOSFET under  $V_g < 0$  V can be simulated.

To examine our model, two kinds of SiON samples with different N profiles are considered, as depicted in Fig. 2(a). Both samples have equal nitrogen concentrations and film thicknesses. Under zero bias (i.e.,  $V_g=0$  V), the simulated energy band diagrams are shown in Fig. 2(b). The SiON sample with a steeper N profile exhibits a steeper conduction band (CB) and valence band (VB) bendings. Take note that

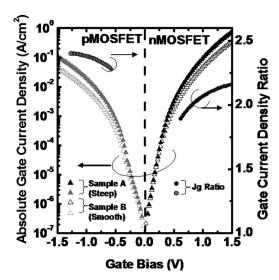


FIG. 4. The gate leakage current density  $(J_g)$  for n-MOSFET and p-MOSFET under various bias conditions. The gate current density  $(J_g)$  ratios of the steep profile to the smooth profile for n-/p-MOSFETs were also presented. The carrier transport mechanism in the bias range of  $J_g$  ratio can be attributed to the direct tunneling, which is verified by conduction processes fitting (see the Ref. 7).

the degree of VB bending is steeper than that of CB. This is attributed to the greater VB offset (than CB offset) difference, comparing  $SiO_2$  to  $Si_3N_4$ , as shown in the inset of Fig. 2(a).

Under nonzero biasing (i.e.,  $V_{\varrho} \neq 0$ ), there will be an additional voltage drops across the silicon oxinitride ( $V_{SiON}$ ). Hence, it is necessary to consider both  $\varphi(x)$  and  $V_{SiON}(x)$  for constructing the potential barrier, while simulating the energy band diagrams. Considering minority carriers under operation mode (at low electric field), <sup>10</sup> the simulated tunneling probability for electrons (in n-MOSFET) under positive biasing, and holes (in p MOSFET) under negative biasing are plotted in Fig. 3. These experimental results are also shown in Fig. 4. These *I-V* curves in Fig. 4 are the average results of five devices for each kind of samples. The gate current density  $(J_{\rho})$  ratios of the steep profile to the smooth profile for n/p-MOSFETs are also presented. The range of gate bias for measuring  $J_{g}$  ratios is just shown between -1.25--0.5 V for p-MOSFET and between 0.5 and 1.5 V for n-MOSFET. The carrier transport mechanism in the bias range can be attributed to the direct tunneling behavior, which is verified by conduction processes fitting.

According to simulated results, it shows that the sample with steeper N profile exhibits a higher tunneling probability, valid for both n- and p-MOSFETs. This result agrees well with our experimental data in Fig. 4. On the other hand, defining the tunneling probability ratio (TP ratio) as  $TP_{\text{steep}}/TP_{\text{smooth}}$ , it is observed that holes (in the p-MOSFET) have a higher TP ratio than electrons (in the n-MOSFET). In other words, SiON with steeper N profile gives rise to a higher  $J_G$  increase. This is particularly true for p MOSFET because VB bending is more sensitive to N profile change than CB bending, as predicted by our model.

In summary, we have proposed a model based on WKB to well explain the gate tunneling current through thin SiON film with different N profiles. The change in N profile influences the band shape of SiON film, leading to the change in the tunneling probability. The SiON film with a steeper N profile will exhibit a higher gate tunneling current. Also, the phenomenon is more apparent in *p*-MOSFET than in *n*-MOSFET. The higher sensitivity of VB bending toward N profile change reasonably explains that *p*-MOSFET is showing a larger current increment than *n* MOSFET.

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<sup>1</sup>N. Kimizuka, K. Yamaguchi, K. Imai, T. Iizuka, C. T. Liu, R. C. Keller, and T. Horiuchi, IEEE Symposium on VLSI Technology, *Digest of Technical Papers*, 13–15 June 2000, p. 92.

<sup>2</sup>C.-C. Chen, V. S. Chang, Y. Jin, C.-H. Chen, T.-L. Lee, S.-C. Chen, and M.-S. Liang, IEEE Symposium on VLSI Technology, *Digest of Technical Papers*, 15–17 June 2004, p. 176.

<sup>3</sup>M. Terai, K. Watanabe, and S. Fujieda, IEEE Trans. Electron Devices **54**, 1658 (2007).

<sup>4</sup>H. Yu, Y. T. Hou, M. F. Li, and D. L. Kwong, IEEE Trans. Electron Devices **49**, 1158 (2002).

<sup>5</sup>M. Togo, K. Watanabe, T. Yamamoto, N. Ikarashi, T. Tatsumi, H. Ono, and T. Mogami, IEEE Trans. Electron Devices 49, 1903 (2002).

<sup>6</sup>K. Muraoka, K. Kurihara, N. Yasuda, and H. Satake, J. Appl. Phys. **94**, 2038 (2003).

<sup>7</sup>S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (Wiley, New York, 2007) Vol. 48, p. 227.

<sup>8</sup>P. A. Kraus, K. Z. Ahmed, C. S. Olsen, and F. Nouri, IEEE Trans. Electron Devices **52**, 1141 (2005).

<sup>9</sup>J. Robertson, J. Vac. Sci. Technol. B **18**, 1785 (2000).

<sup>10</sup>Y. C. Yeo, Q. Lu, W. C. Lee, T.-J. King, C. Hu, X. Wang, X. Guo, and T. P. Ma, IEEE Trans. Electron Devices 21, 540 (2000).