Miniature RF Test Structure for On-Wafer Device Testing and In-Line Process Monitoring

Ming-Hsiang Cho, *Student Member, IEEE*, Ryan Lee, An-Sam Peng, David Chen, Chune-Sin Yeh, and Lin-Kun Wu, *Member, IEEE*

***Abstract*—In this brief, a miniature test structure for RF device characterization and process monitoring has been proposed. This new layout design can minimize the voltage drop across interconnects and can prevent capacitive coupling to devices. It consumes only 36% and 40% of the chip area of the conventional on-wafer and in-line test structures, respectively. The RF characteristics of the proposed test structure are shown to be in excellent agreement with those of the conventional ones.**

***Index Terms*—MOSFET, process monitoring, RF, scribe line, test structure.**

I. Introduction

With the progress of CMOS process technology, device unity-gain frequency has reached the microwave regime and beyond. It has become more and more significant for process engineers and circuit designers to characterize the silicon-based devices at such high frequencies. As shown in Fig. 1(a), a conventional on-wafer RF test structure is usually laid out in the east–west configuration. The microstriplike interconnects are introduced to reduce the capacitive coupling between the device and probe pads. However, these access lines not only occupy a considerable chip area but also increase IR drop across them. In addition, the conventional on-wafer RF test structure is difficult to be inserted into the scribe line for process monitoring due to its specific configuration.

In previous literatures [1], [2], the in-line RF test structures have been presented to monitor an RF CMOS process. As shown in Fig. 1(b), two ground-signal-ground (GSG) probe pads in these test fixtures are aligned in a row (or in a column) and thus can be placed within a scribe line. Although these in-line test structures are flexible and suitable for both on-wafer testing and process monitoring, they still consume much chip area and suffer from large IR drop and interconnect parasitics. Recently, an area-efficient RF test structure [3] was presented. As shown in Fig. 1(c), this improved test structure rearranges the GSG probe pads to fit in a ground-signal-ground-signal-ground (GSGSG) probe and requires about 60% of the chip area for a conventional on-wafer test structure. In this brief, we propose a new compact layout to further reduce the chip area of RF test structures. As shown in Fig. 1(d), the MOS transistor is slightly off center to prevent the direct coupling from the signal pads to the device. Consequently, both the spacing between two GSG probe pads and the length of interconnect can be substantially reduced. By employing the shielding technique [4], the noise coupling through silicon substrate can be suppressed, and the industry-standard open-short deembedding method [5] can be used to accurately subtract the external parasitics surrounding the MOS transistor. This miniature RF test fixture consumes only 36% of the chip area of a conventional on-wafer test structure and is suitable for characterizing and monitoring various devices such as MOSFETs, BJTs, varactors, capacitors, resistors, etc. To substantiate the proposed RF test structure, the MOS transistors and corresponding dummy structures were fabricated using a 90-nm RF CMOS process and characterized up to 30 GHz with a two-port S-parameter measurement system.

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II. Miniaturization of RF Test Structures

A. Conventional On-Wafer and In-Line Test Structures

As shown in Fig. 1(a), the conventional on-wafer RF test structure is designed to mount the devices with probe pads and interconnects. Both dc and RF sources can be combined with bias-T networks and then delivered to the test fixture through microwave cables and probes. In general, the gate and drain of a MOS transistor are, respectively, connected to the input and output signal pads, whereas the source and bulk are tied together to the ground reference. Moreover, the ground plane (M_1) is laid out as close to the MOS transistor as possible to minimize the IR drop and parasitic effects of the dangling leg in the source terminal [6].

Fig. 1(b) shows the conventional in-line test structure. To monitor a process, the on-wafer test structure should be inserted into a scribe line between two adjacent dies, and hence, its total width should be typically less than 80–100 μm [2]. Once the electromagnetic wave is propagated along the input/output interconnects within the limited space of the in-line test fixture, the substrate noise coupling between the signal and ground traces would be considerable and should also be taken into account for the analysis. To simplify this task, the bottom metal layer (M_1) can be connected to the ground pads to shield the lossy silicon substrate. Consequently, both substrate leakage and port-to-port coupling can be significantly mitigated [4]. As

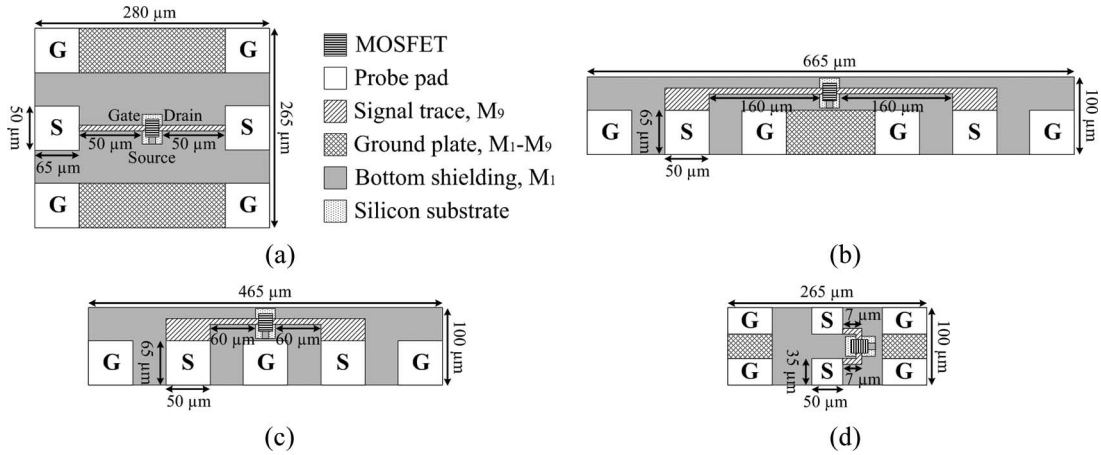

Fig. 1. Illustration of RF test structures for on-wafer device testing and in-line process monitoring. (a) Conventional on-wafer GSG test structure. (b) Conventional in-line GSG test structure. (c) In-line GSGSG test structure. (d) Proposed miniature GSG test structure. The width of the interconnect is 9 μm, and the estimated resistances of each interconnect for (a)–(d) are 0.27, 0.86, 0.32, and 0.04 Ω, respectively.

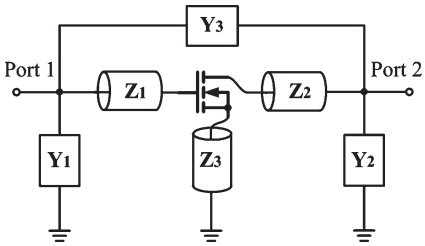

Fig. 2. Lumped equivalent-circuit representation of a fixtured MOS transistor for on-wafer device testing and in-line process monitoring.

shown in Fig. 1(c), the GSGSG (or GSSG) RF probes can also be utilized to further reduce the length of interconnect [3].

B. Proposed Miniature RF Test Structure

Fig. 2 shows the parasitic model of an RF MOSFET test structure. The shunt parasitics Y_1 and Y_2 are the admittances of the probe pads and interconnects at the two ports, and Y_3 is the capacitive coupling between them. The series parasitics Z_1, Z_2, and Z_3 represent the impedances of the probe pads and interconnects in the gate, drain, and source terminals, respectively. Since the shielding technique is introduced here, the shunt and series parasitic networks surrounding a MOS transistor can be faithfully reproduced from the open and short dummy structures [4] and subtracted out in Y- and Z-domains [2], respectively. For the design of RF MOSFET test structures, interconnects should be wide and short to reduce the IR drop across Z_2 and Z_3. As the spacing between two signal pads becomes shorter, however, care must be taken to avoid coupling from signal pads to the MOS transistor. Fig. 3 shows that the measured probe-to-probe capacitance increases as the spacing between two face-to-face GSG probes decreases. This implies that the RF characteristics of a MOS transistor between two close signal pads will suffer from a strong electric field and associated problems, which cannot be easily modeled.

In this brief, to overcome these difficulties, we propose a miniature RF test structure suitable for on-wafer device testing and in-line process monitoring. As shown in Fig. 1(d), the MOS transistor is located in an area between the signal and ground pads to prevent the electric field penetrating into the device.

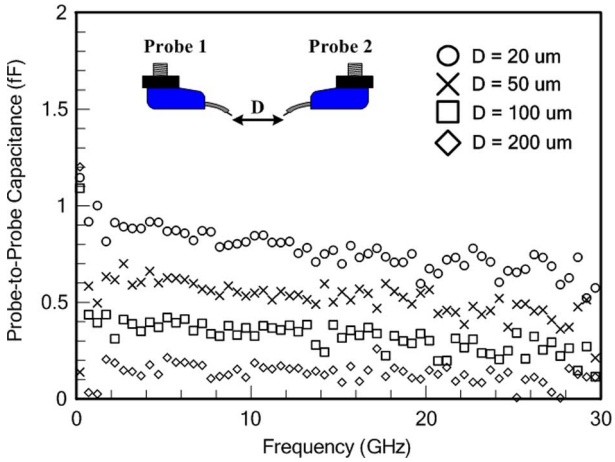

Fig. 3. Forward capacitive coupling between GSG RF Probes. Two infinity probes were placed in air, with different separation distances. The reference plane of each port was shifted to the probe tips using the short-open-load-thru calibration procedure.

Therefore, the pad-to-pad spacing can be minimized, and fixture size can be significantly reduced. Moreover, small signal pads ($35\ \mu\text{m} \times 50\ \mu\text{m}$) and short interconnect ($7\ \mu\text{m} \times 9\ \mu\text{m}$) are used to mitigate the coupling capacitance between pads as well as the voltage drop across interconnects. This miniature RF test fixture requires only 36% and 40% of the chip area of the conventional on-wafer and in-line test structures, respectively, and it can be used for both device characterization and process monitoring.

III. Results and Discussion

A 90-nm nine-metal-layer RF CMOS process was used to fabricate the MOSFET test structures and deembedding dummies. The NMOS transistors with a channel length of $(L) = 90$ nm and a channel width of $(W) = 64\ \mu$m ($4\ \mu\text{m} \times 16$ fingers) were connected in a two-port common-source configuration. The dc and RF measurements of the on-wafer and in-line test fixtures were carried out on an HP 4142B Modular DC Source/Monitor and an HP 8510C Vector Network Analyzer, respectively. Before S-parameter measurements, the system

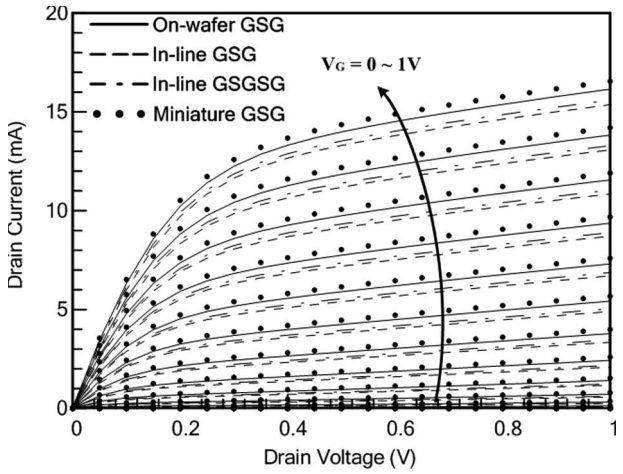

Fig. 4. DC characteristics obtained from the on-wafer and in-line MOSFET test fixtures. I_D–V_D curves for $V_G = 0 - 1$ V with 50-mV steps.

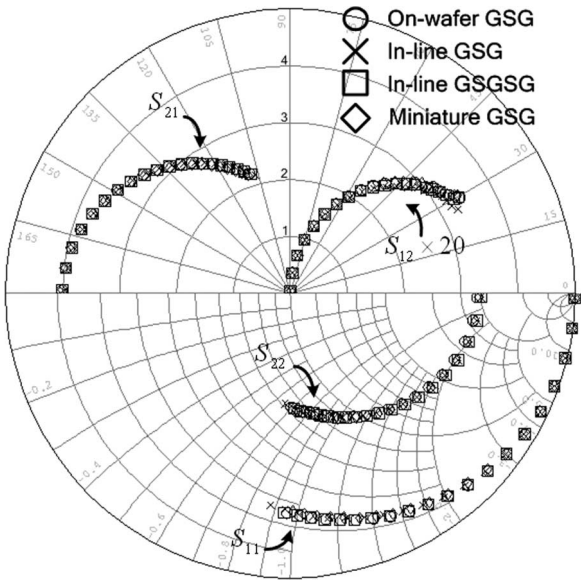

Fig. 5. S-parameters obtained from the on-wafer and in-line MOSFET test structures using the standard open-short deembedding method [5]. The MOSFETs were biased at $V_G = V_D = 1$ V, and the S-parameter measurements were performed from 0.1 to 30 GHz with 0.1-GHz steps.

was calibrated up to 30 GHz using the line-reflect-reflect-match calibration procedure with Cascade Microtech Infinity RF probes and an impedance standard substrate. It should be noted that both dc and RF characteristics were measured with the same devices-under-test (DUTs) to mitigate the effects of process variation.

Fig. 4 shows the measured dc I_D–V_D curves of the on-wafer and in-line MOSFET test structures. Compared with the conventional test structures, the proposed miniature test structure demonstrates the highest drain currents under various gate/drain bias conditions. This indicates that the IR drop across the interconnects will degrade the dc characteristics as well as the other parameters of the MOS transistors. Fig. 5 shows the deembedded reflection coefficients (S_{11} and S_{22}) and transmission coefficients (S_{12} and S_{21}) of the RF MOSFET test fixtures. It is shown that the results obtained from the proposed RF test

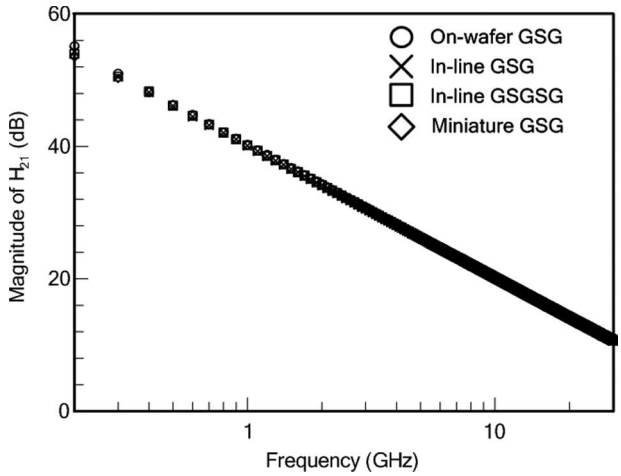

Fig. 6. Current gain H_{21} as a function of frequency using the standard open-short deembedding method. The MOSFETs were biased at $V_G = V_D = 1$ V, and the S-parameter measurements were performed from 0.1 to 30 GHz with 0.1-GHz steps.

structure and the conventional ones, except the conventional in-line GSG structure, are in excellent agreement over the entire frequency range. This small inconsistency in the deembedded S-parameters may be caused by the higher IR drop and/or the larger interconnect parasitics, which cannot be properly modeled by open-short deembedding [7], of the conventional in-line GSG test structure. Fig. 6 also shows no significant difference in gain-frequency response between the conventional and proposed test structures. Based on the aforementioned results, the proposed miniature RF test structure can be used to acquire reliable dc and RF characteristics of the MOSFETs and to reduce the consumption of the chip area. The fixture size of the proposed design is compact and could be further reduced; nevertheless, pad size would be limited by the tip size and skating distance of the RF probe. Theoretically, there is no lower limit for the pad-to-pad spacing that can be realized. However, care must be taken to ensure probing consistency when two signal pads are placed as close as possible. For instance, the automatic measurement system can be applied to achieve a good probing stability.

IV. Conclusion

In this brief, we propose a miniature RF test structure suitable for both device testing and process monitoring. With the application of shielding technique and careful design of the probe pads and interconnects, the chip area of the proposed layout can be reduced to less than 40% of the conventional ones. Compared with the conventional RF test structures, the proposed new design shows lowest voltage drop and consistent RF characteristics.

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