行政院國家科學委員會補助專題研究計畫成果報告

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計畫類別：▒個別型計畫　　□整合型計畫
計畫編號：NSC 88－2215－E－009－056
執行期間：88 年 8 月 1 日至 89 年 7 月 31 日

計畫主持人：陳明哲

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□國際合作研究計畫國外研究報告書一份

執行單位：國立交通大學電子工程學系

中　華　民　國　89　年　8　月　24　日

行政院國家科學委員會專題研究計畫成果報告

低功率低電壓數位類比積體電路之晶片實現及設計法則(五)

Implementation and Methodology for Low Power/Low Voltage Digital and Analog Integrated Circuits(Ⅴ)

計畫編號：NSC 88-2215-E-009-056
執行期限：88 年 8 月 1 日至 89 年 7 月 31 日
主持人：陳明哲教授　　國立交通大學電子工程學系

一、中文摘要

本計劃承襲我們以往於低功率低電壓積體電路領域之研究成果, 繼續作更深入完善之研究。進行的項目是：(1)根據閘控橫向雙載子結構及背閘技術製作新式記憶細胞晶片之實現、測試及設計法則；(2)背閘動態控制臨界電壓之新式數位電路以環振盪晶片形式實現、測試及設計法則；(3)混合式積體電路中低功率低電壓取樣保存電路晶片之實驗研究及設計法則；(4)提高電路品質的新式匹配改善技巧及解析設計模式；(5)次臨界互補式金氧半基本類比計算及電壓參考源晶片之製作 測試及設計法則; 及(6)閘控雙載子及互補式金氧半元件雜訊量測分析。 本計劃產生之成果除以論文專利及實作展示顯現外, 對於國內半導體工業在此一低功率低電壓嶄新領域之發展將有極大助益。

關鍵詞：低功率，低電壓，記憶體，數位類比，積體電路，混合式，次臨界，匹配，可攜帶型，雜訊

Abstract

As highlighted by the research achievements over the three years, this project has extensively investigated the low power/low voltage integrated circuits. The topics performed are:(1) implementation, measurement, and design methodology of the novel Memory chip based on a high-gain gated lateral BJT structure as well as on a back-gate bias technique; (2) chip implementation , measurement and design methodology of new digital circuits in terms of a ring oscillator by means of back-gate controlled dynamic threshold voltage; (3) experimental study and design methodology of sample/hold chips for low power/low voltage mixed mode IC; (4) new match improvement techniques and analytic design model for enhanced circuit quality; (5) basic analog computation circuits and voltage references utilizing subthreshold CMOS; and (6) Noise characterization and analysis of gated BJTs and CMOS. The achievements created from the project will be demonstrated in terms of paper, patent, and also practical show. In addition, our work will be a great aid to our semiconductor industry in the new field of low power/low voltage integrated circuits.

Keywords: Low power, Low voltage, memory, digital-analog, IC, mixed-mode, subthreshold, match, portable, noise

二、緣由與目的

低電壓低功率消耗可攜帶型(portable)器具設備已是時勢潮流，反映於半導體工業上無論製程技術或電路設計法則處處都可見到此潮流帶來的衝激。國際上低電壓低功率電子(Low voltage、Low power Electronics)方面的研究一日千里進展極快。

三、研究方法與成果

(i) 一種新式 SRAM 記憶胞 cell(此為在 CMOS 製程相容下，應用高電流增益閘控橫向雙載子電晶體之特性在低電源電壓下就可得 base current(基極電流)逆向現象，利用此現象以實驗證明具有 SRAM cell 性能，卻僅需二個 MOSFETs 元件即可，比傳統形式大幅降低消耗之面積)，亦獲得中華民國及美國專利。

(ii) 一種動態(dynamic)臨界電壓(threshold voltage)技巧(在數位 switching 時 active，將 back-gate 予以 slightly forward biased 但在 stand-by 時則 back-gate 予以 reverse bias，如此就可在訊號變化時增加充電或放電電流，且在 stand-by 時可保持 off-current 最小值以降低 stand-by power；為實現低電壓低功率數位電路之有效方法之一)，亦獲得美國及中華民國專利。

(iii) 一種類比開關(Analog Switch)或 Sample-and-Hold(取樣保存)(低電壓低功率 Analog Switch 或 Sample/Hold 亦是 mixed IC 關鍵部份，我們亦已發展出新式補償電路技術以克服 charge injection 電荷注入)。

(iv) 一種改進 match 匹配技巧(我們已發展出以 back-gate slightly forward biased 技巧即可改進低電壓數位及類比電路之元件匹配能力，此為 CMOS 製程相容，並無引起 Latch-up 鎖定或干擾之疑慮)。

(v)由於在發生 Soft Breakdown 之後擾動現象已經被觀察到，並且可由量測到 RTS(Random Telegraph Signal) 的行為獲知。然而，目前本研究群想藉由 l/f noise 來觀察發生 Soft Breakdown 之後的現象，建立與 l/f noise 之間的關連，並深入了解其物理機制。在此方面，我們也有相當不錯的研究成果，並已提出一篇 paper 在 7 月 JAP 2000 年。

四、結論與討論

(a) 在 back-gate bias 技巧方面,我們已成功分離出二種不同的 band-to-band tunneling 成份(一為 surface,一為底下 bulk):

- Ming-Jer Chen, Huan-Tsung Huang, Chin-Shan Hou, Kuo-Nan Yang, "Back-gate bias enhanced band-to-band tunneling leakage in scaled MOSFET's," IEEE Electron Device Letters, vol.19, pp.134-136, April 1998.

此成果可為設計法則定出 Low voltage safe window 以開發新式技術元件及電路.本論文被 1999 IEEEE IEDM 引用開發 Low Power Process: "Ultra-low leakage 0.16um CMOS for low-standby power applications," p.671

(b) Mismatch 除了 transistor 外, capacitor 亦頗重要.我們已與 TSMC 就 0.35um mixed-mode Process 進行合作,開發成功 IPO(inter-poly oxide) capacitor,並獲 Taiwan 及 USA patent:

- Chin-Shan Hou, Ming-Jer Chen, "Cross-coupled capacitors for improved voltage coefficient," US patent 6069050,2000.
- Chin-Shan Hou, Ming-Jer Chen, "Cross-coupled capacitors for improved voltage coefficient ,"ROC patent 098946."
- M. J. Chen, C. S. Hou ," A novel cross-coupled Inter-Poly-Oxide capacitor for mixed-mode CMOS processes," IEEE Electron Device Letters, p.360, July 1991.

(c) 費時的 Mismatch 量測 wafer data 已大幅推進至 0.15um 製程並建立新的統計模式.

(d) Back-gate forward bias 操作的 gated-diode 結構用於早期 CMOS 熱載子預警器已在 TSMC 0.25um 製程實地驗證成功: M.J. Chen & T.K. Kang, "low-voltage forward gated diode:

an early monitor of carrier degradation in scaled MOSFET's," IEEE IPFA, p.195, July 1999.

(e) 一種新穎補償電荷注入技巧(US patent 5479121), 已被工研院微電子部門引用研發成功視訊類比數位轉換器.

(f) 一篇 back-gate bias 論文被引用於 1997 Proceedings of the IEEE(special issue on nanometer-scale science & technology). 2000 ISSCC 有為數不少的論文探討 back -gate bias 之潛力及產品證實.

(g) 一篇 Analog Switch 論文被引用於 1998 IEEE International SOI Conference 及其它 IEEEE journals, 且此類比電路近來大幅用於評估 thin oxide tunneling 之影響 (如 1999 IEEE IEDM).

(h) 一篇 mismatch 論文被引用於 1998 IEEE International Workshop on Statistical methodology 及 1999 IEEE Trans. CAD of Integrated Circuits and Systems.

(i) 指導學生何繼勛博士論文獲得 1996 年宏碁龍騰博士論文獎.

(j)已完成在 2000 年七月一篇關於"1/f noise in n-channel metal-oxide-semiconductor field-effect transistors undergoing soft breakdown"，基於我們的研究成果與豐富經驗, 可進一步深入研究發生 SBD 之後元件的 1/f noise 退化情況，並深入探討其雜訊的物理機制, 以建立物理解析的模式來重現實驗數據。

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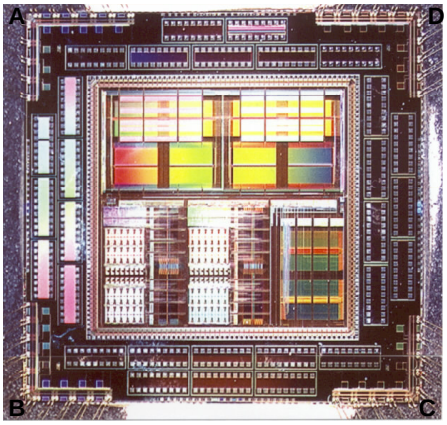


Fig. 1 Micrograph of test chip

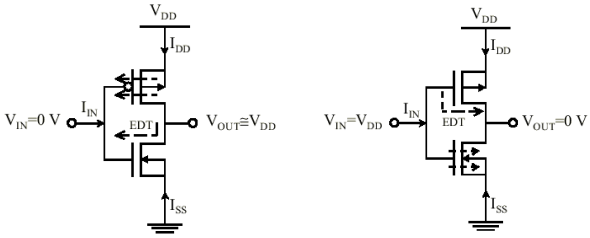


Fig. 2

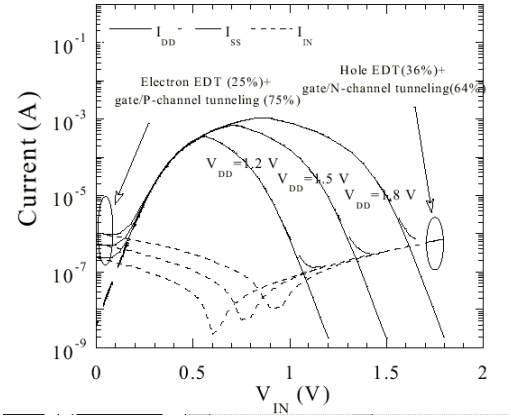
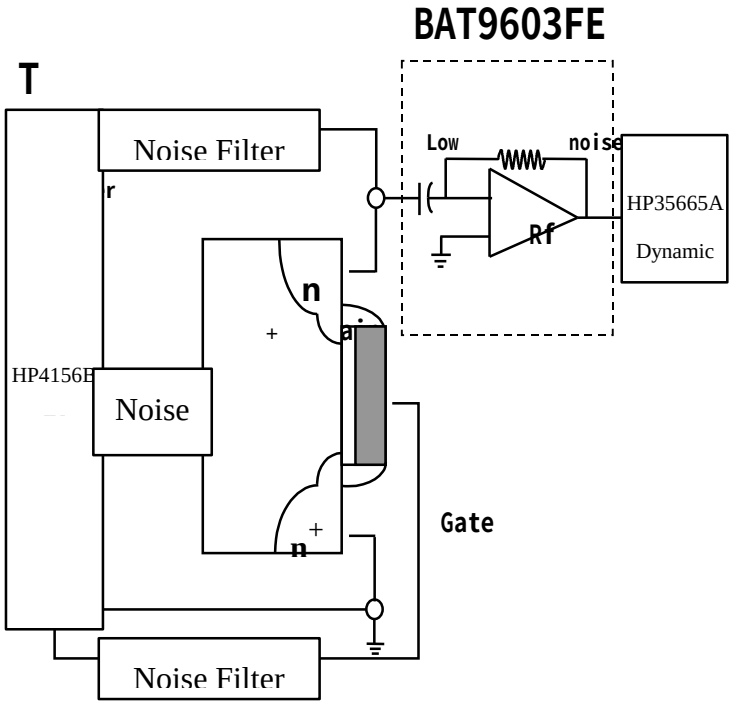


Fig.4



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