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Effect of the single grain boundary position on surrounding-gate polysilicon thin film transistors

Yiming Li[1], **Jung Y Huang**[2] **and Bo-Shian Lee**[3]

[1] Department of Communication Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan
[2] Department of Photonics, National Chiao Tung University, Hsinchu 300, Taiwan
[3] Display Institute, National Chiao Tung University, Hsinchu 300, Taiwan

E-mail: ymli@faculty.nctu.edu.tw

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Abstract

In this paper, single-grain-boundary (GB)-position-induced electrical characteristic variations in 300 nm surrounding-gate (i.e., gate-all-around (GAA)) polysilicon thin film transistors (TFTs) are numerically investigated. For a 2T1C active-matrix circuit, a three-dimensional device–circuit coupled mixed-mode simulation shows that the switching speed of GAA TFT can be improved by nine times, compared with the result of the circuit using single-gate (SG) polysilicon TFTs. The position of a single GB near the drain side has an bad effect on device performance, but the influence can be suppressed in the GAA polysilicon TFTs. We found that under the same threshold voltage, the variation of the threshold voltage can be reduced from 15% to 5%, with varying gate structures of the GAA polysilicon TFT.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The grain size of polysilicon thin film transistors (TFTs), which is currently larger than 1μm (see, for instance, [1] and references therein), plays an important role in polysilicon TFT devices and driving circuit with either long channel [2] or submicron [3] channel length polysilicon TFTs. Though the grain size of polysilicon film quality has been significantly improved, grain boundaries (GBs) still exist randomly in the device channel and influence the characteristics of the device and circuit. When the channel length is decreased to the polysilicon grain size, the TFT devices may contain at most a single GB in the channel [4]. This can happen for example, by using modern metal-induced lateral crystallization or excimer laser annealing methods to control the gain size [5]. In this case, the performance of submicron polysilicon TFT is strongly limited by the presence of trap states at the grain boundary. Such a problem will result in a nonuniform spatial distribution of electrostatic potential and causes significant variation of threshold voltage (V_{th}) in the driving transistors. There are two ways for improvement: one is to develop a new active-matrix driving method and reduce the variation by a compensation technique [6]. The other is to adopt advanced gate structures, although proper models for trap states at grain boundaries have to be developed [7]. Those advanced multiple-gate structures will not only suppress short channel effects but also reduce the width of channel, which lead to the increase in the active area and aperture ratio. The position of the GB causes V_{th} variation [8], and becomes more significant for deep-submicron polysilicon TFT devices.

In this paper, effects of the single-grain-boundary position on electrical characteristics with 300 nm surrounding-gate (i.e., gate-all-around (GAA) polysilicon TFTs are numerically investigated. We extracted the energy barrier height of the grain boundary and the concentration of carrier traps from measured data. With the physical model and parameters, three-dimensional (3D) drift–diffusion (DD) equations are solved numerically. A lightly doped drain (LDD) profile was used in order to reduce the leakage currents of single-gate (SG) and GAA polysilicon TFTs. We adjusted the doping concentration and work function to yield a satisfied threshold voltage for both device structures according to Seto's model [9]. The position near the drain side has a significant effect on device performance. The influence can be suppressed with

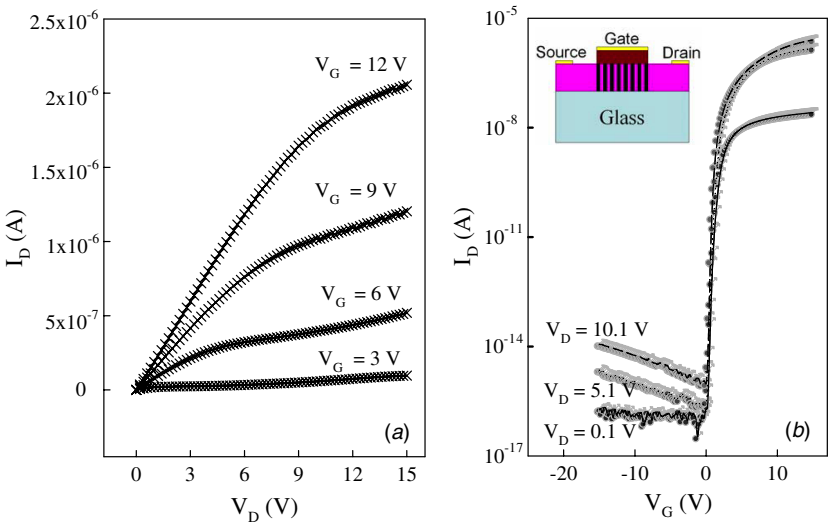

Figure 1. Comparison of (*a*) I_D–V_D and (*b*) I_D–V_G between measured (symbol curve) and simulated (solid curve) for n-type polysilicon TFT with $W = 5\ \mu$m and $L = 5\ \mu$m.

GAA polysilicon TFTs. With the same threshold voltage of SG polysilicon TFT, the $V_{\rm th}$ variation can be reduced to less than 5%, with varying gate structures of GAA polysilicon TFTs. We demonstrate the 2T1C active-matrix driving circuit using GAA and SG polysilicon TFTs for the OLED device [10]; and the results are fairly encouraging. The circuit with GAA polysilicon TFTs exhibits a nine-time improvement in switching speed, compared to that with the SG polysilicon TFTs, three-times increase in the driving current, and two-times higher stability of the output driving voltage.

2. A simulation model

The 3D DD equations which consist of the electron–hole current continuity equations and Poisson equation, were solved numerically. The Shockley–Read–Hall model was employed to describe carrier emission and absorption processes at the grain boundary. The trap model at grain boundary is included on the right hand side of the Poisson equation to simulate the effect of polysilicon grain boundary:

$$\nabla^2\phi = -\frac{q}{\varepsilon}\left\{p - n + N_D - N_A + \sum_{E_t}(N_{\rm Dt} - n_{\rm Dt}) - \sum_{E_t}(N_{\rm At} - p_{\rm At}) + \sum_{E_t} p_t - \sum_{E_t} n_t\right\}, \quad (1)$$

where ϕ is the electrostatic potential, n is the electron density, ε is the semiconductor permittivity, p is the hole density, N_A is the acceptor doping concentration, and N_D is the donor-doping concentration. $N_{\rm Dt}$ is the donor trap concentration, $n_{\rm Dt}$ is the electron concentration of the donor trap level, $N_{\rm At}$ is the acceptor trap concentration, $p_{\rm At}$ is the hole concentration of the acceptor trap level, p_t is the hole concentration of the neutral hole trap level, and n_t is the electron concentration of the neutral electron trap level. E_t in each summation of (1) represents the energy levels of the carrier trap. The trapped electron and hole charges are given by [11]

$$\sum_{E_t}(N_{\rm Dt} - n_{\rm Dt}) + \sum_{E_t} p_t \quad (2)$$

and

$$\sum_{E_t}(N_{\rm At} - p_{\rm At}) + \sum_{E_t} n_t. \quad (3)$$

The trap concentration is a function of energy (E) and exhibits a Gaussian distribution, and the charges at the grain boundary are calculated by integrating over the energy range of occupied traps. The Poisson equation was solved self-consistently in the 3D DD model [12–15]. We calibrate the calculated results with respect to measured data taken from a fabricated 5/5/0.2 μm (width W/length L/oxide thickness) n-type polysilicon TFT, shown in figure 1. From the calibration, a 2×10^{13} cm^{-2} acceptor-liked trap surface concentration ($N_{\rm TA}$) and a 0.15 eV barrier height (E_B) of trap were extracted and used in our following study. These parameters are extracted by comparing the simulation results with measured data. For the conduction mechanisms, such as band-to-band tunneling, the low-field mobility model and saturation velocity are calibrated with respect to off-state, on-state linear and on-state saturation regions, respectively.

Table 1. The used parameters in the 3D device simulation.

Parameters	Values (nm)	Parameters	Values
Gate length	300	Work function	4.55 eV
Poly-Si thickness	30	Channel doping	1×10^{16} cm^{-3}
Channel width	300	LDD doping	2.5×10^{18} cm^{-3}
Oxide thickness	15	S/D doping	2.5×10^{19} cm^{-3}

3. Results and discussion

Two different TFT devices with 300 nm SG and GAA TFTs are investigated; a GAA TFT structure is shown in figure 2(*a*). The device parameters used are shown in table 1 [16]. Because

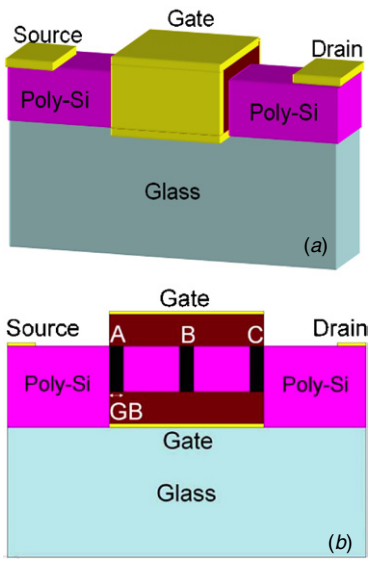

Figure 2. (*a*) A schematic plot of the GAA polysilicon TFT. The device is with a square-shaped-surrounding gate. (*b*) Single grain boundary occurs at the positions of A, B and C.

the size of GB used is 300 nm, only one GB was assumed to exist in the channel and is perpendicular to the channel length. The position of GB was assumed to occur at three different locations, as depicted in figure 2(*b*). To explore the potential advantages of GAA ploysilicon TFTs, we compare our calculated results with the data of SG ploysilicon TFTs. The threshold voltage for these two devices is adjusted with varying channel doping and gate material. The extracted barrier height (E_B) and the acceptor-liked trap surface density (N_{TA}) at the grain boundary were used for GAA and SG structures. The doping concentration (N_A) at the channel is calculated with [9]

$$E_B = \frac{q^2 N_A}{8\varepsilon}\left(\frac{N_{TA}}{N_A}\right)^2, \tag{4}$$

where ε is the semiconductor permittivity. Therefore by keeping E_B at constant, N_A is proportional to $(N_{TA})^2$. By varying the concentration of the doping profile and increasing the gate work function, a reasonable $V_{th} = 0.62$ V can be obtained and was used for both structures.

Characteristics of I_D–V_D and I_D–V_G for devices without GBs are presented in figure 3. The off-state current, shown in figure 3(*b*), is suppressed with the 300 nm GAA ploysilicon TFT by using a LDD doping profile close to the SG. The on-state current of the 300 nm GAA ploysilicon TFT is about three times larger than that of the SG, so we expect that the 300 nm GAA ploysilicon TFT can have a larger driving capability and yield a higher luminescence output.

The effect of a single GB on parameters of the short channel effect for GAA and SG devices is calculated and compared in table 2, respectively, where the definitions of DIBL and SS are described in figure 3(*b*). The *V*th is determined from a current criterion that $I_D = 10^{-8}\,(W/L)$ (A) and $D\overline{V}_{th}$ is the normalized difference of threshold voltages for the device with and without GB by the threshold voltage of the device without GB. Comparison shows that GAA polysilicon TFT exhibits good device characteristics compared with the results of SG one. It is observed that the worst case of V_{th} variation on GAA could be reduced from 15% to 5.5% when the GAA structure is considered.

$D\overline{V}_{th}$ versus the position of single GB, calculated with respect to different sizes of single GB, is shown in figure 4. When the drain and source sides have GB, the variation of V_{th} becomes significant. $D\overline{V}_{th}$ can be reduced when the size of GB is decreased from 15 nm to 3 nm. The effect of the GB is independent of the position when the size is relatively small compared with the channel length.

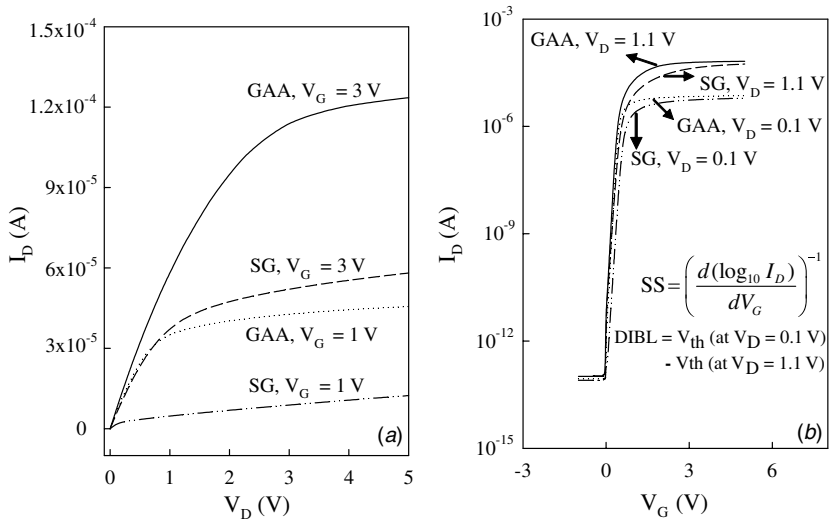

Figure 3. The simulated 300 nm polysilicon (*a*) I_D–V_D and (*b*) I_D–V_G characteristics in GAA and SG devices without GB, where the drain-induced barrier lowing (DIBL) and the subthreshold swing (SS) are computed.

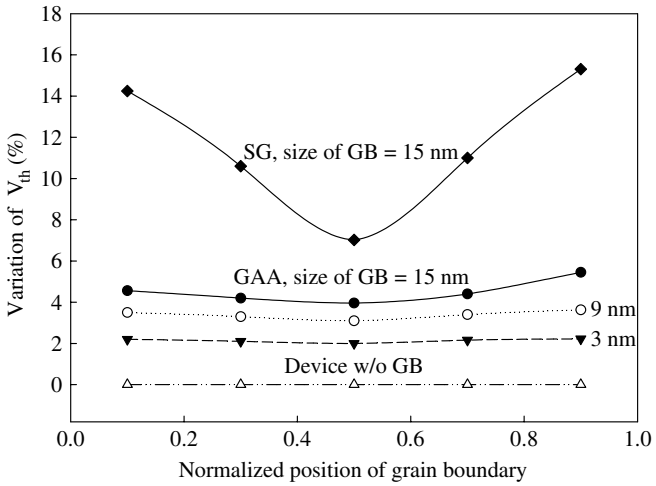

Figure 4. Effect of the GB position on V_{th} variation of the 300 nm GAA polysilicon TFTs. Suppression of variation is observed when the size of GB is reduced from 15 nm to 0 nm (i.e., device w/o GB).

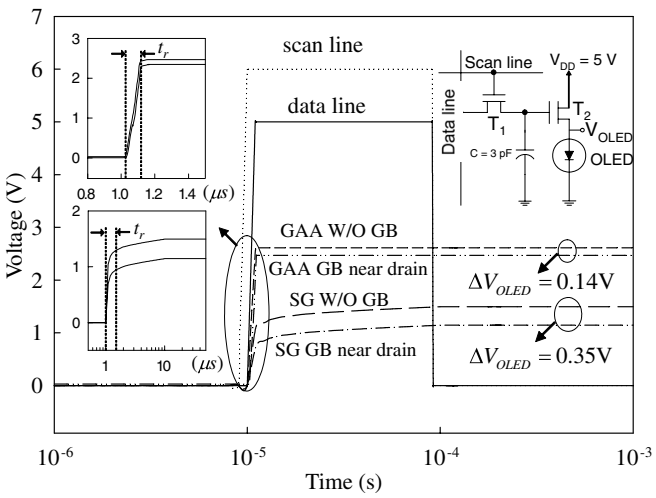

Figure 5. Circuit behavior of a 2T1C active matrix driver. As shown in the inset, T_1 is for switching and T_2 is for driving. The GAA circuit exhibits short delay time and stable current.

Currently, the well-established SPICE model of GAA polysilicon TFTs is not available for circuit simulation. Therefore, based on our recent work [17, 18], we develop a circuit-device coupled mixed-mode simulation technique to explore the circuit behavior. The aforementioned device equations are solved simultaneously with circuit equations of a 2T1C active-matrix driver, shown in the inset of figure 5. The characteristics of OLED are taken from the measured data [10, 19]. Clearly, the left inset shows that the delay time of the GAA circuit is about 0.12 μs which is only one ninth of the SG circuit. This property may benefit the application of a high-resolution display panel. Usually GB appearing on the drain side is the worst situation for devices, where the GAA circuit still has an effect to yield higher driving current than that of SG one without GB. The 2T1C circuit with GAA polysilicon TFTs can sustain stable currents. We believe similar results can occur for a more complicated active matrix circuit, such a 4T2C circuit using GAA polysilicon TFTs. Figure 6 shows

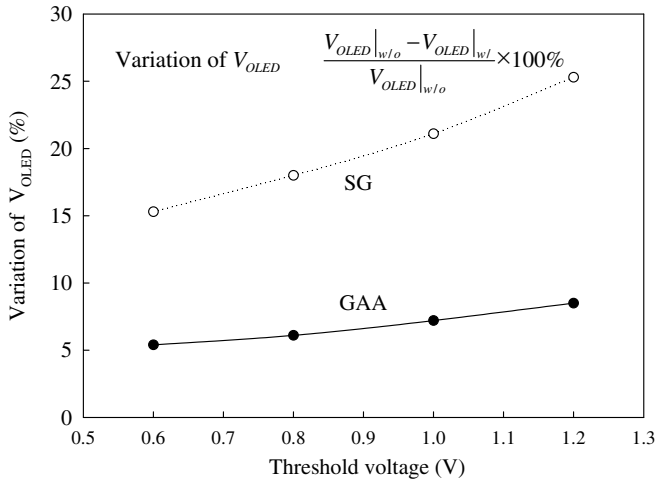

Figure 6. Variation of V_{OLED} versus V_{th}. A higher V_{th} implies a serious variation of OLED voltage due to heavy channel doping.

Table 2. Effects of the GB position on the device characteristics for the 300 nm GAA polysilicon tft, where the size of single GB is 15 nm. I_{on} and I_{off} are the on-state current and off-state current.

	$D\overline{V}_{th}$	I_{on}/I_{off}	DIBL (V)	SS (mv dec^{-1})
		GAA polysilicon TFT		
w/o GB	–	6×10^7	0.02	91
GB at A	4.56%	5.7×10^7	0.042	105
GB at B	3.96%	5.9×10^7	0.031	101
GB at C	5.45%	5.6×10^7	0.047	107
		SG polysilicon TFT		
w/o GB	–	2×10^7	0.04	101
GB at A	14.25%	1.2×10^7	0.08	139
GB at B	7.02%	1×10^7	0.06	134
GB at C	15.31%	1.3×10^7	0.09	144

variation of V_{OLED} with respect to V_{th}. High channel doping not only increases V_{th} but also trap concentration of single GB. The latter one results in a serious variation of V_{OLED} for the SG circuit. The GAA circuit yields more stable driving capability. We note that this approach can be applied to estimate the characteristics of driving circuits with more transistors.

4. Conclusions

In summary, we have explored characteristics of GAA polysilicon TFTs and behavior of the 2T1C active matrix circuit. Effects of the position and trap concentration of single GB on electrical characteristics of the device and circuit have been examined using the circuit–device coupled mixed-mode technique. The variation on the threshold voltage and short channel effect near the source and drain sides was studied. It could be suppressed by reducing the GB size which also eliminates the effect of the GB position. Submicron GAA polysilicon TFTs possess a higher on/off current ratio, and smaller SS and DIBL, and exhibits more stable driving capability, compared with the results of SG polysilicon TFTs.

Acknowledgments

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