K-Band CMOS Sub-Harmonic Resistive Mixer With a Miniature Marchand Balun on Lossy Silicon Substrate

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***Abstract*—A K-band sub-harmonically pumped resistive mixer is demonstrated using standard 0.13 μm CMOS technology. A miniature Marchand Balun is integrated with the resistive mixer to generate equal amplitude and out-of-phase signals for mixer's local oscillation (LO) port directly on the lossy silicon substrate. The sub-harmonic resistive mixer with the integrated Marchand balun has conversion loss of 11–12 dB at $f_{\rm IF}$ = 100 MHz and $P_{\rm LO}$ = 7 dBm for RF frequencies from 18 to 26 GHz. The LO–RF and LO–IF isolations are approximately 30 and 33 dB, respectively.**

***Index Terms*—Marchand balun, monolithic microwave integrated circuit (MMIC), sub-harmonically pumped resistive mixer (SPRM).**

I. Introduction

FOR a high-speed communication system, the mixer plays an important role for the frequency conversion. To alleviate the burden of designing a local oscillator at high frequencies, the sub-harmonic mixer topology is proposed [1]. The sub-harmonic mixer prevents the self-mixing problem caused by the local oscillation–radio frequency (LO–RF) leakage by operating the LO frequency at half of the RF frequency. An active Gilbert mixer requires a high dc power consumption for the specific conversion gain and speed. Therefore, the passive mixer without dc power consumption becomes an attractive candidate for high frequency applications. However, most sub-harmonically pumped resistive mixers (SPRM) are implemented in III/V semiconductor technologies over the past years [2]–[6].

As the CMOS device continuously scales down to the deep sub-micrometer regime, the cut-off frequency, f_T, obviously already catches up with and even exceeds that of III/V technologies. More and more CMOS integrated circuits have been realized at microwave and millimeter-wave frequencies. For instance, the first CMOS drain-pumped resistive mixer was demonstrated at 30 to 40 GHz with a low conversion loss of 4.6 dB [7] and the resistive mixer using gate-pumped topology has high linearity performance from 26.5 to 30 GHz [8]. However, these are fabricated in the 90-nm silicon-on-substrate (SOI) CMOS technology, which can reduce the substrate loss and coupling at the cost of higher fabrication price. For a low cost requirement, a 9–31 GHz source-pumped resistive mixer is first demonstrated in 90-nm standard CMOS process [9].

In this work, a single balanced structure with gate-pumped topology is employed to achieve better isolation and higher linearity. The symmetry of the balanced structure renders the inherent ability of rejecting unwanted signals. Therefore, the single-to-differential component significantly affects all kinds of specifications, such as the LO–RF isolation and the minimum conversion loss. It is difficult to generate a pair of equal amplitude and opposite phase signals at high frequencies for the active baluns. Thus, the passive broadband Marchand balun is explored in this work. Most miniature Marchand baluns are designed on the semi-insulating, high-resistive substrate or ground shielding plane [10] in the past. In this letter, we report a SPRM with a Marchand balun directly on the lossy silicon substrate [11]. The implementation method is compatible with

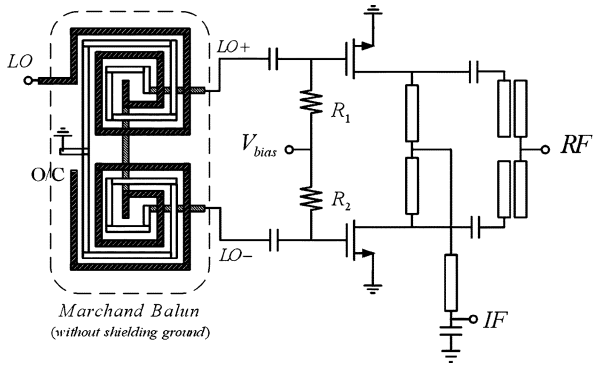

Fig. 1. Schematic of 0.13 μm CMOS SPRM with integrated Marchand balun.

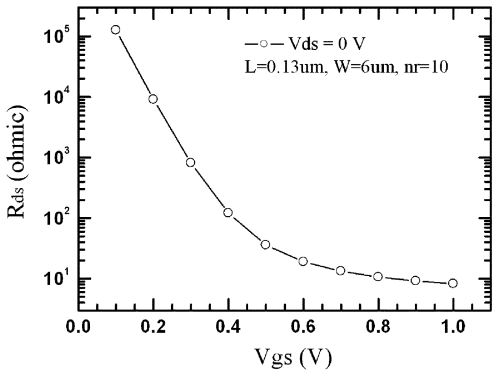

Fig. 2. Simulated $R_{\rm ds}$ as a function of Vgs at Vds = 0 V for the NMOS devices used in the SPRM.

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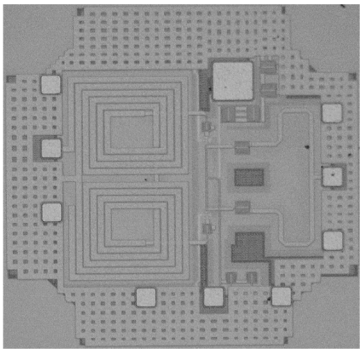

Fig. 3. Photograph of the 0.13 μm CMOS SPRM with the integrated Marchand balun.

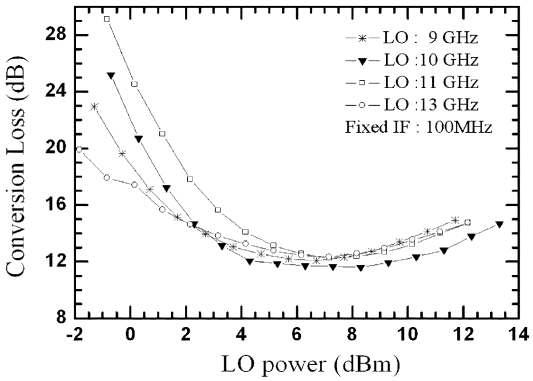

Fig. 4. Measured conversion loss versus LO power for the 0.13 μm CMOS SPRM with the integrated Marchand balun.

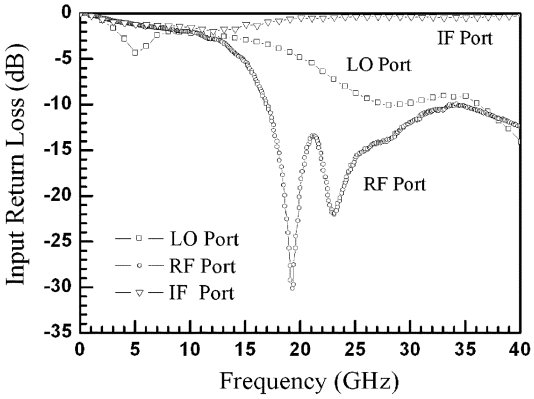

Fig. 5. Return loss of the 0.13 μm CMOS SPRM with the integrated Marchand balun.

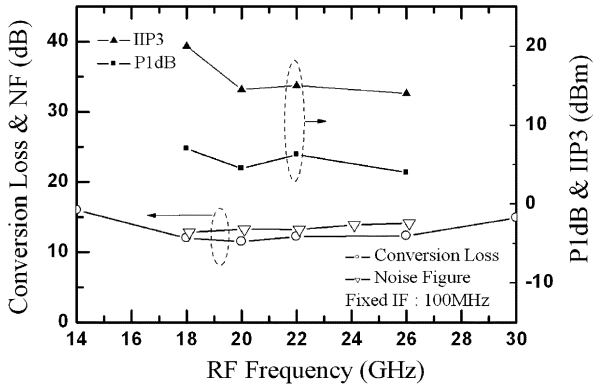

Fig. 6. Measured conversion loss, noise figure, IP_{1dB} and IIP_3 as a function of the RF frequency at the LO power of 7 dBm.

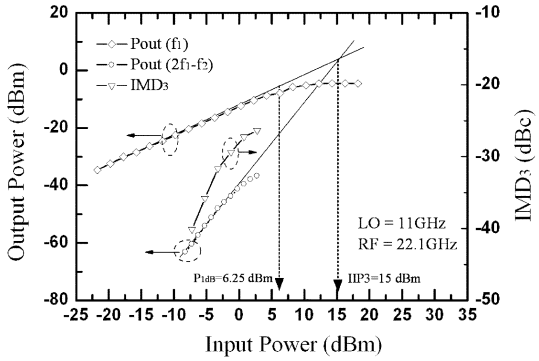

Fig. 7. Measured IP_{1dB}, IIP_3 and IMD_3 of the 0.13 μm CMOS SPRM with the integrated Marchand balun.

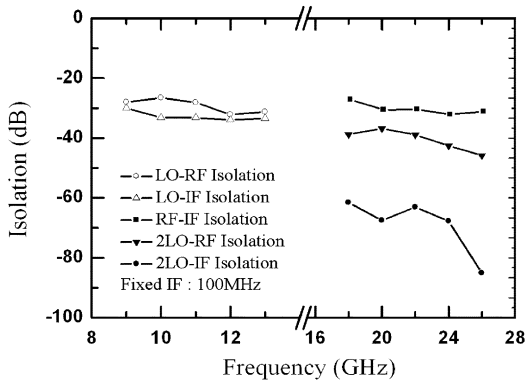

Fig. 8. Measured port-to-port isolations for the 0.13 μm CMOS SPRM with the integrated Marchand balun, IF= 100 MHz.

the standard silicon process and the Marchand balun has small size out of higher effective dielectric constant when compared with other published resistive mixers [12].

II. Circuit Design

Fig. 1 shows the schematic of the SPRM using the standard 1P8M 0.13 μm CMOS technology. The passive down-converter basically consists of two identical NMOS devices, a miniature marchand balun and RF/IF filters.

For the SPRM, the individual channel resistance is pumped by the LO signal in the anti-phase way. Because of the parallel anti-phase modulation, the net effective channel conductance of the SPRM appearing in the IF port is modulated at twice of the LO frequency. After mixing with the RF signal, the in-phase IF signal $(f_{\mathrm{RF}} - 2f_{\mathrm{LO}})$ is extracted from the IF low pass filter. To reduce conversion loss, the ratio of the channel conductance between the on-state and off-state must be increased by injecting more LO power and biasing the gate voltage near the threshold voltage. As shown in Fig. 2, the simulated channel resistance of the NMOS employed in this design is described as the function of the gate voltage. This NMOS has the minimum $R_{\mathrm{ds(total)}}$ of 8.2 Ω for the ten-finger device with unit gate width

TABLE I
COMPARISON OF THE PERFORMANCES FOR PUMPED RESISTIVE MIXERS

Tech.	*RF(GHz)*	*CL(dB)*	*LO(dBm)*	*LO-RF(dB)*	*LO-IF(dB)*	*IIP3*	*Size(mm²)*
0.2 um InGaP/InGaAs/GaAs PHEMT [2]	10-12	6.5	12 (Gate Pumping)	65	37	---	Hybrid
0.15 um AlGaAs/InGaAs/GaAs PHEMT [3]	40-45	10	7 (Gate Pumping)	---	---	---	Hybrid
0.15 um InGaAs PHEMT [4]	85-92	4.7 ~10	10 (Gate Pumping)	15~25	20~30	---	1.00x2.00
0.15 um InGaAs PHEMT [5]	27.5-28.5	11	13 (Gate Pumping)	35	30	---	1.00x2.00
90 nm CMOS (SOI) [7]	30-40	4.6	7.5 (Drain Pumping)	48	45	2	0.50x0.47
90 nm CMOS (SOI) [8]	26.5-30	10.3	0 (Gate Pumping)	24	22	12.7	0.50x0.32
90 nm Standard CMOS [9]	9-31	8~11	9.7 (Source Pumping)	17	22.5	3	0.90x1.00
	6.5~20	12~15	3.3 (Gate Pumping)	19	37.7	7	
0.13 um Standard CMOS This Work	18~26	11~12	4~8 (Gate Pumping)	30	33	14~20	0.68x0.60

of 6 μm. The conversion loss can be minimized as the ratio of $R_{\mathrm{ds(max)}}/R_{\mathrm{ds(min)}}$ increases. The best dc bias is approximately at 0.3 V for the efficient conversion.

The photograph of the sub-harmonically pumped resistive mixer is shown in Fig. 3. The die size is 0.68×0.6 mm^2. The layout is symmetrical to reduce the mismatch, and then better port-to-port isolation can be achieved. The realized size of the Marchand balun is 478 μm $\times$ 250 μm. The thickness, spacing and width of the spiral metal designed at 11 GHz are 3.4 μm, 2 μm, and 14 μm, respectively. Notice that wider metal widths can be employed here and thus the metal loss is somewhat small [11].

III. MEASUREMENT RESULT

Fig. 4 shows the conversion loss as a function of the LO power at the fixed IF frequency of 100 MHz. When the LO power exceeds 4 dBm, the conversion loss reaches the flat minimum region, and stays around 12 dB. The minimum conversion loss of 11.5 dB is under the condition of LO = 10 GHz and $P_{\mathrm{LO}} =$ 7 dBm. The measured return loss at the RF, LO and IF ports is represented in Fig. 5.

The conversion loss, noise figure, $\mathrm{IP_{1dB}}$ and $\mathrm{IIP_3}$ versus the RF frequency are shown in Fig. 6. For RF frequencies from 18 to 26 GHz, the conversion loss is less than 12.5 dB and varies within 0.5 dB at the LO power of 7 dBm. Basically, the noise figure is equal to the conversion loss of the passive component. In our experiment, the noise figure is about the same as the conversion loss as expected. The $\mathrm{IP_{1dB}}$ and $\mathrm{IIP_3}$ within the RF bandwidth are better than 4 and 14 dBm, respectively. Fig. 7 depicts the detailed $\mathrm{IP_{1dB}}$, $\mathrm{IIP_3}$, and $\mathrm{IMD_3}$ at $f_{\mathrm{RF}} = 22.1$ GHz.

The measured port-to-port isolations of the SPRM are shown in Fig. 8. The average LO-RF, LO-IF and RF-IF isolations are about -30 dB, -33 dB, and -30 dB, respectively.

The measured 2LO–RF and 2LO–IF isolations also exceed -40 dB and -60 dB. Table I summarizes the state-of-the-art results of the resistive mixers. When compared with the PHEMT process on the semi-insulating substrate, this work integrates the passive mixer with a Marchand balun on the standard CMOS process without any performance degradation, such as required LO pumping power and conversion loss.

IV. CONCLUSION

In this letter, a K-band SPRM is demonstrated in standard 0.13 μm CMOS technology. A Marchand balun directly on lossy silicon substrate is employed to generate a balanced LO pumping signal. From the measured results, the passive mixer has the conversion loss of 11–12 dB with 4–8 dBm LO pumping power for the RF bandwidth of 18–26 GHz. Thus, this SPRM with the miniature Marchand balun fabricated by the standard silicon process is suitable for the high-frequency applications.

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