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High-performance poly(3-hexylthiophene) transistors with thermally cured and photo-cured PVP gate dielectrics

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We have fabricated poly(3-hexylthiophene) organic field-effect transistors (P3HT-OFETs) with either high-temperature (200 °C) thermally cured PVP gate dielectrics or low-temperature (120 °C) photo-cured PVP gate dielectrics. We prepared the thermally cured PVP dielectric layer from a blend of poly(4-vinylphenol) (PVP) and poly(melamine-*co*-formaldehyde) (PMF); the photo-cured PVP dielectric formulation contained an additional photo-acid generator (PAG), which allowed the temperature for the cross-linking reaction to be reduced. We examined the intrinsic dielectric properties (*e.g.*, the dielectric constant, the electrical insulating properties) and surface properties (*e.g.*, morphology, surface energy) of the formulations loaded with various amounts of PAG (from 0 to 2.4 wt%). The P3HT-OFETs with the thermally cured PVP gate dielectrics exhibited an excellent carrier mobility of *ca.* 0.1 $cm^2 V^{-1} s^{-1}$, a sub-threshold swing of 2.0 V $decade^{-1}$, and an on/off ratio of 1.2×10^4. For comparison, the P3HT-OFET devices with the photo-cured PVP gate dielectrics also exhibited good electrical characteristics, including carrier mobilities as high as 0.06 $cm^2 V^{-1} s^{-1}$, sub-threshold swings as low as 1.4 V $decade^{-1}$, and on/off ratios as large as 3.0×10^4. To take advantage of the photo-cured PVP films, we also fabricated OFETs on a flexible, cheap ITO/PET substrate.

Introduction

Organic field-effect transistors (OFETs) are of great interest because of their potential use in such applications as radio-frequency identification tags, flexible displays, and smart cards.[1–4] During the past decade, much effort has been exerted on research into high-mobility, stable organic semiconductors and robust polymer dielectrics exhibiting uniform surfaces and low leakage current densities. Among the polymer dielectrics reported to date,[5,6] one of the most useful is cross-linked poly(vinylphenol) (PVP), which has good dielectric properties and a high carrier mobility of 3–5 $cm^2 V^{-1} s^{-1}$ when using pentacene as the semiconductor.[7,8] The cross-linked PVP gate dielectric can be obtained by mixing PVP with a cross-linking agent, poly(melamine-*co*-formaldehyde) (PMF), spin-coating the mixture from solution, and then curing at the temperature of at least 180 °C. Although the resulting cross-linked PVP material possesses excellent chemical resistance and good dielectric performance, the high temperatures required for the thermal cross-linking reaction make this process unsuitable for fabrication on common low-cost plastic substrates (usually T_g < 150 °C).

To solve this problem, Lee *et al.*[9] recently reported a photo-cured PVP gate insulator for the fabrication of OFETs *via* a low-temperature curing process. The photo-curing system comprised PVP as the resin, epoxy resin (triglycidyl ether) as the cross-linker, and triphenylsulfonium triflate as the photo-acid generator (PAG). After exposure to UV irradiation, the PAG decomposed to form a strong acid and the resulting film could be cross-linked at a temperature of 100 °C for *ca.* 30 min *via* acid-catalyzed ring opening polymerization of the epoxy groups. Lee *et al.*[10] also demonstrated a photo-cured PVP formed from PVP as the resin, tetraacetoxymethylbenzene as the cross-linker, and triazine as the PAG. In the devices fabricated by the two research groups, pentacene was used as the semiconductor and the resulting OFETs exhibited high mobilities (>0.5 $cm^2 V^{-1} s^{-1}$) and on/off current ratios (>10^7). Although these two initial studies demonstrated the potential application of PAG-assisted photo-cured PVP in OFETs, the dielectric properties (*e.g.*, the value of *k*, the electrical insulating properties) and the surface properties (*e.g.*, morphology, surface energy) of the resulting PVP films have not been explored as a function of the PAG content. Moreover, to fully enjoy the advantages of OFETs, namely their low-cost for large-area electronics, it will be necessary to develop OFET devices with polymeric semiconductors and polymeric dielectrics that can be processed using solution methods and cured at low temperatures.

In this study, we prepared OFET devices with regioregular poly(3-hexylthiophene) (rr-P3HT) as the semiconductor and either thermally cured PVP or photo-cured PVP as the gate insulator. To investigate the effects of the PAG content, we prepared dielectric films by varying the amount of PAG in the formulations from 0 to 2.4 wt% and then determined their current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) characteristics. Because surface treatment of gate dielectrics with self-assembled monolayers (SAMs) can dramatically affect the performance of OFETs, we examined the surface morphologies and surface energies of the resulting cross-linked PVPs with and without treatment with SAMs. Finally, to take advantage of the

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PAG-assisted photo-cured PVP films, we fabricated P3HT-OFETs on flexible indium tin oxide (ITO)-coated polyethylene terephthalate (PET) substrates and investigated their electrical performance.

Experimental section

Materials

A heavily doped N-type low-resistance wafer and a flexible ITO/PET sample were used as substrates and common gate electrodes. PVP (M_w = 20 000), PMF (M_w = 511), and octyltrichlorosilane (OTS) were obtained commercially from Aldrich. {4-[(2-hydroxyltetradecyl)oxy]phenyl}phenyliodonium hexafluoroantimonate (Sartomer, CD1012) was used as the PAG. Regioregular P3HT was purchased from Aldrich and purified through Soxhlet extractions with hexane and CH_2Cl_2 to remove low-molecular-weight chains. The chemical structures of the materials used for the gate dielectrics are presented in Fig. 1.

Film fabrication and characterization

The weight percentage ratios of PVP, PMF, and the PAG in the photo-cured formulations (blends) in this study were 8 : 4 : 0 (PVP0), 8 : 4 : 0.5 (PVP05), 8 : 4 : 1.0 (PVP10), and 8 : 4 : 2.4 (PVP24) in propylene glycol methyl ether acetate (PGMEA). For the formulation lacking the PAG, PVP0, the resulting film was cured at 200 °C for 1 h. The other formulations (PVP05, PVP10, and PVP24) were spin-coated and then exposed to 365 nm UV irradiation (9.6 mW cm^{-2}) for 1 min to catalyze the cross-linking reaction; these films were then hardened through baking at 120 °C for an additional 30 min. Prior to spin-coating of the organic semiconductor, the surfaces of the PVP films were treated with OTS to form SAMs to improve the performance of the OFET devices. OTS treatment was performed through the deposition of OTS vapor in a chamber.

The thicknesses of the corresponding PVP films were determined using cross-sectional scanning electron microscopy (SEM). The morphologies of all of the cross-linked PVP films were evaluated using atomic force microscopy (AFM; Nanoscope IIIa, Digital Instruments). All of the root-mean-square (rms) surface roughnesses are reported herein over an area of 25 μm^2. The surface energies of the cross-linked PVP films were determined from contact angle measurements (FACE contact-angle meter, Kyowa Kaimenkagaku Co.) using distilled water and CH_2I_2 as the probe liquids.

Device fabrication and electrical measurements

The OFETs were fabricated with the thermally cured and photo-cured PVP as gate dielectrics; the source and drain electrodes having channel widths and lengths of 1000 and 10 μm, respectively, were prepared using a photolithography/Pt (20 nm) deposition/lift-off (acetone) process. Fig. 2 provides a schematic representation of the bottom-gate P3HT-OFETs fabricated in this study.

To characterize the leakage currents and capacitances of the cross-linked PVP films, we prepared a metal–insulator–metal (MIM) capacitor structure by sandwiching the cross-linked PVP materials between the heavily doped N-type wafer and the Pt electrode (dot area = 0.0010 cm^2).

The capacitances were measured using a capacitance analyzer (590 CV, Keithley) at 100 kHz. All I–V measurements for our OFETs and MIM devices were performed using a semiconductor parameter analyzer (4156C, Agilent) at room temperature under ambient conditions.

Results and discussion

We prepared the high-temperature thermally cured PVP0 film and low-temperature photo-cured PVP05, PVP10, and PVP24 films by spin-coating a solution of the composite blends using the procedures described in the Experimental section. Each of these films exhibited good chemical resistance to the bases typically found in positive photoresist developers; thus, the photo-cured PVP samples prepared in this study were suitable for use in photolithography processes. Thus, we defined the region of the electrodes on the OFET and MIM devices by using a photolithography/electrode-deposition/lift-off process (rather than by using a traditional vacuum-deposition process through a shadow

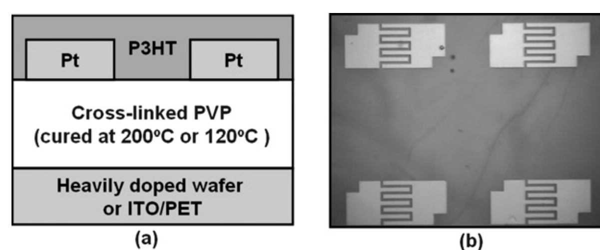

Fig. 2 (a) Device structure of the bottom-gate, bottom-contact configuration employed in this study. (b) Optical micrograph of finger electrodes having a channel length of 1000 μm and a width of 10 μm.

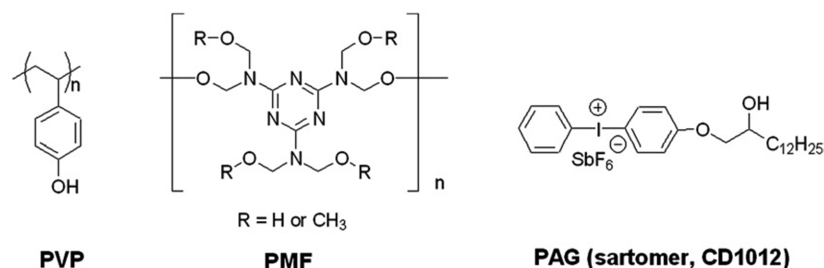

Fig. 1 Chemical structures of the materials used to prepare the cross-linked PVP gate insulators.

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mask), leading to an accurately patterned electrode and an intact surface of the underlying cross-linked PVP films. Moreover, these films also exhibited good chemical resistance toward the organic solvents, such as toluene and chlorobenzene, that are commonly used as solvents for the preparation of organic semiconductors; thus, we suspected that these films would be good candidates for use as insulators for fabricating bottom-gate OFET devices.

We performed quantitative leakage current and capacitance measurements to evaluate the dielectric characteristics of the MIM devices with the cross-linked PVP films. In addition, we used SEM to measure the thicknesses of the cross-linked PVP films. Fig. 3a reveals that the dielectric films PVP0, PVP05, PVP10, and PVP24 exhibited leakage currents ranging from 10^{-5} to 10^{-6} A cm^{-2} at 40 V. The leakage current of PVP0 (3.6×10^{-6} A cm^{-2}) is consistent with that reported by Halik *et al.*[8] All of the photo-cured PVP films, except for PVP05, exhibited current densities lower than that of PVP0, presumably because the PVP10 (530 nm) and PVP24 (580 nm) films were thicker than the PVP0 film (445 nm). The thickness of these PVP films increased upon increasing the solid content in the PVP formulations. Although the thickness of the PVP05 film (505 nm) was greater than that of the PVP0 film, its leakage current density was slightly higher, indicating that a PVP05 film was only partially cross-linked because of an insufficient PAG loading in the composition blend. The low-temperature photo-cured PVP films (PVP05, PVP10, and PVP24) all exhibited insulating properties as good as those of the high-temperature thermally cured PVP0 film, suggesting that they would be good candidates for use as solution-processed gate dielectrics for OFETs, especially on flexible, low-cost, plastic substrates.

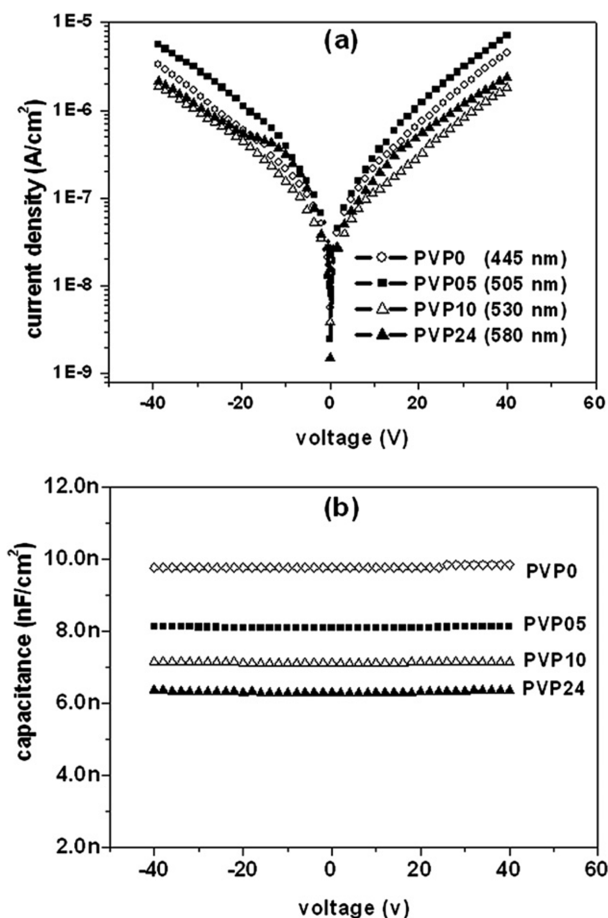

Fig. 3 Plots of (a) current density and (b) capacitance as a function of the applied voltage for the cross-linked PVP films.

Fig. 3b reveals that the *C–V* characteristics of these cross-linked PVP0, PVP05, PVP10, and PVP24 films were 9.7, 8.1, 7.2, and 6.3 nF cm^{-2}, respectively. According to the capacitance and the thickness data, we estimated the dielectric constants (k) of the PVP0, PVP05, PVP10, and PVP24 films to be 4.9, 4.6, 4.3, and 4.1, respectively (Table 1). Thus, the values of k of these films decreased from 4.9 to 4.1 upon increasing the content of PAG from 0 to 2.4 wt%.

We determined the surface energies of the dielectrics using distilled water and CH_2I_2 as probe liquids and employing the geometric mean equation (1)[11]

$$(1 + \cos\theta)\gamma_{\mathrm{pl}} = 2(\gamma_{\mathrm{s}}^{\mathrm{d}}\gamma_{\mathrm{pl}}^{\mathrm{d}})^{1/2} + 2(\gamma_{\mathrm{s}}^{\mathrm{p}}\gamma_{\mathrm{pl}}^{\mathrm{p}})^{1/2} \quad (1)$$

where γ_{s} and γ_{pl} are the surface energies of the sample and the probe liquid, respectively, and the superscripts d and p are the dispersion and polar components of the surface energy, respectively. Table 1 summarizes the dielectric constants and surface properties of the cross-linked PVP films. The surface energy of the high-temperature thermally cured PVP0 film was 53 mJ m^{-2}; those of the low-temperature photo-cured PVP05, PVP10, and PVP24 films ranged from 49 to 43 mJ m^{-2}. Thus, the surface energy decreased from 53 to 43 mJ m^{-2} upon increasing the PAG content from 0 to 2.4 wt%. The low surface energies of the photo-cured PVP films are most likely due to the presence of residues arising from PAG, the structure of which contains a long alkyl side chain. When we treated the surfaces with OTS to form SAMs, the water contact angle increased from *ca.* 60° to *ca.* 110°, indicating that the hydrophilic surfaces of the original PVP films had been transformed into hydrophobic surfaces. It is interesting to note that all of our OTS-treated PVP films exhibited the same surface energy (*ca.* 22 mJ m^{-2}), despite the fact that the pristine PVP films were prepared using different curing processes and different PAG loadings. It is well known that the growth of organic semiconductor layers on gate dielectrics possessing different surface energies will result in a change in the morphology of the semiconductor film.[12,13] Hence, to investigate the advantages of employing the thermally and photo-cured PVP films and the effects of the PAG residues within them, we fabricated OFET devices using only the OTS-treated surfaces because their surface energies were identical.

The surface roughness of gate insulators is another important factor affecting the performance of OFETs. We used tapping-mode AFM to determine the surface roughness of each film (Fig. 4, Table 1). Fig. 4a and 4b reveal that no aggregates had formed on the PVP0 and PVP24 surfaces; the rms values of the PVP films on the silicon wafer were 0.58 and 0.28 nm, respectively, very close to that of the SiO_2 surface on the Si substrate. The other two photo-cured PVP films also exhibited small rms values, revealing the good uniformity of all of the PVP–PMF–PAG blends. After OTS treatment (Fig. 4c and 4d), we observed uniform aggregates on the PVP0 surface; the rms value increased from 0.58 to 0.66 nm. The other three photo-cured PVP films also

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Table 1 Dielectric and surface properties of the cross-linked PVP films

			Surface properties of cross-linked PVP				Surface properties of cross-linked PVP with OTS treatment			
				Contact angle				Contact angle		
Gate dielectric	PVP : PMF : PAG (wt%)	*k*	Surface rms/nm	Water/°	CH_2I_2/°	Surface energy γ_s[a]/mJ m^{-2}	Surface rms/nm	Water/°	CH_2I_2/°	Surface energy γ_s[a]/mJ m^{-2}
PVP0	8 : 4 : 0	4.9	0.58	61.73	33.08	53.33	0.66	108.39	72.10	21.90
PVP05	8 : 4 : 0.5	4.6	0.28	68.58	36.11	49.05	1.19	108.66	71.18	22.36
PVP10	8 : 4 : 1.0	4.3	0.29	74.82	37.55	45.90	1.20	109.37	72.20	21.78
PVP24	8 : 4 : 2.4	4.1	0.29	80.44	38.59	43.53	1.20	110.96	72.76	21.41

[a] γ_s: solid surface free energy.

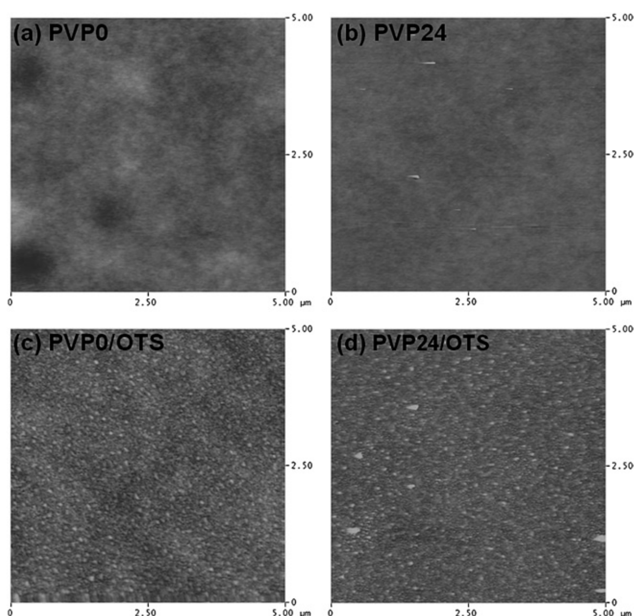

Fig. 4 Tapping-mode AFM images of (a, b) the highly smoothly surfaces of PVP0 and PVP24 and (c, d) the surfaces of PVP0/OTS and PVP24/OTS exhibiting a few aggregates. All images represent a scan area of 5 × 5 μm^2.

exhibited uniform aggregates; their rms values increased from 0.28 to 1.20 nm—slightly higher than that of PVP0, but still sufficiently low to behave as smooth surfaces for growing semiconductor layers.

We fabricated P3HT-OFET devices by spin-coating P3HT (3 mg mL^{-1} in toluene, 500 rpm, 60 s) as the semiconductor upon the OTS-treated PVP substrates. After thermally annealing at 120 °C for 30 min in an oven, we obtained bottom-gate, bottom-contact OFET devices with each of the four types of cross-linked PVP gate dielectrics. Table 2 summarizes the mobilities, threshold voltages, sub-threshold swings, and on/off current ratios of these devices. We determined the transfer characteristics by operating the four devices at V_{ds} of −40 V and V_{gs} ranging from +40 to −40 V (Fig. 5). We determined the carrier mobility *u* and the threshold voltage V_{th} by using the following equation (2):

$$\sqrt{I_{D,SAT}} = \sqrt{\frac{W\mu C_{ox}}{2L}}(V_G - V_{th}) \quad (2)$$

Table 2 Electrical characteristics of P3HT-OFETs with cross-linked PVP gate dielectrics

	Electrical parameters				
Gate dielectric	*C*/nF cm^{-2}	*u*/cm^2 V^{-1} s^{-1}	On/off ratio	Ss/V dec^{-1}	V_{th}/V
PVP0	9.7	0.097	1.2 × 10^4	2.0	−14.8
PVP05	8.1	0.029	6.9 × 10^3	3.9	−2.6
PVP10	8.3	0.050	2.5 × 10^4	2.0	−5.1
PVP24	6.3	0.060	3.5 × 10^4	1.4	−2.9

where $I_{D,SAT}$ is the saturated drain current, C_{ox} is the gate capacitance per unit area, *W* and *L* are the conducting channel width and length, respectively, V_{th} is the threshold voltage, and V_G is the gate applied voltage. We extracted the mobilities from the slopes of the linear plots of the square root of the drain current *versus* the gate voltage.

For the device with the OTS-treated PVP0 gate insulator, the mobility in the saturation region was 0.097 cm^2 V^{-1} s^{-1}, the threshold voltage was −14.8 V, the sub-threshold swing was 2.0 V $decade^{-1}$, and the on/off ratio was 1.2 × 10^4. Thus, the performance of this device was comparable with that of reported P3HT-OFETs possessing an HMDS-treated SiO_2 gate dielectric.[14] To the best of our knowledge, this is the first example of a P3HT-OFET with a PVP gate dielectric that exhibits a mobility reaching almost 0.1 cm^2 V^{-1} s^{-1} as well as an on/off ratio greater than 10^4. Among the thermally cured PVP gate dielectrics reported previously,[15–17] in which HMDS or octadecyltrichlorosilane was used as the SAM and deposited by solution process, the mobilities of the P3HT-OFETs usually ranged from 10^{-3} to 10^{-2} cm^2 V^{-1} s^{-1} with on/off ratios of 10^2–10^3.

For our devices with the OTS-treated PVP10 and PVP24 gate dielectrics, the mobilities (*ca.* 0.06 cm^2 V^{-1} s^{-1}) were somewhat lower than that of the PVP0-containing device, but the on/off ratios (2.5 × 10^4 and 3.5 × 10^4, respectively) were better; the sub-threshold swings of these OFETs were 2.0 and 1.4 V $decade^{-1}$, respectively. Again, these systems are the first examples of high-performance P3HT devices based on PVP dielectrics prepared through a low-temperature curing process. The mobility of the PVP05 device was 0.029 cm^2 V^{-1} s^{-1} with an on/off ratio of 6.9 × 10^3; thus, its performance was inferior to those of the PVP0-, PVP10-, and PVP24-based devices. In addition, the sub-threshold swing of the OFET with the PVP05 gate dielectric was

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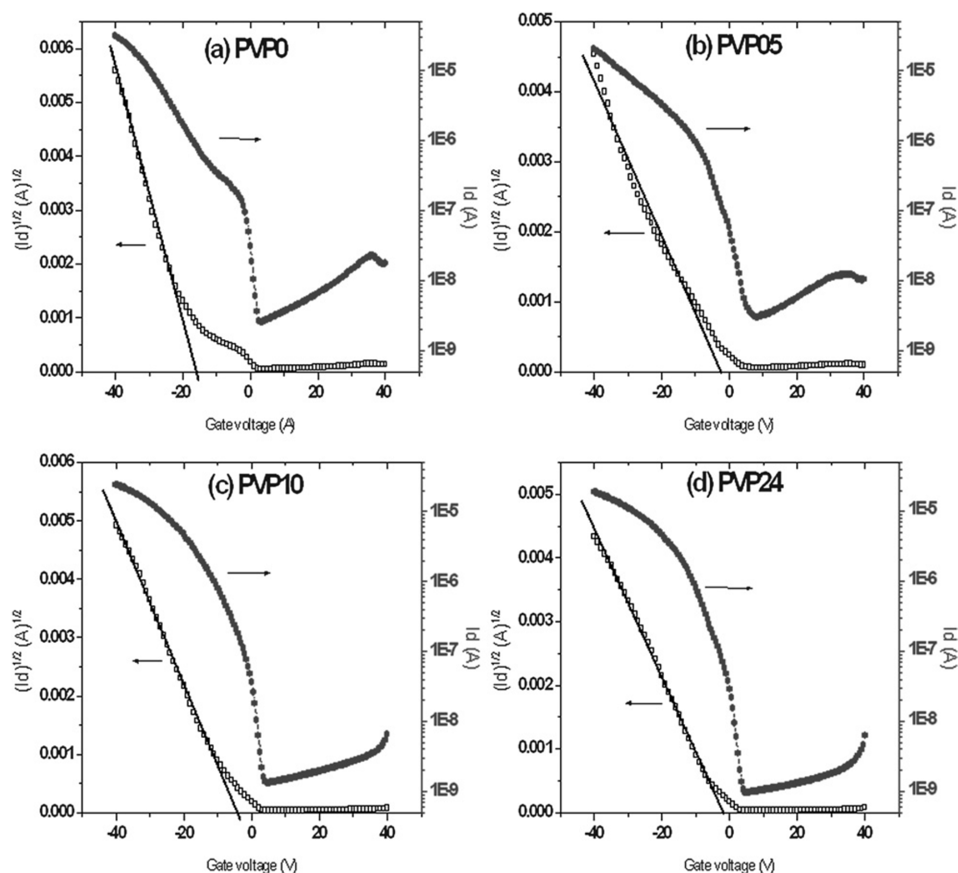

Fig. 5 Transfer characteristics of P3HT-OFETs with (a) PVP0, (b) PVP05, (c) PVP10, and (d) PVP24 as gate dielectrics.

twice as large as those of the other three gate dielectrics. The relatively low mobility and low on/off ratio of the PVP05-based device might be due to the insufficient PAG loading in its composition blend, thereby leading to a partially cross-linked film that was slightly soluble at the polymer surface, causing the polymer to swell when immersed in the semiconductor solution.

To take the advantage of the excellent properties of the low-temperature photo-cured PVP films, we employed PET (a flexible plastic) and ITO as the bottom-gate substrate. To obtain a thicker gate dielectric layer on this plastic substrate, we spin-coated the PVP24 solution at 800 rpm for 40 s, exposed it to UV irradiation for 1 min, and then cured the sample at 120 °C for 30 min. The thickness of the gate dielectric was 635 nm; the roughness of its OTS-treated surface was 2.17 nm. Fig. 6 displays the output and transfer characteristics of the P3HT-OFET prepared from the PVP24 gate dielectric on the ITO/PET substrate. The mobility and threshold voltage of this device were 0.046 $cm^2 V^{-1} s^{-1}$ and -19.7 V, respectively, with an on/off ratio of 4.9×10^3. The sub-threshold swing was 3.0 V $decade^{-1}$. Although the performance of P3HT with the PVP24 gate

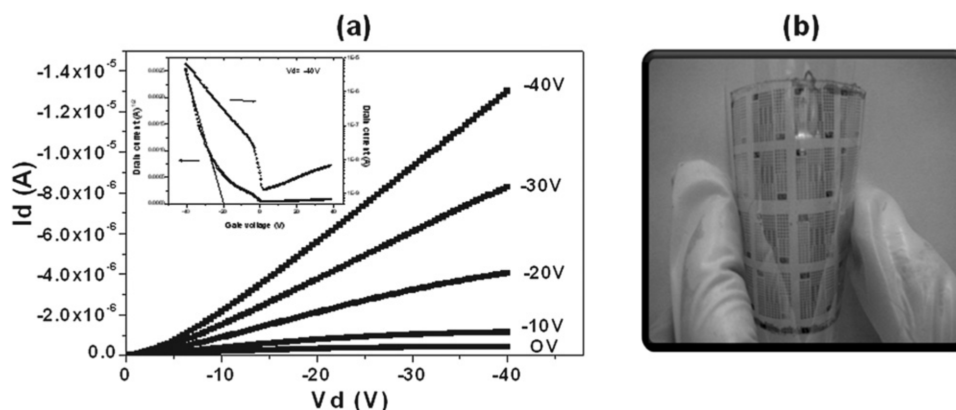

Fig. 6 (a) Output characteristics and transfer characteristics (inset) of the P3HT-OFET device with the PVP24 gate dielectric on an ITO/PET substrate. (b) Photograph of the OFET fabricated on the ITO/PET substrate.

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dielectric on the plastic substrate was not as good as that on the silicon wafer, this photo-cured PVP still has great potential for application in OFETs prepared on low-cost, flexible substrates. Further efforts to improve the film smoothness and optimize the other experimental parameters should lead to an increase in the device performance on such plastic substrates.

Conclusion

We have investigated the intrinsic dielectric and surface properties of thermally cured and photo-cured PVP films with various PAG loadings. MIM devices prepared with thermally cured (PVP0) and photo-cured (PVP05, PVP10, and PVP24) PVP films exhibited leakage currents ranging from 10^{-5} to 10^{-6} A cm^{-2} at 40 V. The value of k of these films decreased from 4.9 to 4.1 upon increasing the PAG content from 0 to 2.4 wt%. The surface energy of PVP0 was 53 mJ m^{-2}; those of the photo-cured PVP05, PVP10, and PVP24 ranged from 49 to 43 mJ m^{-2}. After OTS treatment, the four PVP films exhibited identical surface energies (*ca.* 22 mJ m^{-2}). From AFM images, we determined that all the PVP films possessed small rms values (<0.58 nm) that were very close to that of SiO_2 surfaces on Si substrates; after OTS treatment, however, we observed some aggregation and the rms values increased up to 1.2 nm. The P3HT-OFETs that we prepared from the thermally cured PVP gate dielectric and the three low-temperature photo-cured PVP gate dielectrics all exhibited good carrier mobilities (up to *ca.* 0.1 cm^2 V^{-1} s^{-1}) and on/off current ratios up to 3×10^4. We also fabricated OFETs from the photo-cured PVP films deposited onto a cheap plastic substrate (ITO/PET); the devices exhibited carrier mobilities of up to 0.046 cm^2 V^{-1} s^{-1}, sub-threshold swings of up to 3.0 V $decade^{-1}$, and on/off ratios of up to 4.9×10^3.

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