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Improved Electrical Properties of Gd_2O_3/GaAs Capacitor with Modified Wet-Chemical Clean and Sulfidization Procedures

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In this study we demonstrated improved electrical characteristics of Gd_2O_3 dielectric thin films on n-GaAs substrate by manipulating wet-chemical clean and $(NH_4)_2S$ passivation. With X-ray photoelectron spectroscopy analysis, the HCl-cleaned GaAs surface was characterized to possess oxide species mainly in the form of As_2O_x near the outmost surface and Ga_2O_x with elemental arsenic close to the interface. These undesirable components could be suppressed through rinsing in NH_4OH alkaline solution and then performing sulfidization at 80°C, resulting in alleviating the Fermi level pinning effect on Gd_2O_3/GaAs capacitor performance. Higher oxide capacitance and alleviated frequency dispersion at the accumulation/depletion regimes were achieved, accompanied by negligible charge trapping (<100 mV). Accordingly, gate leakage J_g was lowered to ca. 10^{-5} A/cm^2 at gate voltage $V_g = (V_{FB} + 1)$ V, which was comparable to the recently reported performance of HfO_2/GaAs structure with an ultrathin Si/Ge interfacial layer. We attributed the electrical improvements to the enhanced stabilization of high-*k*/sulfur-terminated GaAs interface due to abatement of native oxides and excess arsenic segregation.
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GaAs metal-oxide-semiconductor (MOS) devices with different high-*k* gate dielectrics have been of more interest in recent years. Examples of these include the well-known Gd_2O_3,[1] Al_2O_3,[2] TiO_2,[3] and Hf-based oxides.[4,5] The primary bottleneck of these high-*k*/GaAs structures in realizing practical devices is a large density of interfacial states, which causes significant Fermi-level pinning effects, e.g., low modulation of surface potential and other poor electrical properties. Carbon contamination, native oxides, and, in particular, arsenic element segregation are commonly detected species on the GaAs surface.[6] In other words, understanding the chemical bonding configuration at the dielectric/GaAs interface is of the utmost importance, and its quality also determines device performance because the GaAs surface is likely to debase during dielectric deposition and thermal anneal processing. Several groups have demonstrated promising capacitor and transistor characteristics by performing various surface-preparation techniques, mainly comprising three aspects of wet-chemical cleaning, interface passivation, and thermal treatment, respectively. Numerous acidic or basic wet solutions have been extensively studied; it was found that the amount of impurity contamination and residual components strongly depended on the entire cleaning procedures.[7-9] Prior to the deposition of gate dielectrics, the passivations of GaAs surface (the sulfide-based immersion,[10,11] the silicon/germanium interfacial layer,[12-14] and the coverage of lattice-matched dielectric thin film[15]) have also been reviewed in recent years. Additionally, thermal desorption in the high-vacuum system, especially for molecular beam epitaxy, is another widely used approach to clean III–V deposited surface.[16,17] In this work we modified the wet-chemical cleaning and sulfide passivation processes to improve the electrical performance of Gd_2O_3 dielectric thin film deposited on n-GaAs substrate. Low gate leakage, diminutive hysteresis, and reduced interface state density can be achieved in the fabricated Gd_2O_3/GaAs structures.

Experimental

MOS structures were fabricated on highly doped ($\sim 1 \times 10^{18}$ cm^{-3}) n-type GaAs substrates. A series of wet-chemical cleaning processes (WCPs) were applied and are listed in Table I. Both the HCl and NH_4OH aqueous solutions with the same diluted concentration (acid or alkaline/H_2O, 1:10) were used in GaAs surface clean. Subsequently, the samples were dipped into aqueous ammonium sulfide solution [$(NH_4)_2S$/deionized water, 1:100] at two different processing temperatures of room temperature and 80°C, respectively, with fixed immersion time of 5 min for studying the sulfur bonding states as well as the efficiency of oxide removal. After undergoing these WCPs, we measured the roughness variation of GaAs surface morphology within the scanning area of 1×1 μm^2 by atomic force microscopy (AFM). Meanwhile, we employed X-ray photoelectron spectroscopy (XPS) in which Al Kα ($h\nu = 1486.6$ eV) was used as an excitation source and the take-off angle was fixed at 60° in order to understand the surface chemistry. High surface-sensitive As $2p_{3/2}$ and Ga $2p_{3/2}$ core level spectra, after subtraction of the Shirley background, were analyzed by the least-squares fitting method; the contributed components comprised a Gaussian line shape convoluted with a Lorentzian broadening function. In addition, to examine the impact of WCPs on the properties of the resultant capacitor, we deposited the Gd_2O_3 thin film as gate dielectric using electron-beam evaporation with pure Gd_2O_3 ingot, followed by performing postdeposition annealing (PDA) at 500°C for 10 s in Ar/O_2 mixed ambient for further condensation. Most importantly, the distribution of $(Ga,As)_2O_x$ oxides and GaAs-related defects into the high-*k* dielectric after thermal processing was examined. A 600 Å thick layer of sputtered Pt was patterned as circular capacitor electrode via a specific shadow mask, while the back side ohmic contact was formed by E-beam evaporation of a In/Pt (300/300 Å) bilayer. The capacitance–voltage (*C-V*) curves and the gate leakage (*I-V*) characteristics for the fabricated Pt/Gd_2O_3/GaAs MOS structures were measured using an HP4284 LCR meter and a Keithley 4200 semiconductor analyzer system, respectively. The level of fast interface states was evaluated by frequency-dependent conductance method, while the capacitance-equivalent-thickness (CET) was determined by the value of accumulation capacitance (10 kHz) at gate voltage $V_g = 3$ V.

Results and Discussion

Figures 1 and 2 show the respective As $2p_{3/2}$ and Ga $2p_{3/2}$ photoemission spectra of the GaAs surface after four WCPs and all the deconvoluted peaks; the fitting results are summarized in Table I. It was seen in Fig. 1a, as compared to the others, that more As oxides as well as amorphous As preferred to accumulate on the GaAs surface, subject only to HCl acidic solution etching. The chlorine ion tends to attack the GaAs surface, forming soluble gallium chloride,[18] and the simultaneously produced As-rich overlayer can

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Table I. Chemical ratios of As $2p_{3/2}$ and Ga $2p_{3/2}$ spectra for the cleaned GaAs surface after different WCPs.

	As $2p_{3/2}$ and Ga $2p_{3/2}$				
	$As–As/As_{tot}$	As_2O_x/As_{tot}	Ga_2O_x/Ga_{tot}	$As–S/As_{tot}$	$Ga–S/Ga_{tot}$
HCl only	15.4%	45.6%	27.8%	—	—
HCl + sulfur (room temperature)	14.9%	34.8%	27.6%	5.4%	7.3%
HCl + NH_4OH + sulfur (room temperature)	12.8%	28.1%	23.5%	3.5%	11.7%
HCl + NH_4OH + sulfur (80°C)	12.3%	22.9%	23.2%	2.6%	12.5%

then be partly oxidized to form As_2O_3 and As_2O_5 species on the outmost surface. From the viewpoint of thermodynamics, Ga atoms are more easily oxidized because the Gibbs energy of the formation of Ga_2O_3 (ca. −999 kJ/mol) at room temperature is lower than that of As_2O_3 (ca. −576 kJ/mol).[19] However, our experimental observation is obviously contradictory to this prediction. This is because Gibbs energy is not the sole determining factor; the constituent distribution as well as the oxidized probability also play a big role in the real oxidation processing.[7] Thus, we suggest that excess As atoms possibly block the access of chlorine to underlying gallium atoms during HCl clean, which also act as a passivation layer to hinder the interfacial gallium oxidation. This result is similar to what was observed in previous studies in which GaAs substrate was cleaned by hydrofluoric acid.[20,21]

Subsequently, performing $(NH_4)_2S$ immersion at room temperature was found, as shown in Fig. 1b, to effectively diminish the oxidized As species; raising the temperature up to 80°C lessened them further. As reported, wet sulfide solution comprising $(NH_4)_2S$ or Na_2S agent are capable of suppressing these undesirable species on GaAs by forming sulfur-related chemical bonds, where the outer oxide is etched away and then reactive sulfur starts to create bonds with surface atoms.[22] The dissolution of ammonium sulfide produces both the weak acid HS^- ions and H_2S molecules adsorbed onto the GaAs, which is closely correlated to the electrostatic interaction and surface dipole moment.[23] We suppose that the solution temperature affects both the rate of oxide removal and the creation of sulfur bonds, mainly in terms of their activation energies; it also determines the dissociation of $(NH_4)_2S$ solution. The higher removal efficiency at increased temperatures may be ascribed to the enhanced migration of etching agent into the oxide layer[24] and the increasing solubility of As oxides.[25]

In Fig. 1c and d, another interesting feature was noticed; increasing the sulfide-treated temperature and adding the NH_4OH clean caused the rearrangement of the sulfur bonding state, i.e., more Ga–S bonds did emerge relative to the reduced As–S bonds. Such a surface bonding reconstruction was attributed to the following conversion mechanisms: (*i*) AsS_x sulfidized compounds transfer into highly stable GaS_x species by reacting with GaAs surface;[26] (*ii*) because As–S chemical bond easily breaks at temperatures as low as 200°C,[27-29] indicative of lower bonding strength, loose sulfur atoms thus prefer to create strong Ga–S bonds.[24] Furthermore, the NH_4OH alkaline solution was critical in abating these surface components compared to the results obtained in the untreated samples; we characterized that the NH_4OH rinse obviously decreased the content of not only As–O and As–As species but also Ga–O species. Here, we can only speculate on the underlying mechanism because the explicit role of NH_4^+ and OH^- ions in the dissolution of GaAs surface components is still in controversy.[25] Two kinds of surface-cleaning mechanisms, to our knowledge, have been conjectured. One is that OH^- ions directly react with either Ga or As chemical species, forming soluble compounds such as GaO_3^{3-} and AsO_2^- with the participation of free holes from the semiconductor;[29] another is that the former reaction initially produces hydroxides in the form of $Ga(OH)_3/As(OH)_3$, which are transformed into soluble complexes like hydroxygallate aggregates $NH_4Ga(OH)_4$ and $(NH_4)_3AsO_4$ via the assistance of free NH_4^+ agent.[25] Irrespective of the detailed dissolution procedure, the resultant defect suppression can then be expected to promote interface quality between Gd_2O_3 deposited film and GaAs substrate, thereby achieving better insulator properties. This claim was first supported by improved surface morphology after WCP modulation, as displayed in Fig. 3. The root-mean-square (rms) roughness of HCl-etched GaAs surface can be reduced from ca. 0.35 to ca. 0.25 nm by rinsing in either $(NH_4)_2S$ at 80°C or NH_4OH aqueous solution.

Figures 4a and b display the capacitor characteristics of $Pt/Gd_2O_3/n$-GaAs structures subjected to different WCPs. In the following discussion we denote the MOS capacitor [which underwent the HCl and $(NH_4)_2S$ processes] without and with the NH_4OH clean as the "HS sample" and "HNS sample," respectively. The bidirectional *C-V* curves in Fig. 4a show that the HNS sample relative to the HS sample had a high value of accumulation capacitance. However, they still presented the counterclockwise hysteresis loop,

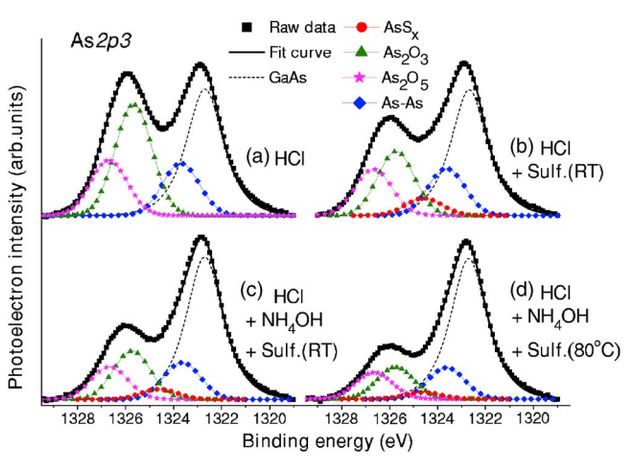

Figure 1. (Color online) As $2p_{3/2}$ XPS spectra of clean GaAs substrate subjected to four different WCPs. Five components were extracted: GaAs, AsS_x, As_2O_3, As_2O_5, and elemental As.

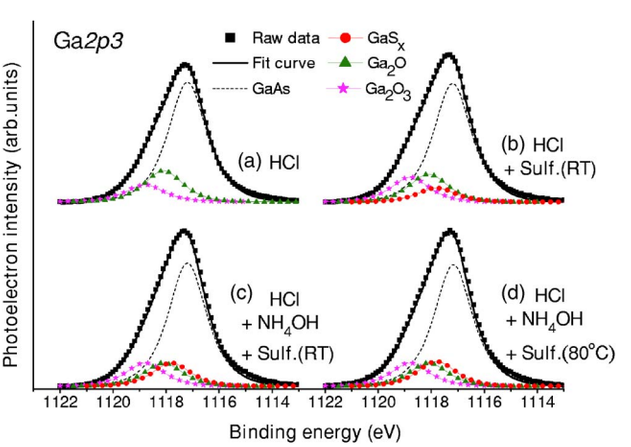

Figure 2. (Color online) Ga $2p_{3/2}$ XPS spectra of clean GaAs substrate subjected to four different WCPs. Four components were extracted: GaAs, GaS_x, Ga_2O, and Ga_2O_3.

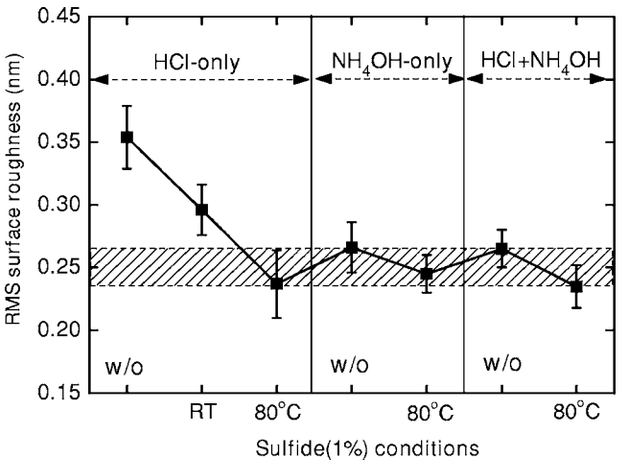

Figure 3. RMS surface roughness of clean GaAs substrate subjected to different WCPs.

which could be eliminated by increasing the sulfidized temperature up to 80°C. From the variation of $(NH_4)_2S$ concentration level, an increase in sulfide concentration from 1 to 10% plainly degraded the overall accumulation capacitance. In addition, because poor insulator–substrate interface leads to a remarkable shift of the flatband voltage (V_{FB}), i.e., the large frequency dispersion at the accumulation/depletion region, in frequency-dependent *C-V* curves, we qualitatively examined the Fermi level (E_f) pinning effect through variations of the ΔC and ΔV that were defined as follows

$$\Delta C(\text{at } V_g = 3\text{V}) = 1 - C_{acc}(\text{at 1 MHz})/C_{acc}(\text{at 1 kHz}) \quad [1]$$

$$\Delta V(\text{at } C_{FB}) = V_g(\text{at 1 kHz}) - V_g(\text{at 100 kHz}) \quad [2]$$

where ΔC is the deviation of the accumulation capacitance measured at 1 kHz and 1 MHz for the V_g of 3 V, while ΔV is the voltage difference between 1 and 100 kHz *C-V* curves, achieving the value of the flatband capacitance (C_{FB}). In Fig. 4b, the respective ΔC and ΔV were ca. 64% and ca. 2.2 V for the HS sample; both values could be reduced to ca. 38% and ca. 1.4 V provided that we added the NH_4OH clean with sulfidization at 80°C. These improvements confirmed that the WCP optimization further unpinned the interface Fermi level. Due to a high density of surface states formed by segregated As atoms, the E_f at the GaAs(100) surface being pinned at ca. 0.8 V below the conduction band (E_c) minimum was demonstrated.[30,31] Possible energy-level models, based on the framework of a donor state near the midgap with an acceptor state close to the valence band (E_v) edge, have also been proposed.[32] It seems that the lower surface states induced by sulfide passivation can cause a movement of the E_f back toward the E_c.[10,33] However, this conclusion is not confirmative because some previous experimental findings in which the E_f moved toward the E_v by ca. 0.2 eV were also illustrated.[34,35] We suggest that the movement of surface Fermi level is related to the actual sulfidation procedure and the resulting sulfur adsorption; the E_f intends to shift back to E_c provided that more Ga–S bonds form at the interface,[36] for example, which can be obtained after high-temperature annealing. On the as-treated sample the formation of less-stable As–S bonds compared to Ga–S bonds has been deduced to induce the extra gap states;[37] this consequence directly affects the shift behavior of the E_f in experiments. In our case, because the interfacial state density (D_{it}) was reduced from the order of 10^{13} to 10^{12} cm^{-2} eV^{-1}, we believe that improved WCP, along with relatively more GaS_x formation, did facilitate the reduction of overall surface recombination centers, in particular for donors induced by As_{Ga} antisites. Evidently, it promotes the carrier population at the dielectric interface at a high frequency of 1 MHz, coinciding with the consequence of ΔC and ΔV reduction.

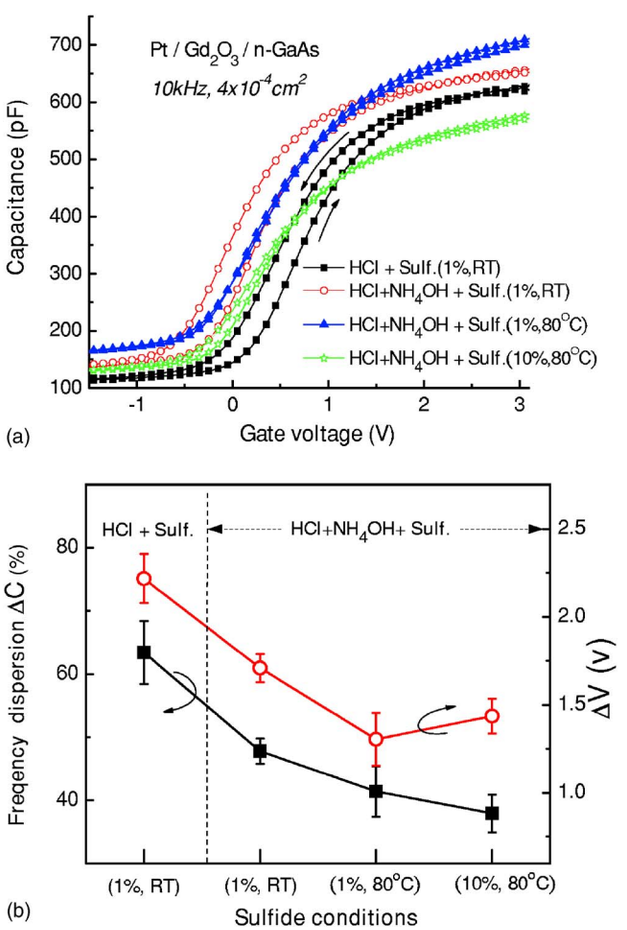

Figure 4. (Color online) (a) Bidirectional sweep (10 kHz) *C-V* curves; (b) the frequency response of $\triangle C$ and $\triangle V$ values for $Pt/Gd_2O_3/n$-GaAs capacitors with four kinds of WCPs.

Figure 5 shows the corresponding *I-V* characteristics, and the inset displays the comparison of gate leakage J_g at $V_g = (V_{FB} + 1)$ V for all samples with different WCPs. The result clearly indicates that the WCP [HCl + NH_4OH + sulfide (1%, 80°C)] led to better leakage performance and that J_g could be reduced to ca. 1.5×10^{-5} A/cm^2 at $V_g = (V_{FB} + 1)$ V; however, either increasing the concentration to 10% or lowering the temperature to room temperature caused J_g to increase considerably. Our explanations for these experimental findings are given below. In the course of performing $(NH_4)_2S$ immersion, one or two GaAs sulfide monolayers were formed upon bonding saturation, and then sulfur ions remained on the outer surface, probably in the form of either molecules or a complex compound. Excess sulfur contamination might be induced by the increased concentration; we evidenced this consequence by the AFM images that the 1% sulfide could flatten the morphology of HCl-etched surface, whereas an increased roughness was seen after 10% sulfide due to the presence of small particles (not shown here). Subsequent annealing-induced diffusion toward the Gd_2O_3 thin film possibly induced the leakage path and/or behaved as a leaky defect, causing gate-leakage degradation with increased equivalent-oxide-thickness (EOT). In addition, as we mentioned earlier, more As–S bonds formed at room temperature than at 80°C, and they were reduced to elemental arsenic because kinetics naturally drives the reaction below[26]

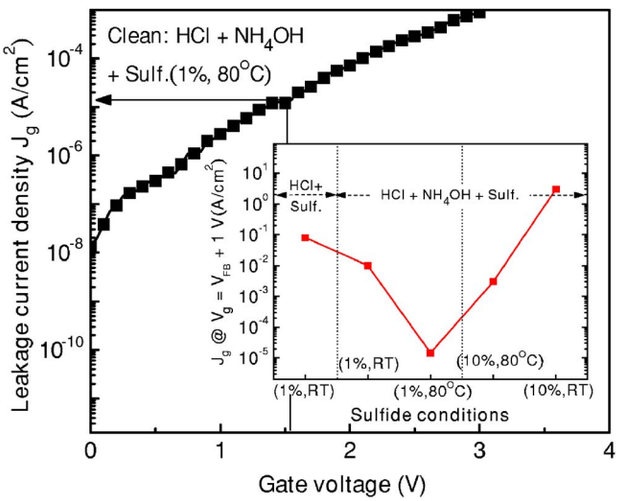

Figure 5. (Color online) *I-V* characteristics of $Pt/Gd_2O_3/n$-GaAs capacitor with the WCP – HCl + NH_4OH + sulfide (1%, 80°C). The inset displays the plot of J_g at $V_g = (V_{FB} + 1)$ V vs WCP conditions.

$$GaAs + AsS_x \rightarrow GaS_x + 2As \quad [3]$$

Higher sulfidized temperature, i.e., 80°C, reduced As suboxides and arsenic accumulation at the high-*k*/GaAs interface, resulting in lowered J_g and less-severe charge trapping. This fact also implies that forming stable Ga–S chemical bonds at the interface is indispensable in the pursuit of high-performance high-*k* gate dielectric and interface on GaAs substrate. Figure 6 shows the XPS spectra for these samples after 500°C PDA. It was found that both Ga and As oxide components had been incorporated into the annealed Gd_2O_3 films. The estimated concentration of Ga_2O_x is 13, 6, and 4%, with that of As_2O_x below 3% for the respective samples. The enrichment in Ga–O relative to As–O species in bulk Gd_2O_3 can be reasonably understood by the following heat reaction

$$GaAs + As_2O_3 \rightarrow Ga_2O_3 + 4As \quad [4]$$

This chemical transformation is thermodynamically favorable at room temperature. We did observe a relatively high Gd_2O_3 concentration in the HS sample, which was accompanied by serious desorption of the interfacial arsenic into high-*k* dielectric film. As a result, we think that it is a direct attribute of J_g increase and other degraded electrical properties.

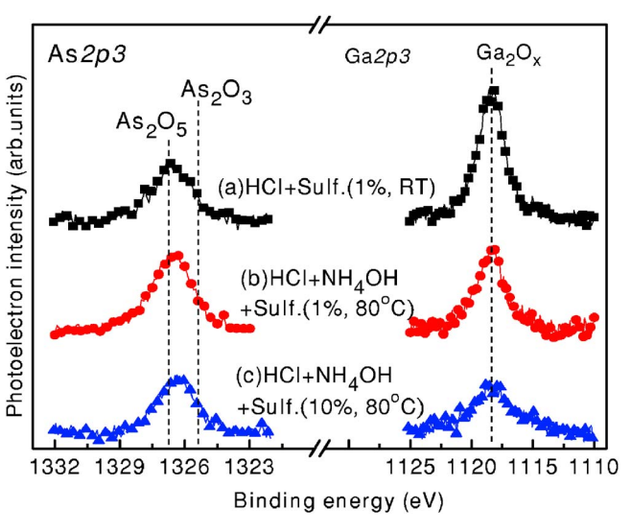

Figure 6. (Color online) As $2p_{3/2}$ and Ga $2p_{3/2}$ XPS spectra of the $Pt/Gd_2O_3/GaAs$ structures investigated in Fig. 4 and 5.

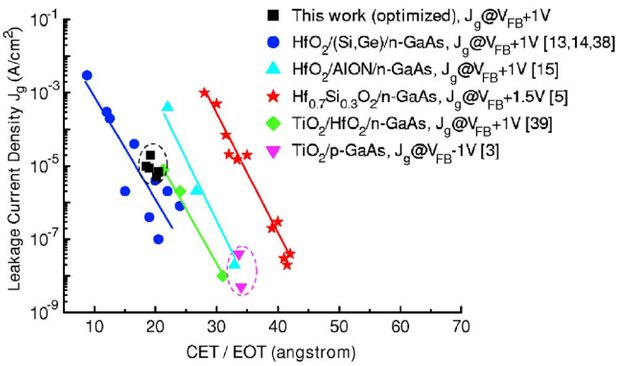

Figure 7. (Color online) Comparison of J_g vs CET or EOT characteristics for $Pt/Gd_2O_3/n$-GaAs capacitors with other published data.

Figure 7 plots the characteristic of J_g vs CET or EOT along with the previously published data.[3,5,13-15,38,39] We observed that the Gd_2O_3/n-GaAs capacitors through WCP optimization exhibited excellent insulating properties as compared to HfO_2 dielectrics reported on the n-GaAs in combination with Si or Ge interfacial passivation layers. A lower CET of ca. 20 Å with a reduced J_g of ca. 10^{-5} A/cm^2 at $(V_{FB} + 1)$ V was accomplished. Continuously optimized interface quality via process modification is expected to further improve $Gd_2O_3/GaAs$ electrical performance, which could thus be considered as a promising MOS device structure.

Conclusions

This study presented improved electrical characteristics of the $Gd_2O_3/GaAs$ structure by modifying wet-chemical clean and $(NH_4)_2S$ treatment on the dielectric interface. Photoemission analysis showed that As oxides tended to reside near the upper surface relative to Ga oxides, while excess arsenic atoms were generated and then piled up close to the GaAs substrate. We found that employing NH_4OH alkaline solution and then sulfide passivation at 80°C further suppressed these surface components, thereby enhancing their capacitor performance. Higher oxide capacitance with reduced *C-V* frequency dispersion was shown, which was direct evidence of abating the E_f pinning effect; also, diminutive hysteresis (<100 mV) was achieved. In addition, the $Gd_2O_3/GaAs$ capacitor exhibited J_g of ca. 1.5×10^{-5} A/cm^2 at $V_g = (V_{FB} + 1)$ V with CET of ca. 20 Å, which was comparable to the reported performance of the $HfO_2/GaAs$ system with an ultrathin Si/Ge interfacial layer. The inhibited formation of native oxides and elemental arsenic at high-*k*/sulfur-passivated GaAs interface were mainly responsible for these electrical improvements.

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