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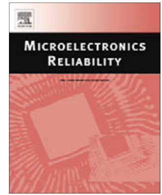

A simple method for sub-100 nm pattern generation with I-line double-patterning technique

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ABSTRACT

We have developed a simple method adopting double-patterning technique to extend the I-line stepper limit for the sub-100 nm poly-Si pattern generation in this work. Through in-line and cross-sectional scanned electron microscopic analyses of the generated patterns, we confirmed the feasibility of the double-patterning technique for the fabrication of nano-scale devices. Resolution capability of this technique has been confirmed to be at least 100 nm, which is much superior to the resolution limit of conventional I-line lithography. This approach has also been applied for fabricating p-channel metal–oxide-semiconductor field-effect transistors. Excellent device characteristics were verified.

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1. Introduction

The well-known Moore's Law states that the number of transistors on an integrated circuit (IC) chip will double every 18 months [1]. Since the advent of IC manufacturing, this law has been in force for decades. In order to keep up with the Moore's Law, shrinkage in device dimensions is indispensable, which also promotes device density, operation speed, and chip functionality. In other words, for better performance and cheaper manufacturing cost, the continuous scaling of the devices is evitable. To keep pace with the law, it requires innovation to overcome several fundamental physical barriers lying ahead, and first of all is to extend the photolithography limit. According to the Rayleigh's criterion, the resolution, *R*, of a photolithography technique can be expressed as follows [2]:

$$R = k_1\lambda/NA, \quad (1)$$

where k_1 is a system constant, λ is the wavelength of incident light, and *NA* is the numerical aperture of the lithography system. Based on such criterion, we could adjust the three factors of the criterion so as to boost the resolution of a lithography system [3–5]. Nowadays, state-of-the-art mass production of nano-scale ICs employs the immersion lithography tools with the 193 nm excimer laser as the exposure light source, which has been widely adopted in 300-mm wafer fabrication for manufacturing chips with sub-100 nm technology node. However, the extremely high cost on the lithography tool and related processes hinders these tools from being used in the laboratories of universities. On the other hand, electron-beam lithography [5] is therefore far more popular in these environments for generating sub-100 nm patterns, although the throughput is dramatically limited, and thus its proliferation in mass manufacturing is prohibited.

Recently, it was reported that the double exposure (DE) technique [6], and double-patterning (DP) technique [7–9] were being considered as promising candidates to extend lithography processing beyond the 45 nm node at k_1 factors below 0.30. DP is a process that splits one patterning step into two to relax the imaging fidelity requirements for small technology nodes. The most common form of DP typically decomposes a target layout pattern into two separate photomasks employing two exposure steps and subsequent etching steps. Consequently, the dimensions of the final target patterns can easily break the resolution limit with single exposure. Usually I-line stepper is not capable of sub-100 nm pattern generation owing to its long exposure wavelength of 365 nm. In this work, we develop a DP technique with conventional I-line stepper to generate sub-100 nm photoresist (PR) patterns with the goal to fabricate nano-scale MOSFETs. Although this technique consists of two times the lithographic and subsequent etching steps, we show that the DP method could reliably generate line patterns with dimension down below 100 nm. Our results indicate that the method developed in this work is promising for both the research works carried out at universities and for practical manufacturing in terms of much lower cost (as compared with state-of-the-art DUV lithography) and decent throughput.

2. Experiments

For all lithographic steps carried out in this work, we used an I-line stepper (Canon FPA-3000i5+) to generate the photoresist (PR)

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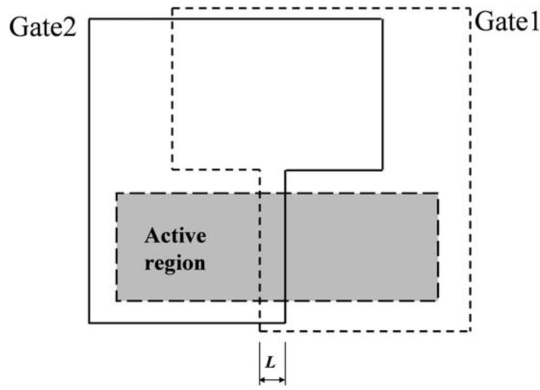

Fig. 1. Mask layouts for defining the gate pattern on the active region. Gates 1 and 2 represent the two masks used in the DP process. Channel length of the device is determined by the overlap region of the two masks in the active region.

patterns. We have implemented the DP technique on the practical fabrication of nano-scale p-channel metal–oxide-semiconductor field-effect transistors (pMOSFETs). Fig. 1 is the schematic of the two masks used for generating the gate patterns. The most critical portion in the design is the overlapped region of the two gate patterns in the active area which determines the channel length (L) of the fabricated device.

Fig. 2 illustrates the major process steps in the device fabrication. Local oxidation of Si (LOCOS) scheme was first used for device isolation. N well was then formed by P^+ implantation with energy of 120 keV and dose of $7.5 \times 10^{12}\ cm^{-2}$, followed by an anneal at 1100 °C for dopant drive-in. Next, channel stop implantation was performed by implanting As^+ (120 keV, $3 \times 10^{12}\ cm^{-2}$), followed by wet oxidation to form 550 nm-thick field oxide. Anti-punch through and threshold voltage adjustment implantations were performed individually by implanting P^+ (120 keV, $4 \times 10^{12}\ cm^{-2}$) and As^+ (80 keV, $1 \times 10^{13}\ cm^{-2}$), respectively. Thermal gate oxide of

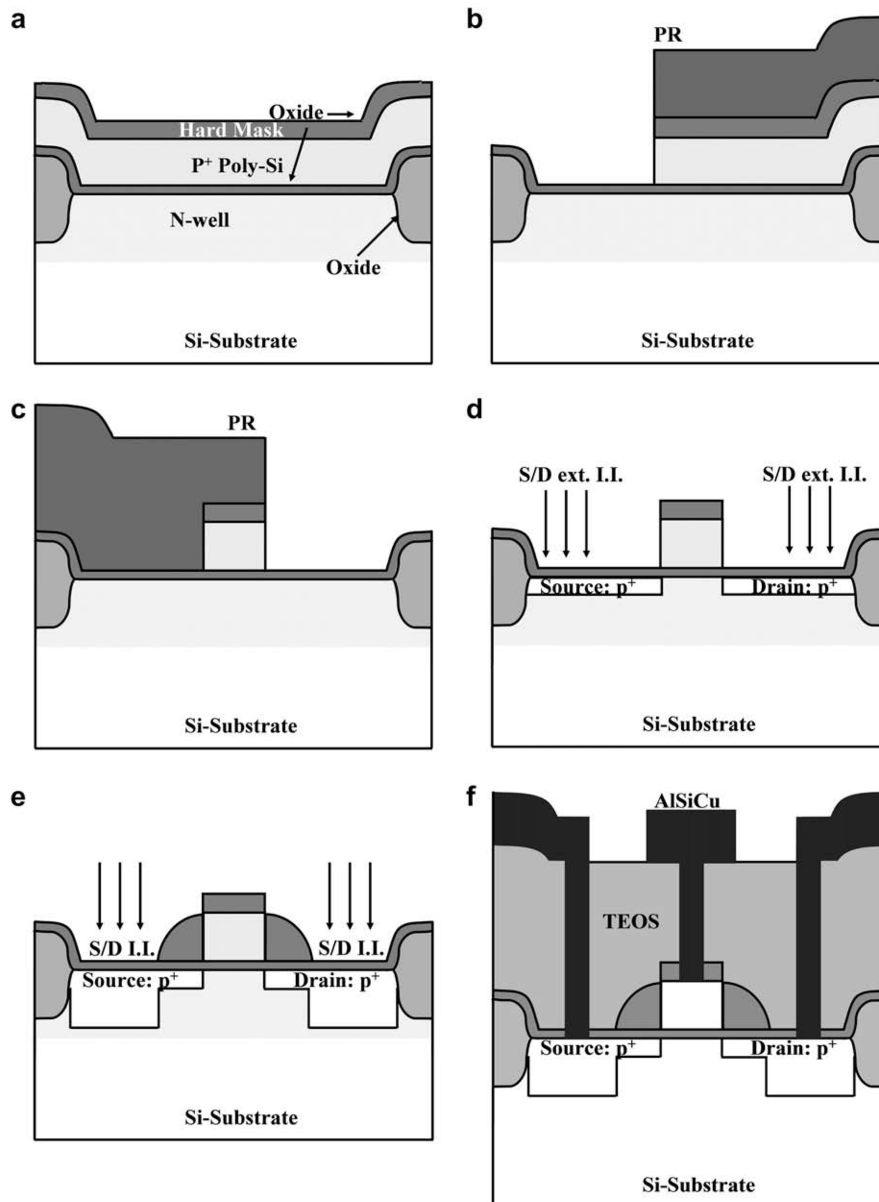

Fig. 2. Process flow of a pMOSFET with the DP method. (a) Deposition of TEOS and poly-Si layers onto the gate oxide (active region) and field oxide (isolation region). (b) First gate pattern definition. (c) Second gate pattern definition. (d) S/D extension implantation. (e) Spacer formation and deep S/D implantation. (f) Formation of contact holes and test pads.

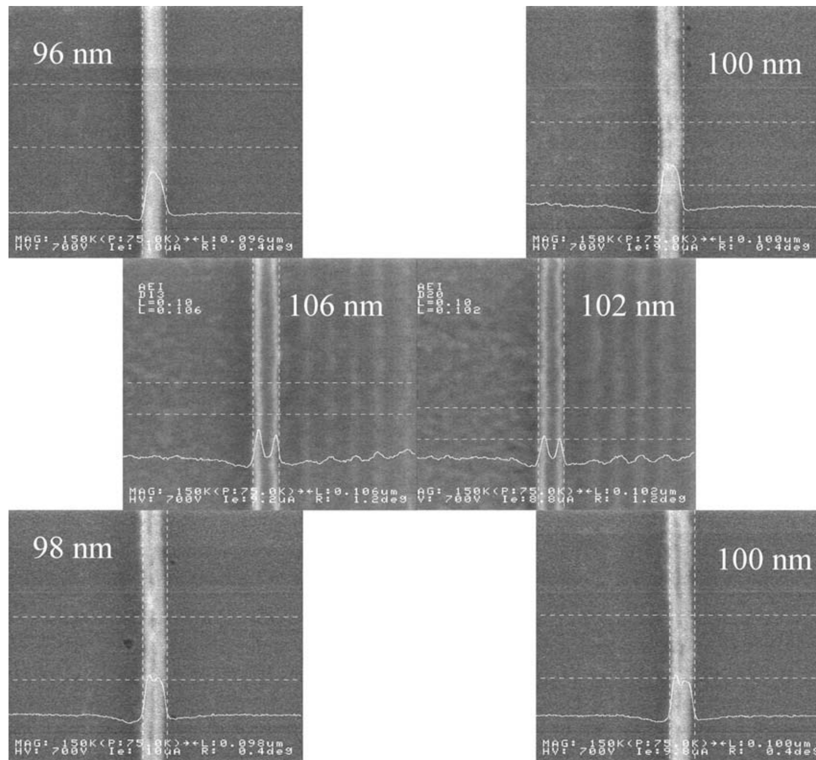

Fig. 3. In-line SEM images of poly-Si structures formed with the DP method with nominal width of 100 nm. The images were taken from different locations on a 6-in. Si wafer. The measured width is given in each picture.

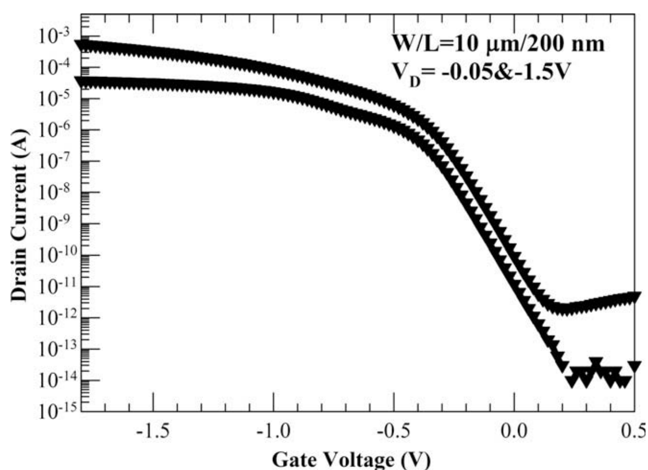

Fig. 4. Transfer characteristics of a pMOSFET with channel length of 200 nm and channel width of 10 μm, measured at $V_D = -0.05$ and -1.5 V.

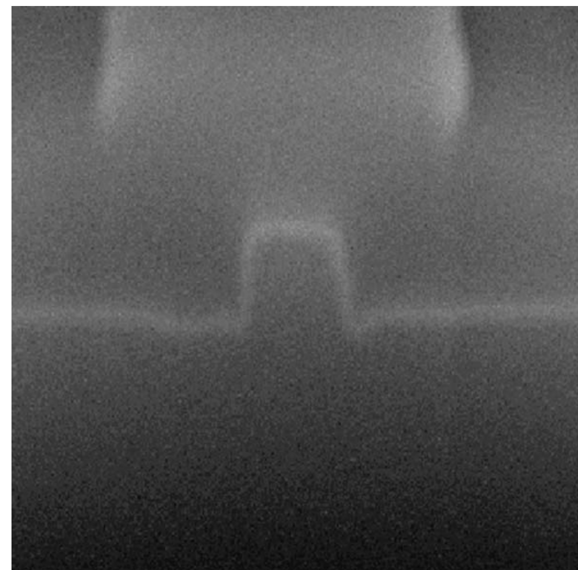

Fig. 5. Cross-sectional SEM image of a fabricated device with channel length of 200 nm.

about 3 nm was subsequently grown in an N_2O ambient, followed by the deposition of 200 nm undoped poly-Si and gate implantation (BF_2^+, 10 keV, 5×10^{15} cm^{-2}). Afterwards a LPCVD tetraethoxysilane (TEOS) oxide of 50 nm was deposited to serve a hard mask layer, as shown in Fig. 2a. After gate definition using the DP method (Fig. 1) with the two masks shown in Fig. 1 (Fig. 2b and c), shallow source/drain (S/D) extension regions were formed by implanting BF_2^+ (10 keV, 5×10^{14} cm^{-2}), as shown in Fig. 2d. After forming a 100 nm TEOS sidewall spacer, deep S/D junctions were formed by implanting BF_2^+ (15 keV, 5×10^{15} cm^{-2}), and then annealed at 1000 °C for 5 s as shown in Fig. 2e. Finally, a conventional AlSiCu metallization was carried out to form the metal pads (Fig. 2f). Electrical characterizations were performed using an HP 4156 system.

3. Results and discussion

3.1. Feasibility of the DP process

In-line SEM images of several etched poly-Si structures with the designed pattern width of 100 nm are shown in Fig. 3. These

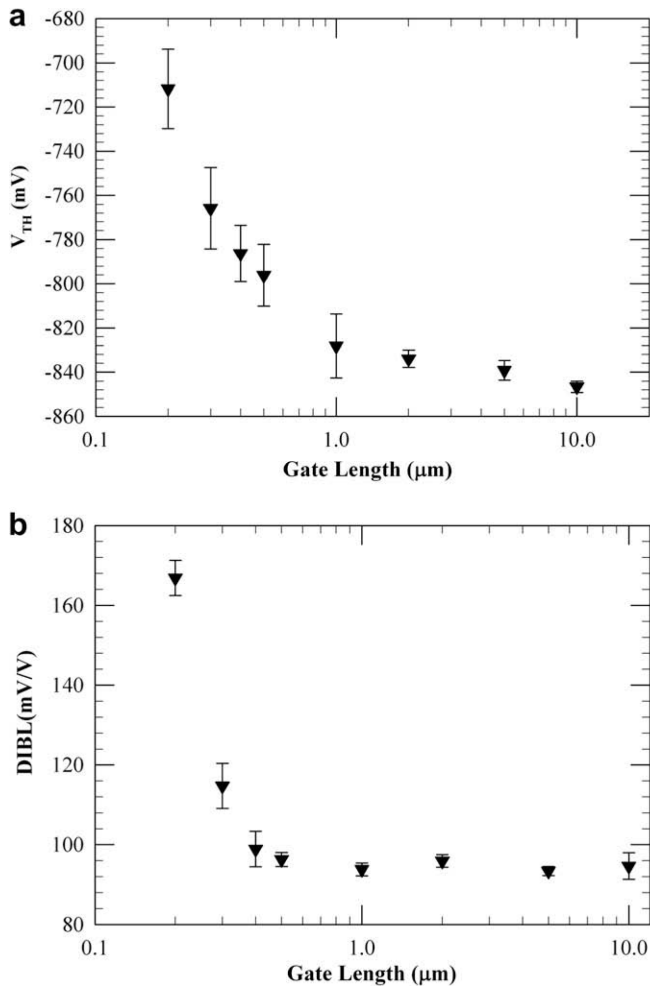

Fig. 6. (a) Threshold voltage (V_{TH}) and (b) drain induced barrier lowering (DIBL) of the fabricated devices as a function of gate length.

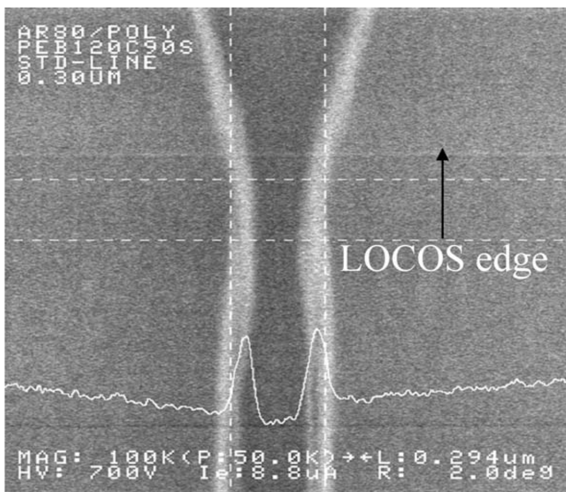

Fig. 7. In-line SEM view of a fabricated device showing the necking of the poly-Si gate at the isolation edge.

images were taken from different locations of a 6-in. Si wafer. The range of the measured pattern width is distributed from 96 to 106 nm in Fig. 3. These results confirm the feasibility of the DP method for forming structures having dimension as small as 100 nm with an I-line stepper. The capability of the developed method for forming sub-100 nm poly-Si patterns is also examined with in-line SEM. However, we found the fluctuation in the measured line width of the patterned poly-Si structures becomes large as the nominal width is smaller than 100 nm. Such finding is reasonable when considering the overlay limit of the exposure system which is 45 nm as listed in the specification information provided by the vendor. Since the dimension of the patterned lines is determined by the overlap region of the two gate masks (see Fig. 1), the misalignment of the two masks would definitely affect the control of the critical dimension.

3.2. Device characteristics

Next we shift our attention to fundamental electrical characteristics of the fabricated devices. Typical transfer characteristics of a pMOSFET with channel length of 200 nm and channel width of 10 μm are illustrated in Fig. 4 with drain induced barrier lowering (DIBL) of 166 mV/V, subthreshold swing of 77 mV/dec. Cross-sectional SEM of the device is illustrated in Fig. 5. Fig. 6a and b shows the threshold voltage (V_{TH}) and DIBL, respectively, of the devices as a function of the gate length. Overall the device performance is decent. Nonetheless, poor device characteristics featuring significant punch trough are observed for devices with channel length of 100 nm or below. This is partly ascribed to the non-optimal implant conditions used in the device fabrication. During the course we have also found the occurrence of the necking phenomenon at the isolation edge as shown in Fig. 7. The origin of this phenomenon is postulated to be caused by the uneven morphology of the LOCOS isolation. The necking is observed in long- and short-channel devices, and is responsible for the leaky characteristics of the short-channel devices. We are currently investigating the cause of the necking, trying to resolve the issue and pushing the channel length of the fabricated devices down below 100 nm.

4. Conclusion

In this work we present the results of developing an I-line DP technique for generating sub-100 nm patterns which are much finer than the resolution capability of the conventional I-line lithography. The feasibility of this approach is confirmed through the in-line and cross-sectional SEM characterization. Although an additional lithographic step and an additional etching step are required in the process, the overall throughput is still much higher than the e-beam lithography, while the process cost could be significantly lower than the DUV lithography. Finally, this approach has been applied for device fabrication. The fabricated pMOSFETs with 200 nm channel length have been characterized and confirmed with good characteristics and control over the short-channel effects. With suitable modification of layout design, we believe the necking issue mentioned above will be settled completely for the sub-100 nm device fabrication. These results clearly evidence the usefulness of the proposed I-line DP technique for nano-scale device fabrication and study.

Acknowledgments

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