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Enhancement of Charge-Storage Performance in Ni-Silicide Nanocrystal Devices by Thermal Annealing a Ni–Si–N Thin Film

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The stored charge characteristics of Ni-silicide nanocrystals embedded in nitride formed by annealing a Ni–Si–N thin film were studied in this paper. We used X–ray photoelectron spectroscopy, leakage current density, and X-ray diffraction to offer chemical material analysis of nanocrystals with surrounding dielectric and the crystallization of nanocrystals for different thermal annealing treatments. Transmission electron microscope analyses revealed nanocrystals embedded in the nitride layer. Nonvolatile Ni–Si nanocrystal memories with 600°C annealing revealed superior electrical characteristics for charge-storage capacity and reliability compared with the memories with 300 and 500°C annealing. In addition, we used energy-band diagrams to explain the significance of surrounding dielectric for reliability.
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In recent years, portable electronic products, such as digital cameras, notebook computers, MP3 walkmans, intelligent IC cards, USB flash storage disks, etc., have been widely applied daily and play important roles in the consumer market. These electronic products are all embedded with flash memory devices. As the demand for flash memory devices grow increasingly, the device density and operation speed of flash memory as well as device reliability have also received much attention.[1-4] For the development of a next-generation nonvolatile memory (NVM) technique, devices should be compatible with the current integrated circuit manufacture process. Therefore, the silicon-oxide-nitride-oxide-semiconductor (SONOS) type and nanocrystals (NCs) memory structures have been proposed and demonstrated to lead to an improvement in reliability compared with conventional NVM because of employing discrete traps served as charge-storage media.[5,6]

In order to overcome the limitations of conventional NVM for the scaling-down process, we proposed memory structures that were combined with SONOS-type and metal NCs to obtain good charge-storage ability and strong coupling with conduction channel. In our work, we used a Ni–Si–N thin film to control the size and distribution of NCs by the internal competition mechanism[7] and studied the stored charge characteristics of Ni-silicide NCs embedded in nitride under different temperature effects. It was found that the crystallization of NCs and the quality of surrounding dielectric were distinct from the different temperature annealing; and thus that the annealing temperature was a key parameter for the charge-storage properties of NVMs.

Experimental

This memory cell was fabricated on a 4 in. p-type silicon (100) wafer with a resistivity of 10 Ω cm. After a standard clean process and native oxide removing, a 5 nm thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric-pressure chemical vapor deposition furnace. Afterward, a 10 nm thick nitrogen-incorporated $Ni_{0.3}Si_{0.7}$ layer serving as the charge-trapping layer was deposited by sputtering a $Ni_{0.3}Si_{0.7}$ commixed target in Ar/N_2 (24/10 sccm denotes cubic centimeter per minute at standard temperature and pressure) environment at room temperature, and the dc sputtering power was set to 80 W (deposition pressure ~7.6 mTorr). Here, we could obtain a Ni–Si–N thin layer by X-ray photoelectron spectroscopy (XPS) analysis (not shown). Then, a 30 nm thick blocking oxide was deposited by plasma-enhanced chemical vapor deposition at 300°C. In this study, before blocking oxide deposition, the charge-trapping layer was annealed at 300°C (sample A), 500°C (sample B), and 600°C (sample C) for 100 s using a rapid thermal annealing system to improve the shape and crystallization of NCs. Finally, Al gate electrodes on the back and front sides of the sample were deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. The formation flow of the memory cell structure is shown in Fig. 1. Electrical characteristics, including the capacitance–voltage (C-V) hysteresis, retention, and endurance characteristics were also performed. The C-V characteristics were measured by an HP4284 Precision LCR meter with a high frequency of 1 MHz. In addition, transmission electron microscopy (TEM), XPS, and X-ray diffraction (XRD) were adopted for the microstructure analysis, chemical material analysis, and crystallization of NCs.

Results and Discussion

Figure 2 exhibits the material analyses of the charge-trapping layer under the annealing temperature conditions of 300, 500, and 600°C. Figure 2a shows the N 1s core-level spectra with different temperature annealing. Obviously, the spectra are composed of two peaks, SiN (396.8 eV) and Ni–N (398.5 eV), for 300 and 500°C annealing.[8,9] The peak signal of Si–N bonding shifted toward higher binding energy, and the peak signal of Ni–N gradually decayed until it disappeared as the temperature increased. To further ascertain the crystallizations of NCs with different temperature annealing, XRD analyses were executed. As shown in Fig. 2c, the diffraction peak of

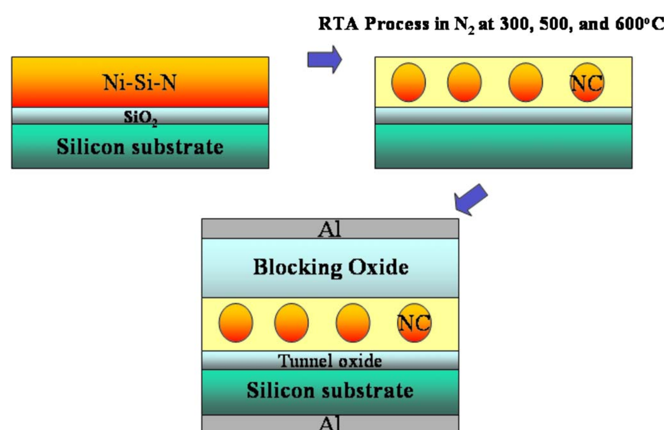

Figure 1. (Color online) Formation flow of the MOIOS structure under different annealing temperatures (300, 500, and 600°C).

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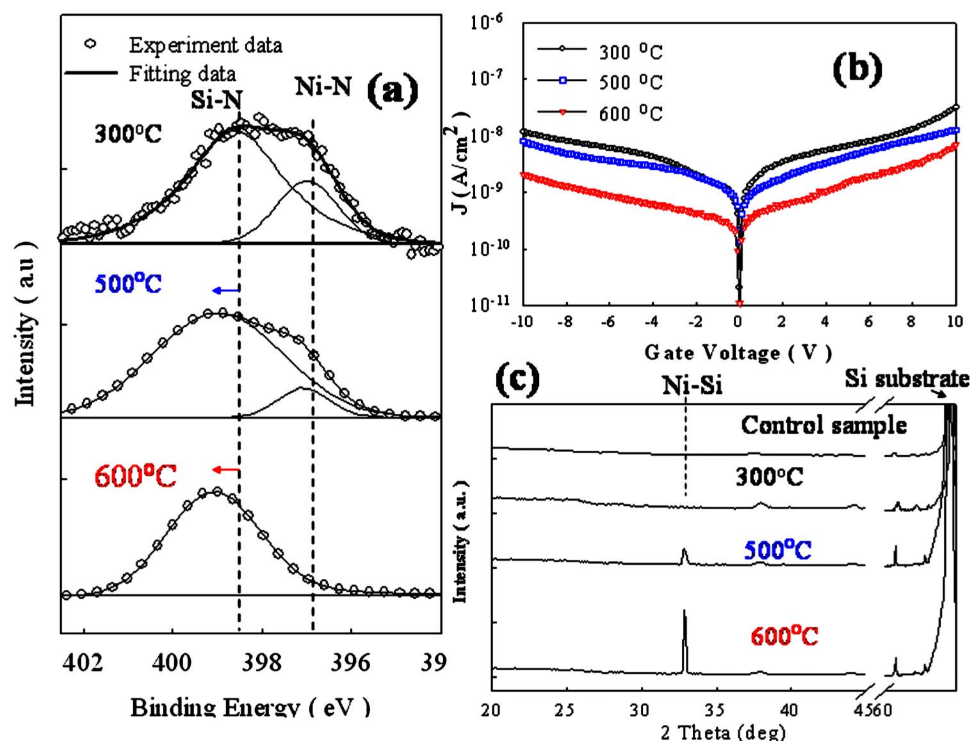

Figure 2. (Color online) (a) N 1s XPS analysis of NCs (empty circles and straight line indicate experimental and fitting results, respectively). (b) Leakage current density (A/cm^2) with gate voltage and (c) XRD analysis of NCs during different thermal annealing temperatures.

32.8° indicates the Ni–Si NCs are formed with an annealing temperature over 500°C.[10] (The control sample is only a structure of Si substrate with tunnel oxide.) From XPS analyses, we considered that the quality of the surrounding dielectric, SiN_x, had been improved by a reducible reaction of Ni–N during the thermal annealing process. To verify this view point, the leakage current density J (A/cm^2) with gate voltage was measured (as shown in Fig. 2b). It was found that the leakage current after 600°C annealing was the lowest under 0 to ±10 V sweeping. Moreover, the compound of NCs could be changed from Ni–N to Ni–Si after the annealing process and also affect charge-storage characteristics for the NVM application.

In general, the forward (from accumulation state to inversion state) and reverse *C-V* hysteresis was measured to investigate the charge-storage abilities of nonvolatile NC memories. Figure 3 presents the memory effect and TEM image (inset) of Ni–N NCs (sample A), and it is clearly observed that memory windows of 1.5 and 3.5 V can be obtained under ±10 and ±12 V operations, respectively. When the annealing temperature increases from 300 to 500°C (sample B) and 600°C (sample C), the memory window raises to 5.0 V for sample B and 4.0 V for sample C under ±10 V sweeping operation. Moreover, these samples also show that the roundness and isolation of NCs are better than for sample A by TEM analyses, as shown in Fig. 4 and 5. These physical phenomena could be contributed by a thermal-enhanced congregation of Ni atoms. According to a previous theoretical model about the probability of an electron escaping from the NC back to the channel, the spherical NCs can reduce the Weinberg impact frequency, which is af-

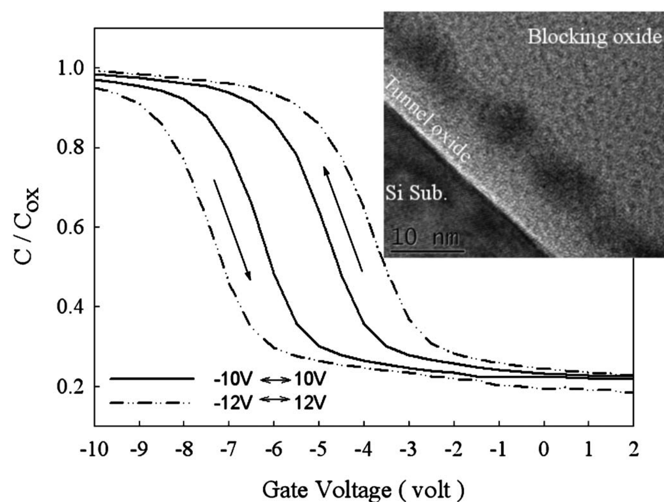

Figure 3. *C-V* hysteresis and TEM image (inset) of nonvolatile Ni–N NC memories (300°C). The memory window was 1.5 V under ±10 V operation.

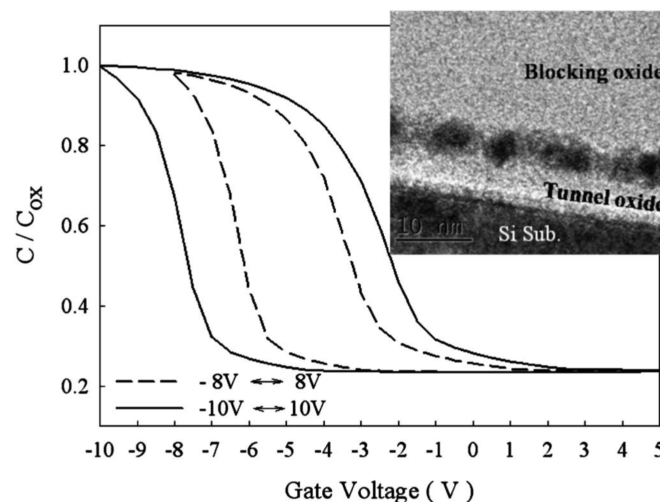

Figure 4. *C-V* hysteresis and TEM image (inset) of nonvolatile Ni–Si NC memories (500°C). The memory window was 5.0 V under ±10 V operation.

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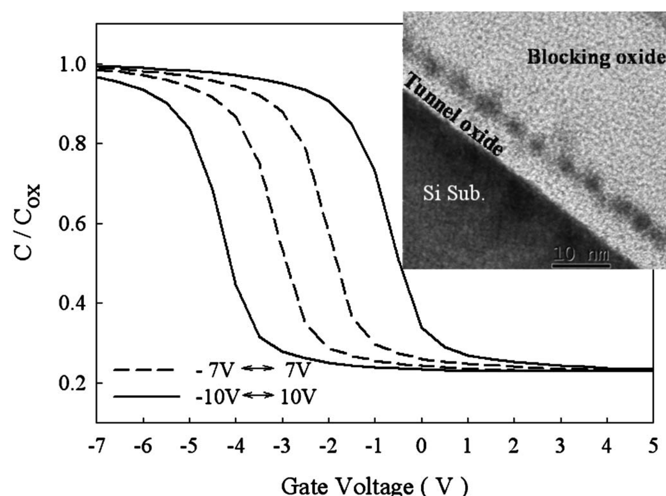

Figure 5. *C-V* hysteresis and TEM image (inset) of nonvolatile Ni–Si NC memories (600°C). The memory window was 4.0 V under ±10 V operation.

fected by the geometry effect.[11] The more-separated NCs could also restrain the electrons' lateral migration effect under a retention test, because the electrons stored in the NC lift the energy level of the NC conduction band, resulting in the increase of the escaping probability. Therefore, the rotundity and severance of NCs are good for the sub-50 nm gate-length process application.

We further compared charge-storage characteristics of samples A–C such as the memory window, retention, and endurance. The results are listed in Table I. The memory window of sample B is three times larger than that of sample A. Because the resistivity of Ni–Si NCs (14–20 $\mu\Omega$ cm) is smaller than Ni–N NCs (151.7 $\mu\Omega$ cm) and the resistivity is inverse with the density of states, which is a property that affects the number of storage charges,[12] sample B has a superior memory window due to a lower amount of Ni–N NCs (as shown in Fig. 2). Hence, it is believed that the nonvolatile memory capacity was greatly influenced by the crystallizations characteristic of Ni–Si and Ni–N NCs. In addition, the initial memory window was fixed at the same value for the retention and endurance test. The memory window of retention was obtained by comparing the *C-V* curves from a charged state (write/erase (W/E) state) and the quasi-neutral state, for which we used an extrapolation (between 1–10^4 s) to give a long-term predictable result (10 years). Furthermore, the W/E biases for endurance were set at V_G-$V_{flatband}$ = ±5 V for 0.1 ms (this condition was enough to define the data information for the current NVMs). Table I clearly indicates that the reliability of nonvolatile Ni–Si NCs memories (sample B and sample C) is better than Ni–N NCs (sample A). According to the above-mentioned material analyses, we concluded that the annealing temperature had a great influence on the properties of NCs, and this factor also significantly affected the memory window.

Table I. Comparison table for the memory window retention, and endurance. The initial memory window was fixed at the same value for the retention and endurance test.

	Memory window under ±10 V	Memory window after 10 years (retention: electrons holding ratio)	Memory window after 10^6 W/E cycles (endurance)
Sample A (300°C)	1.5 V	0.5 V (20%)	1.0 V (degradation 50%)
Sample B (500°C)	5.0 V	0.7 V (31%)	2.1 V (degradation 0%)
Sample C (600°C)	4.0 V	1.1 V (50%)	2.1 V (degradation 0%)

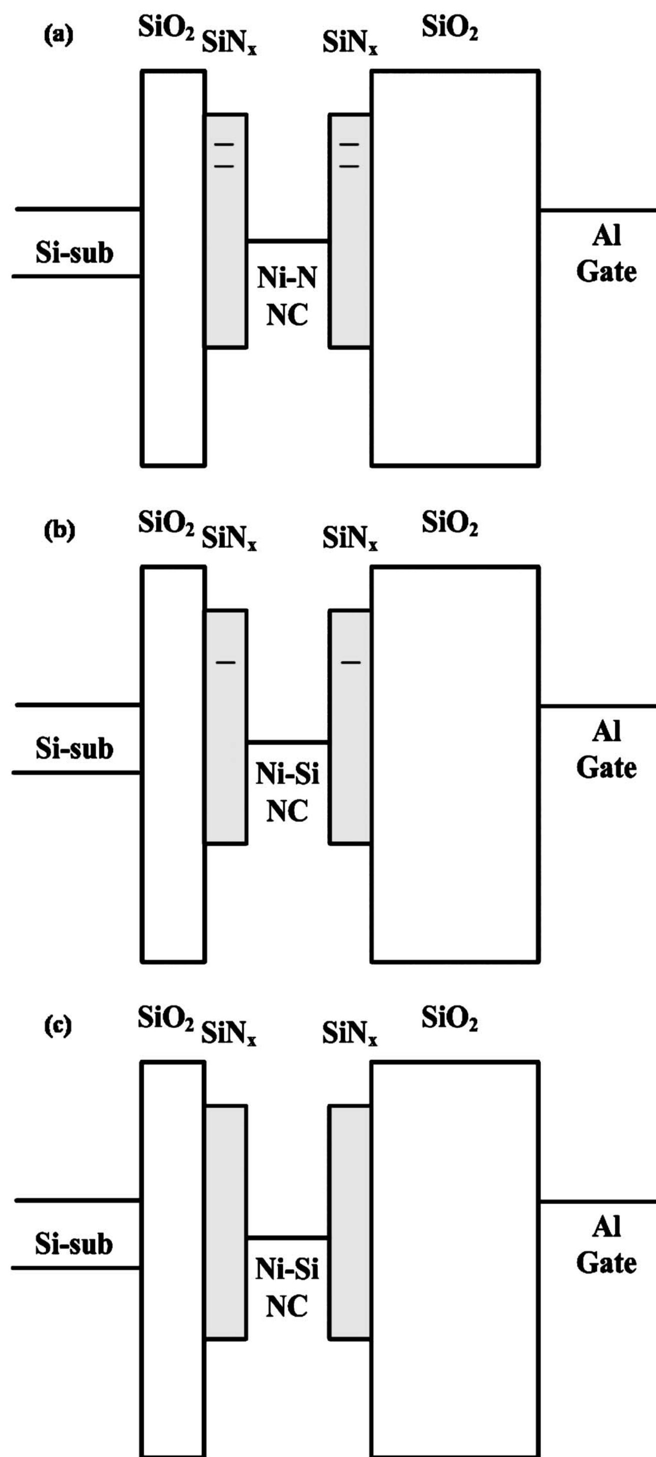

Figure 6. Energy-band diagrams of (a) Ni–N NCs (300°C), (b) Ni–Si NCs (500°C), and (c) Ni–Si NCs (600°C) embedded in the nitride layer.

Here, the conjectural energy-band diagrams were proposed to explain these physical phenomena of charge storage, as shown in Fig. 6. Because the density of traps in the nitride layer decreased as the annealing temperature increased, sample C (600°C) had the least trap density, as shown in Fig. 6c. However, the reduction in trap density resulted in a memory window in sample C that was

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lower than that of sample B, because the traps of nitride could provide additional charge-storage nodes. Although the nitride traps can improve the memory window, electrons stored in these shallow traps of nitride easily escape to the substrate. In addition, the nitride traps surrounding the NCs also provide leakage paths for the stored carriers of NCs. Both the above drawbacks cause the retention of samples A and B to be worse than sample C. As shown in Table I, the electron holding ratio of 50% of sample C, estimated for 10 years, is much better than sample B (31%) and A (20%). Moreover, the endurance results reveal that samples B and C had excellent reliability after 10^6 W/E cycles operation, because the stronger silicon–nitrogen bonding (as shown in Fig. 2a) could suppress the damage during W/E operation. Summarizing the above results, the nonvolatile Ni–Si NC memory after an annealing temperature of 600°C exhibits the best NVM performance, and this device can also be used on a low-temperature substrate (<600°C) for next-generation applications.

Conclusion

In conclusion, the nonvolatile memory characteristics were influenced by the crystallizations of Ni–Si and Ni–N NCs. The nonvolatile Ni–Si NC memory showed better charge storage ability and reliability than nonvolatile Ni–N NCs memory, because Ni–Si NCs have higher density of states and stronger surrounding dielectric than the others. Hence, the MOIOS structure needed a 600°C thermal annealing process to obtain a high-performance nonvolatile NC memory in this work. In addition, the proposed energy-band diagrams could clearly explain the trap density of surrounding dielectric, SiN_x, and how it affected the NVM characteristics.

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