 Journal of The Electrochemical Society, **155** (2) J50-J54 (2008)
0013-4651/2007/155(2)/J50/5/$23.00 © The Electrochemical Society

CF_4-Plasma-Induced Fluorine Passivation Effects on Poly-Si TFTs with High-κ Pr_2O_3 Gate Dielectric

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High-performance polycrystalline silicon thin-film transistors (poly-Si TFTs) integrating high-κ Pr_2O_3 gate dielectric and fluorine-passivated poly-Si film are demonstrated. High gate capacitance density and thin equivalent-oxide thickness provided by the high-κ Pr_2O_3 gate dielectric have the advantage of increasing the driving current capability of the TFT device, but an undesirable off-state leakage current could be introduced from the high electric field near the drain side. Introducing fluorine atoms into poly-Si films by employing a low-temperature CF_4 plasma treatment can effectively passivate the trap states. With 10 W CF_4 plasma treatment on poly-Si film, the electrical characteristics of poly-Si Pr_2O_3 TFTs can be significantly improved, including a steeper subthreshold swing, smaller threshold voltage, higher field-effect mobility, and better on/off current ratio compared with that without CF_4 plasma treatment. The maximum off-state leakage current of the fluorine-passivated TFT is more than one order of magnitude lower than that of the control TFT. Furthermore, the incorporation of fluorine atoms by CF_4 plasma treatment also improves the reliability of poly-Si Pr_2O_3 TFTs against hot carrier stressing, which is due to the formation of stronger Si–F bonds in place of weak Si–H bonds in the poly-Si channel and at the Pr_2O_3 gate dielectric/poly-Si interface. Therefore, high-performance and high-reliability poly-Si TFTs with Pr_2O_3 gate dielectric and CF_4 plasma treatment on poly-Si film are suitable for active-matrix liquid crystal display application.
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Manuscript submitted August 22, 2007; revised manuscript received October 22, 2007. Available electronically December 6, 2007.

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have received considerable attention in fields such as large-area electronic applications including linear image sensors and active-matrix liquid crystal displays (AMLCDs).[1,2] The major application of poly-Si TFTs in AMLCDs lies in integrating the peripheral driving circuits and the pixel switching elements on the same glass substrate to realize system-integration-on-panel technology.[3] The complicated process can be greatly simplified and the fabrication cost can be reduced by realizing system-integration-on-panel technology. However, it is difficult to develop high-performance and high-reliability poly-Si TFTs that are applicable for both pixel-switching elements and peripheral driving circuits. Pixel-switching elements require TFTs to operate at high voltages as well as low gate-leakage currents to drive the liquid crystal. In contrast, TFTs with good electrical characteristics, including low operation voltage, low subthreshold swing, high driving current, and low gate-leakage current, are necessary for achieving the peripheral driving circuit applications. Because poly-Si TFTs are usually fabricated on inexpensive glass substrate, a low-temperature process is required for the realization of commercial flat-panel displays. The solid-phase crystallization (SPC) process with a maximum process temperature limited to 600°C is widely used to recrystallize amorphous Si film due to its low production cost and good grain-size uniformity.[4] Poly-Si TFT with a thinner physical gate-dielectric thickness can increase the gate capacitance density and enhance the driving-current capability. However, a higher gate-leakage current could be introduced by the thinner gate dielectric, exhibiting significantly degraded electrical characteristics of poly-Si TFT.[5]

Several high-κ materials, including oxide/nitride/oxide (ONO) gate stack, Al_2O_3, and Ta_2O_5, were proposed to replace conventional SiO_2 to serve as the gate dielectrics of poly-Si TFTs.[6-8] The gate capacitance density of high-κ gate dielectrics is higher than that of SiO_2 gate dielectric. To reach the same value of gate capacitance density, the physical thickness of the high-κ gate dielectrics can be thicker than that of the SiO_2 gate dielectrics. Therefore, incorporating high-κ gate dielectrics into poly-Si TFTs could induce a higher mobile carrier density in the channel region and suppress the gate-leakage current to improve gate controllability. However, such high gate capacitance density would contribute to a high electric field at the gate-to-drain overlap area, resulting in a rather high field-enhanced emission via the trap states at the grain boundaries. Therefore, poly-Si TFTs with high-κ gate dielectric would suffer from a more undesirable gate-induced drain leakage (GIDL) current.[9] To address this GIDL issue, various techniques, including hydrogen-plasma treatment and fluorine-ion implantation on poly-Si film, have been applied to effectively improve the device performance by reducing the trap state densities.[10-13] However, the hydrogenated poly-Si TFTs suffer from an instability issue due to the easily broken weak Si–H bonds.[11] In contrast, the fluorine-ion implantation on poly-Si film can improve the electrical stability of poly-Si TFTs due to the rather strong Si–F bond formation in the poly-Si channel and at the gate dielectric/poly-Si interface.[12,13] Nevertheless, the ion-implantation method has troublesome problems in large-area electronics, and high-temperature annealing is also required to activate implanted fluorine ions and cure implant damages.

Recently, praseodymium oxide (Pr_2O_3) has become a promising high-κ gate-dielectric candidate in metal-oxide-semiconductor field-effect transistors due to its high dielectric constant value of about 31, low gate-leakage current, good dielectric property, and superior thermal stability.[14,15] We have fabricated high-performance poly-Si TFTs using Pr_2O_3 as gate dielectric in a recent study.[16] In this work, we report a fluorine-passivation technique without ion implantation and an additional annealing step by employing a low-temperature CF_4 plasma treatment. The fluorine atoms dissociated from the CF_4 reaction gas can be introduced into the poly-Si film and then passivate the trap states at the grain boundaries. We have integrated a process-compatible fluorine-passivation technique and a high-κ Pr_2O_3 gate dielectric into poly-Si TFTs and investigated their device characteristics and reliability.

Experimental

Figure 1 illustrates the key fabrication steps for the proposed poly-Si Pr_2O_3 TFTs with CF_4 plasma treatments. Briefly, the fabrication began by depositing a 100 mm undoped amorphous silicon (α-Si) layer on a thermally oxidized Si wafer using low-pressure chemical vapor deposition (CVD) at 550°C. The deposited α-Si layer was then recrystallized by the SPC process at 600°C for 24 h in N_2 ambient. The individual active region was patterned and defined. After the RCA clean process, a CF_4 plasma treatment was applied on the recrystallized poly-Si film by plasma-enhanced CVD (PECVD) at 350°C (Fig. 1a). The chamber pressure and flow rate of CF_4 reaction gas were 400 mTorr and 80 sccm, respectively. To investigate the effect of fluorine content on the poly-Si Pr_2O_3 TFT, various radio frequency (rf) powers of 0, 10, and 20 W, with a constant treating time of 20 s, were used to perform the CF_4 plasma

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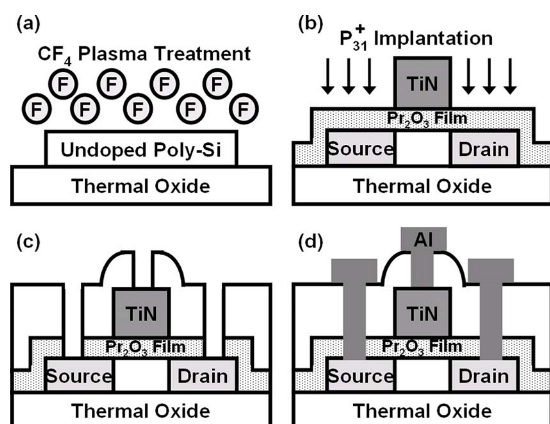

Figure 1. Schematic diagrams of the key fabrication steps for the proposed poly-Si TFT with integrated Pr_2O_3 gate dielectric and CF_4 plasma treatment.

treatment. Afterward, a 33.6 nm Pr_2O_3 film was deposited to serve as the gate dielectric by electron-beam evaporation, followed by a realization of thermal annealing treatment at 600°C for 30 min in O_2 ambient to improve the gate-dielectric quality. After a 200 nm TiN film was deposited, a Cl_2-based dry-etching process capable of stopping on the Pr_2O_3 layer was used to pattern the gate electrode. After a self-aligned phosphorous ion implantation was performed at 80 keV to a dose of 5×10^{15} cm^{-2} to dope the source/drain regions, the dopant was activated by the thermal budget of 600°C for 30 min (Fig. 1b). After a 300 nm passivation SiO_2 layer was deposited by PECVD at 300°C, the contact windows were opened by a two-step wet-etching process. First, the 300 nm passivation SiO_2 layer and the Pr_2O_3 layer were etched away by a buffered oxide etch solution and a H_2SO_4/H_2O_2 mixture solution, respectively (Fig. 1c). Because the H_2SO_4/H_2O_2 mixture solution has a rather high etch selectivity of the Pr_2O_3 thin film to the SiO_2 passivation layer, a Pr_2O_3 film can be completely etched away by excessive overetching. Finally, a typical 400 nm Al metallization completed the fabrication process (Fig. 1d). For comparison, the control poly-Si Pr_2O_3 TFT without the CF_4 plasma treatment, rf power of 0 W, was also prepared with the same process flow. No hydrogen plasma treatment and thermal sintering process were performed to study the fluorine-passivation effects.

Results and Discussion

Figure 2 shows the cross-sectional transmission electron microscopy (XTEM) micrograph of the proposed poly-Si TFT with TiN gate electrode and Pr_2O_3 gate dielectric on the poly-Si channel. The physical thickness of the Pr_2O_3 gate dielectric and the poly-Si channel are around 33.6 and 97 nm, respectively. The higher-resolution TEM micrograph around the Pr_2O_3/poly-Si interface displayed in the inset of Fig. 2 exhibits an about 1.5 nm SiO_2-like interfacial layer between the Pr_2O_3 gate dielectric and poly-Si channel. A metal-oxide-semiconductor (MOS) capacitor on single-crystalline Si was also fabricated to obtain the gate capacitance density of Pr_2O_3 gate dielectric. Figure 3 shows typical capacitance–voltage (C–V) characteristic of the MOS capacitor at 1 MHz. The MOS capacitor has the same gate-dielectric thickness as the proposed TFT device. An accumulation gate capacitance density (C_{acc}) at an applied voltage of $V_{GS} = -4$ V is 532 nF/cm^2. Therefore, the equivalent-oxide thickness (EOT) of the MOS capacitor with Pr_2O_3 gate dielectric extracted from the accumulation gate capacitance density is 6.5 nm. The 6.5 nm EOT is the thinnest thickness reported on TFT studies so far.[17,18] The effective dielectric-constant value of Pr_2O_3 gate dielectric was extracted using the series-capacitor model with a series connection of high-κ and SiO_2-like interfacial layers.[19] The effective dielectric-constant value of Pr_2O_3 film is extracted to be 26.2 by assuming the dielectric-constant value of SiO_2-like interfacial layer to be 3.9. The hyteresis of C–V characteristic is also shown in the

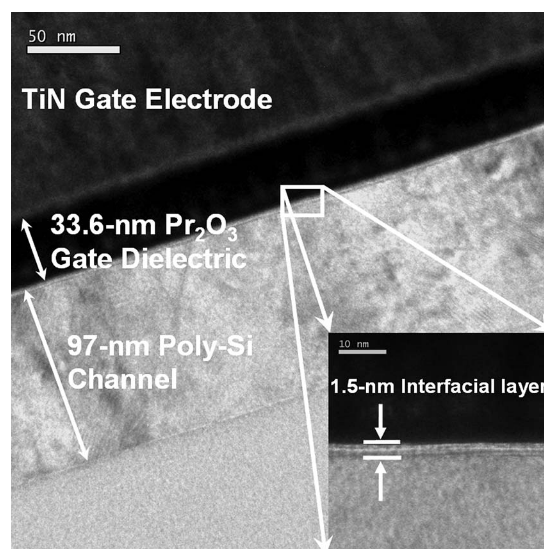

Figure 2. Cross-sectional TEM micrograph of the proposed poly-Si TFT structure.

inset of Fig. 3. The C–V characteristic for hysteresis extraction were measured by sweeping the voltage from accumulation to inversion (−4 to 4 V) and then sweeping back (4 to −4 V). The Pr_2O_3 gate dielectric demonstrates negligible hysteresis characteristic of 5.7 mV, indicating it is a promising gate-dielectric candidate for poly-Si TFT.

Figures 4 and 5 illustrate the transfer characteristics (I_{DS}-V_{GS}) of poly-Si Pr_2O_3 TFTs with various rf powers of 0 (control sample), 10, and 20 W CF_4 plasma treatments, which are measured at V_{DS} = 0.1 and 1 V, respectively. The drawn channel width (W) and channel length (L) are 10 and 10 μm, respectively. The device parameters, including the threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), and subthreshold swing (S.S.), are extracted at $V_{DS} = 0.1$ V. The on/off current ratio (I_{on}/I_{off}) is defined as the ratio of the maximum driving current to the minimum leakage current at V_{DS} = 1 V. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of $I_{DS} = (W/L) \times 100$ nA. The extracted key electrical parameters of the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments are summarized in Table I. The poly-Si Pr_2O_3 TFT with a 10 W CF_4 plasma treatment exhibits better subthreshold and on-state characteristics compared to that without (0 W) and with a 20 W CF_4 plasma treatment. The

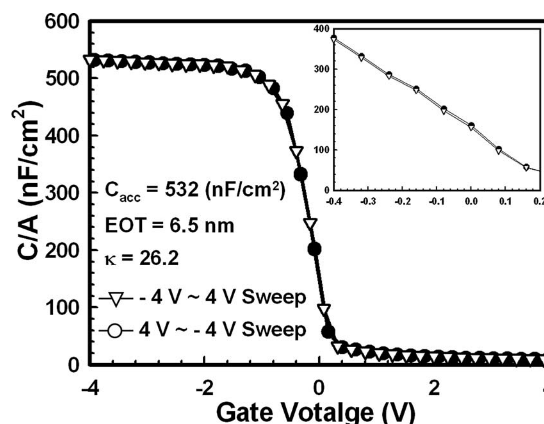

Figure 3. Typical C–V characteristics of the MOS capacitor with a Pr_2O_3 gate dielectric. The inset C–V shows negligible hysteresis characteristics of Pr_2O_3.

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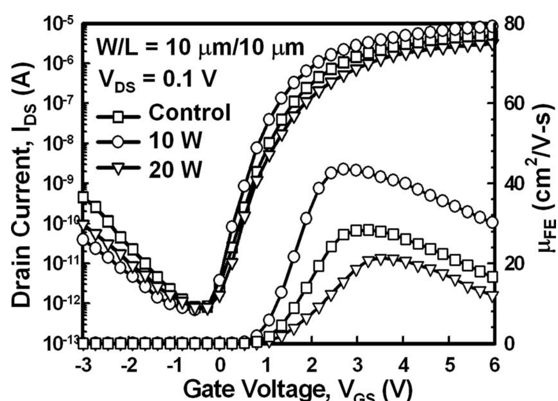

Figure 4. Transfer characteristics of the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments at $V_{DS} = 0.1$ V.

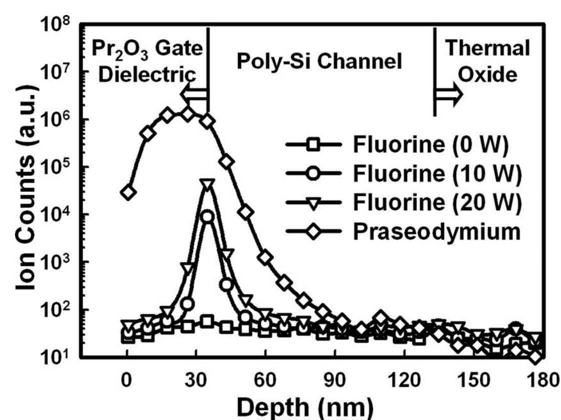

Figure 6. SIMS profiles of fluorine for the poly-Si films with various rf powers of CF_4 plasma treatments.

threshold voltages for the poly-Si Pr_2O_3 TFTs with 0, 10, and 20 W CF_4 plasma treatments are 1.58, 1.27, and 1.93 V, respectively. Also, the S.S. for the poly-Si Pr_2O_3 TFTs with 0, 10, and 20 W CF_4 plasma treatments are 276, 232, and 318 mV/dec, respectively. This tendency indicates that introducing fluorine atoms into the poly-Si layer by an appropriate rf power of 10 W CF_4 plasma treatment can effectively reduce the trap states, leading to a greatly enhanced on-state characteristic.

Although the fluorine passivation of trap states is found to greatly improve the subthreshold and on-state characteristics, the minimum leakage current of the poly-Si Pr_2O_3 TFTs with CF_4 plasma treatments has not been suppressed sufficiently. This observed phenomenon of minimum leakage current is consistent with previously reported data of the poly-Si TFT with fluorine-ion implantation.[12] However, poly-Si TFT with high-κ gate dielectric shows a rather high off-state GIDL current as a consequence of the high electric field enhanced emission via the trap states near the gate-to-drain overlap area.[9] Notably, the maximum GIDL current of the poly-Si Pr_2O_3 TFT with 10 W CF_4 plasma treatment (0.53 nA) is more than one order of magnitude lower than that without CF_4 plasma treatment (control sample) (8.75 nA), especially as the gate voltage continuously decreases to $V_{GS} = -3$ V. In addition, the maximum driving current ($I_{on,max}$) and on/off current ratio of the 10 W CF_4 plasma-treated poly-Si Pr_2O_3 TFT are also superior to those of the 0 and 20 W CF_4 plasma-treated samples. The on/off current ratio of the 10 W CF_4 plasma-treated poly-Si Pr_2O_3 TFT (9.6×10^6) is approximately 2.5 times larger than that of the control sample (3.9×10^6). Therefore, the trap states at the grain boundaries can be effectively passivated by the CF_4 plasma treatment, leading to an improved electrical performance.

Additionally, the field-effect mobility vs gate voltage for the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments is also shown in Fig. 4. The field-effect mobility is extracted from the transconductance measurement at $V_{DS} = 0.1$ V. The maximum field-effect mobility of the poly-Si Pr_2O_3 TFTs with 0, 10, and 20 W CF_4 plasma treatments are 28.33, 43.48, and 21.28 cm^2/V s, respectively. Note that the maximum field-effect mobility is improved by a 10 W CF_4 plasma treatment but degraded by a 20 W CF_4 plasma treatment. This result also confirms that the fluorine atoms incorporated by an appropriate rf power of 10 W CF_4 plasma treatment provide a passivation effect of Si dangling bonds and Si strain bonds in the poly-Si channel and at the Pr_2O_3/poly-Si interface.

Evidence of fluorine incorporation in the poly-Si film can be firmly demonstrated with secondary ion mass spectroscopy (SIMS) analysis. Figure 6 shows the SIMS profiles of fluorine atoms for the poly-Si films with 0, 10, and 20 W CF_4 plasma treatments. It was clearly observed that considerable fluorine atoms were detected in the poly-Si and, in particular, an obvious fluorine peak was located at the Pr_2O_3 gate dielectric/poly-Si channel interface. The SIMS analysis shows an increased concentration of fluorine atoms at the Pr_2O_3/poly-Si interface with increasing rf power. Note that the piled-up fluorine atoms at the Pr_2O_3/poly-Si interface using CF_4 plasma treatment provide an effective termination of trap states.

To verify the fluorine passivation of grain-boundary trap states by using CF_4 plasma treatment, the effective grain-boundary trap-state density was evaluated according to the grain-boundary trapping model proposed by Levinson and Proano.[20,21] Figure 7 exhibits the $\ln[I_{DS}/(V_{GS}-V_{FB})]$ vs $1/(V_{GS}-V_{FB})^2$ curves in the strong inversion at $V_{DS} = 0.1$ V for the poly-Si Pr_2O_3 TFTs with 0, 10, and 20 W CF_4 plasma treatments. The effective grain-boundary trap-state density was calculated from the square root of the slope of $\ln[I_{DS}/(V_{GS}-V_{FB})]$ vs $1/(V_{GS}-V_{FB})^2$. For the cases of the applied rf power =0, 10, and 20 W, the effective grain-boundary trap-state densities are found to be 1.35×10^{13}, 9.44×10^{12}, and 1.47×10^{13} cm^{-2}, respectively. It is observed that there is an optimal rf

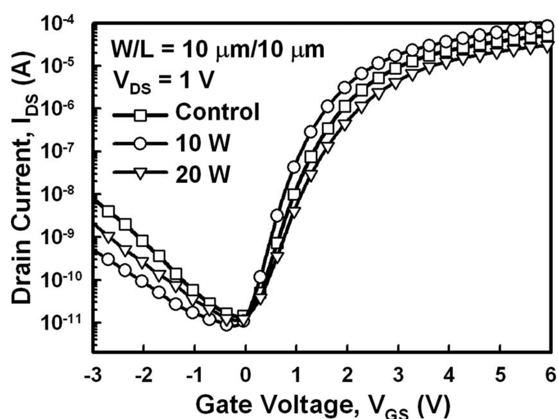

Figure 5. Transfer characteristics of the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments at $V_{DS} = 1$ V.

Table I. Key device parameters for poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

Sample	V_{TH} (V)	S.S. (mV/dec)	μ_{FE} (cm^2/Vs)	$I_{on,max}$ (μA)	I_{on}/I_{off} (10^6)
Control	1.58	276	28.33	53	3.9
10 W	1.27	232	43.48	86	9.6
20 W	1.93	318	21.28	31	2.7

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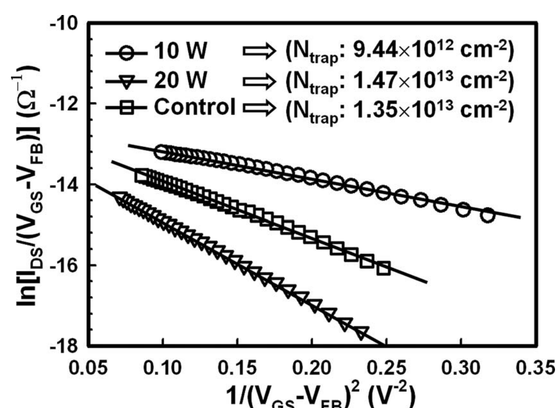

Figure 7. Plot of $\ln[I_{DS}/(V_{GS}–V_{FB})]$ vs $1/(V_{GS}–V_{FB})^2$ under strong inversion at $V_{DS} = 0.1$ V for poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

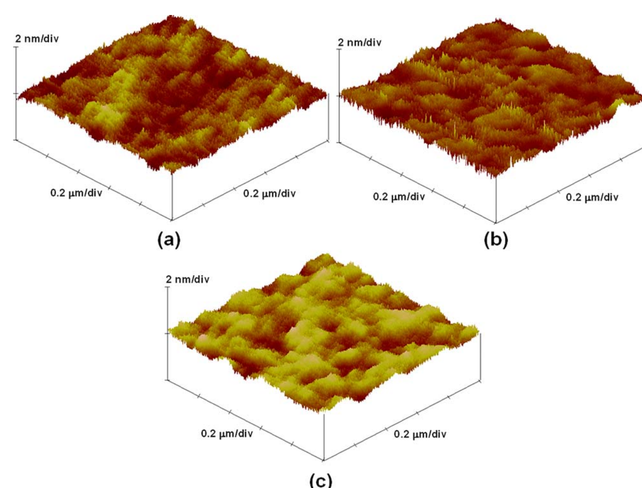

Figure 8. (Color online) AFM images of poly-Si films with various rf powers of (a) 0 (control), (b) 10, and (c) 20 W CF_4 plasma treatments. The corresponding rms values of poly-Si surface roughness are 0.25, 0.31, and 0.47 nm, respectively.

power of 10 W CF_4 plasma treatment for the reduction of grain-boundary trap states. Although the 20 W sample has a higher concentration of fluorine atoms than the 10 W sample, as shown in the SIMS profiles, the effective grain-boundary trap-state density is slightly increased by increasing the rf power to 20 W.

To further investigate the fluorine passivation of the interface trap states near the Pr_2O_3 gate dielectric/poly-Si interface, the effective interface trap-state densities (N_{it}) were calculated from the S.S.[22] N_{it} can be expressed as Eq. 1 without considering the depletion capacitance

$$N_{it} = \left[\left(\frac{\text{S.S.}}{\ln 10}\right)\left(\frac{q}{kT}\right)\right]\left(\frac{C_{acc}}{q}\right) \qquad [1]$$

where C_{acc} is the gate capacitance density of Pr_2O_3 gate dielectric. The N_{it} values for the 0, 10, and 20 W CF_4 plasma-treated poly-Si Pr_2O_3 TFTs are 1.49, 1.25, and 1.71×10^{13} cm^{-2}, respectively. This result reveals that the interface trap states near the gate dielectric/poly-Si interface could be greatly passivated by using an appropriate rf power of 10 W CF_4 plasma treatment, leading to improved device performance. Combined with the SIMS profiles, we believe that the passivation effect is due to the accumulated fluorine atoms at the Pr_2O_3/poly-Si interface.

However, there is a nonideal result; the 20 W CF_4 plasma treatment on poly-Si film shows a detrimental effect on the electrical performance of the fabricated TFT device. As is well known, CF_4 gas dissociated into reactive fluorine radicals by rf gas discharge is a commonly used etching species, thereby etching the exposed poly-Si film.[23] The reason for the degradation of electrical performance may be attributed to the plasma-etching-induced electrical damage to the poly-Si film. The effect of degradation of poly-Si film completely dominates the effect of fluorine passivation of trap states for the 20 W CF_4 plasma treatment, resulting in a degraded electrical performance. Fortunately, the variations of thickness of the poly-Si films before and after CF_4 plasma treatments measured by ellipsometer were negligible. Therefore, the thinning effect of the poly-Si films by CF_4 plasma treatment is excluded. According to previous reports, the roughness of the gate dielectric/poly-Si interface has been reported to affect the on-state characteristic of the TFT device.[24] The electrical characteristics and reliability of the gate dielectric are also correlated with the surface morphology of poly-Si film.[25] To investigate the degradation of the on-state characteristic for the 20 W CF_4 plasma-treated sample, the surface morphology of poly-Si films is analyzed by atomic force microscopy (AFM). Figures 8a-c show the AFM images for the poly-Si films with 0, 10, and 20 W CF_4 plasma treatments, respectively. The average root-mean-square (rms) values for poly-Si roughness with 0, 10, and 20 W CF_4 plasma treatments were 0.25, 0.31, and 0.47 nm, respectively. Clearly, the poly-Si film with a 20 W CF_4 plasma treatment shows a rougher surface morphology, leading to more damage to the integrity of the poly-Si channel film. The plasma-etching-induced damage to the poly-Si film becomes more obvious with increasing rf power to 20 W. The effect of increasing surface roughness completely dominates the effect of fluorine passivation of trap states, thereby leading to the degraded electrical characteristics.

Figure 9 shows the activation energy (E_A) of the drain current as a function of the gate voltage at $V_{DS} = 0.1$ V for the poly-Si Pr_2O_3 TFT without (0 W) and with 10 and 20 W CF_4 plasma treatment. Measurements of the I_{DS}–V_{GS} characteristics are performed on all the devices for temperatures varying from 25 to 150°C in order to extract the variations of the activation energy of the drain current.[26] The value of E_A reflects the carrier-transport barrier of the grain boundary within the poly-Si channel; the higher the E_A in the turn-off state, the higher the carrier-transport barrier of the grain boundary. An optimal rf power of 10 W CF_4 plasma treatment can greatly passivate the trap states to reduce the off-state GIDL current and hence exhibit the highest E_A in the off state. The implication is consistent with the above extracted data of trap-state density.

Finally, the influence of electrical stress on poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments is examined. Figures 10 and 11 show the threshold voltage shift and variation of on current as a function of hot-carrier stress time for the poly-Si Pr_2O_3 TFTs with 0, 10, and 20 W CF_4 plasma treatments. The TFT devices

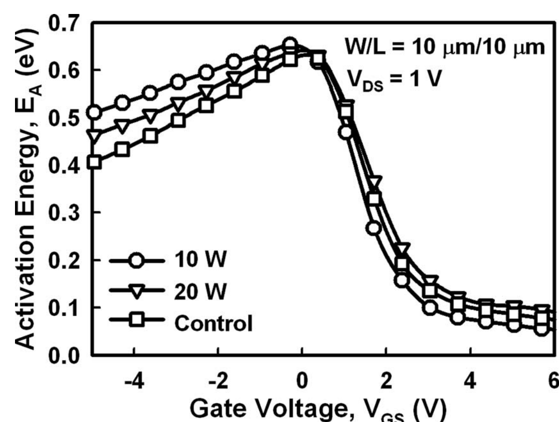

Figure 9. Activation energy (E_A) of the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

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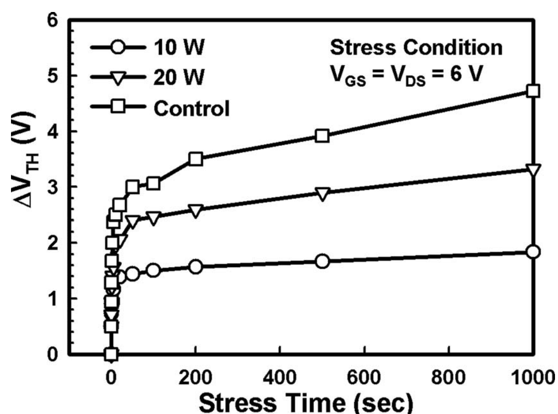

Figure 10. Threshold voltage shift vs hot-carrier stress time for poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

were bias-stressed at room temperature under $V_{GS} = 6$ V and $V_{DS} = 6$ V. The V_{TH} shift and variation of I_{on} were defined as $(V_{TH,stressed}–V_{TH,initial})$ and $(I_{on,stressed}–I_{on,initial})/I_{on,initial} \times 100\%$, respectively, where the index of the initial and stressed represent the extracted values before and after stresses. The TFT devices with CF_4 plasma treatments show smaller V_{TH} shift and variation of I_{on} than that without CF_4 plasma treatment. Notably, the V_{TH} shift and variation of I_{on} of poly-Si Pr_2O_3 TFT with 10 W CF_4 plasma treatment are found to be 1.84 V and 16.06% after 1000 s stress, which are superior to those without CF_4 plasma treatment (4.72 V and 38.34%, respectively). It has been reported that the degradation of electrical characteristics under hot-carrier stress is attributed to the following two conditions: the generation of gate dielectric/poly-Si interface states and the easily broken weak Si–Si and Si–H bonds in the poly-Si channel.[13,14] Thus, introducing fluorine atoms into the poly-Si film by CF_4 plasma treatment would result in the passivation of trap states and the formation of stronger Si–F bonds in place of the weak Si–Si and/or Si–H bonds, exhibiting superior endurance against hot-carrier stress.

Conclusion

We have fabricated and characterized the fluorine-passivation effect on poly-Si TFTs incorporating high-κ Pr_2O_3 as gate dielectric. Poly-Si TFT with Pr_2O_3 gate dielectric can obtain thin EOT and high gate capacitance density. A process-compatible fluorine passivation of trap states by employing a low-temperature CF_4 plasma treatment on poly-Si film is proposed. The incorporation of fluorine atoms into the poly-Si film using CF_4 plasma treatment is demonstrated with SIMS analysis and reduction of trap-state density. The electrical characteristics of the 10 W CF_4 plasma-treated poly-Si Pr_2O_3 TFT, including threshold voltage, off-state GIDL current, field-effect mobility, and on/off current ratio, are improved compared with those of the control TFT. For higher rf power of the 20 W CF_4 plasma treatment, the electrical performances of the TFT device are degraded, resulting from the CF_4 plasma-etching-induced damage to the poly-Si surface. In addition, the incorporation of fluorine atoms also promotes hot-carrier immunity. The improvement is a result of the fluorine passivation, which reduces trap-state density and forms stronger Si–F bonds in place of the weak Si–H bonds in the poly-Si channel and at the Pr_2O_3 gate dielectric/poly-Si interface.

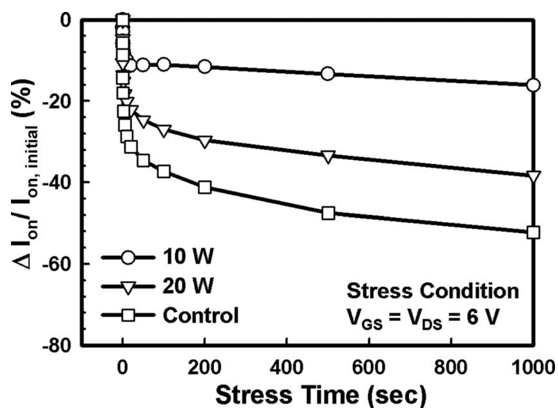

Figure 11. Variations of on current vs hot-carrier stress time for poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

Acknowledgments

The authors acknowledge apparatus support from National Nano Device Laboratories (NDL) and financial support by the National Science Council (NSC) under contract no. NSC 95-2221-E-009-279.

National Chiao Tung University assisted in meeting the publication costs of this article.

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