Electrical Characteristics of the HfAlON Gate Dielectric With Interfacial UV-Ozone Oxide

Yung-Yu Chen, Wen-Yu Fu, and Ching-Fa Yeh

***Abstract*—In this letter, the electrical properties of a HfAlON dielectric with UV-O_3 interfacial oxide were comprehensively studied and then compared with those of a HfAlON dielectric with interfacial chemical oxide. In the comparison of dielectric characteristics including leakage current density, transconductance, subthreshold swing, saturation drain current, effective electron mobility, and constant voltage stress reliabilities, the results clearly indicate that high-density interfacial UV-O_3 oxide is beneficial in reducing both bulk and interface traps as well as diminishing stress-induced trap generation, and possesses a high potential to be integrated with further high-κ dielectric applications.**

***Index Terms*—HfAlON, high-κ dielectric, ozone oxide.**

I. Introduction

THE SHRINKAGE in MOSFET dimensions is accompanied by a scaling of gate oxide thickness. It is well known that the scaling of conventional silicon dioxide (SiO_2) is approaching the predicted limit due to large direct tunneling leakage current, thereby presenting a fundamental challenge to continual scaling [1]. Therefore, an alternative gate dielectric material is needed to replace SiO_2. High-permittivity (high-κ) dielectrics are potential candidates, because a thicker film can be utilized to reduce the direct tunneling leakage current while maintaining the same gate capacitance [2]–[4]. However, direct deposition of high-κ dielectrics on silicon surface will inevitably deteriorate device performances and reliability characteristics [5]. As a result, the control of a SiO_2-like interface between high-κ dielectrics and silicon substrate becomes more and more important since the device performances and reliability characteristics are strongly affected by the interface quality [5]. Therefore, surface treatments prior to the high-κ deposition are considered to be necessary in order to enhance the capabilities of the high-κ gate stack.

Recently, ozone oxide has been grown as the interfacial layer between high-κ dielectrics and Si substrate to improve interface quality [2], [6]–[8]. The growth of the ozone oxide occurs in a layer-by-layer manner, with a thinner transition layer as well as high oxide density comparable to that of a thick thermal oxide [7]. In this letter, the effect of a hafnium–aluminum–oxynitride (HfAlON) dielectric with interfacial oxide grown in the ozone (O_3) ambient with UV lamp irradiation at room temperature, compared with chemical oxide grown in $HCl/H_2O_2/H_2O$ solution, had been systematically surveyed through electrical measurements and reliability evaluation.

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II. Experiment

A standard local oxidation of silicon process was applied for device isolation. n-Channel MOSFETs (nMOSFETs) were fabricated on 4-in p-type (100) Si wafers that utilize a conventional self-align process. After standard RCA cleaning, a 3-nm HfAlON dielectric was deposited by reactive cosputtering hafnium (Hf) and aluminum (Al) targets in $Ar/N_2/O_2$ at room temperature on either 1-nm chemical oxide or 0.8-nm UV-ozone oxide (UV-O_3 oxide), followed by postdeposition annealing (PDA) at 900 °C for 30 s in the N_2 ambient. The chemical oxide was formed by the $HCl/H_2O_2/H_2O$ solution after removal of the sacrificial oxide using a 5% diluted hydrofluoric acid. The UV-O_3 oxide was grown in O_3 ambient with UV lamp irradiation at room temperature. A 200-nm polysilicon gate was then deposited on the HfAlON gate stack at 620 °C by low-pressure chemical vapor deposition system using silane (SiH_4) gas. Following a gate-patterning step, 20-keV phosphorous was implanted at a dose of 5×15 cm^{-2}. Dopant activation was performed by rapid thermal annealing at 950 °C for 30 s in a N_2 ambient. Equivalent oxide thickness (EOT) was obtained from the high-frequency (100 kHz) capacitance–voltage (C–V) measurement using a Hewlett-Packard (HP) 4284 inductance–capacitance–resistance meter at the inversion region, without calculating quantum effect. The electrical properties were measured using an HP 4156C semiconductor parameter analyzer. Interface state density N_{it} conversion was evaluated from the charge-pumping method. A varied rise time/fall time square-wave waveform (1 MHz) generated from an HP 81110A was applied to the gate electrode while source/drain and body were grounded. The base voltage was varied from accumulation to inversion while keeping the pulse amplitude at 1.5 V.

III. Result and Discussion

Fig. 1 plots the C–V curves of the HfAlON nMOSFET with interfacial UV-O_3 oxide or chemical oxide. The extracted EOT at the inversion region $\mathrm{EOT_{inv}}$ was 2 and 2.02 nm for the HfAlON dielectric with interfacial UV-O_3 oxide and that with chemical oxide, respectively. Since the interfacial UV-O_3 oxide was thinner than the chemical oxide, the slightly higher

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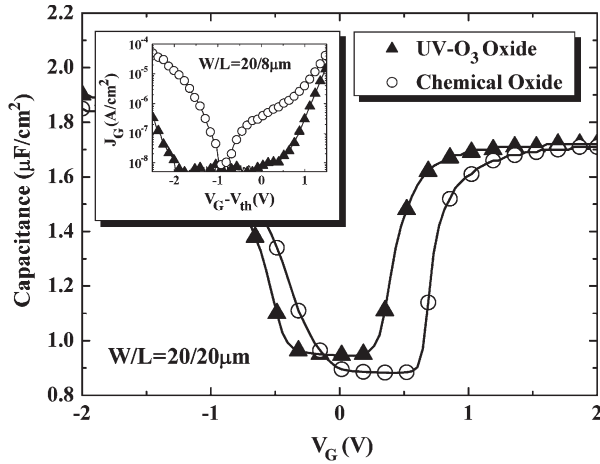

Fig. 1. C–V curves and gate leakage current density of the HfAlON nMOSFET with interfacial UV-O_3 oxide or chemical oxide.

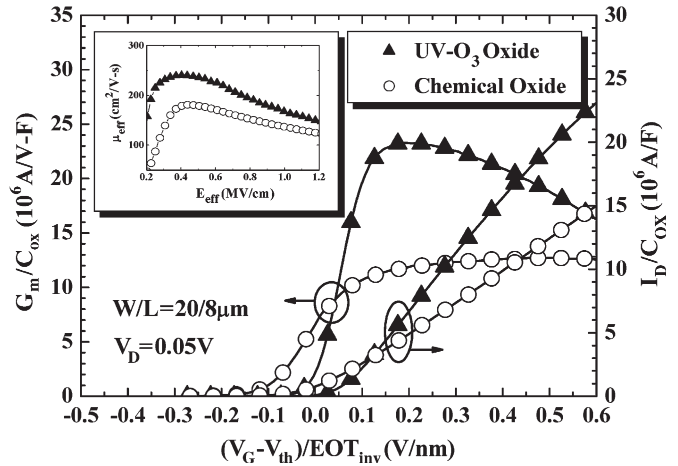

Fig. 2. Transconductance G_m and subthreshold characteristics of the HfAlON nMOSFET with interfacial UV-O_3 oxide or chemical oxide. The inset also shows the corresponding electron effective mobility μ_{eff}.

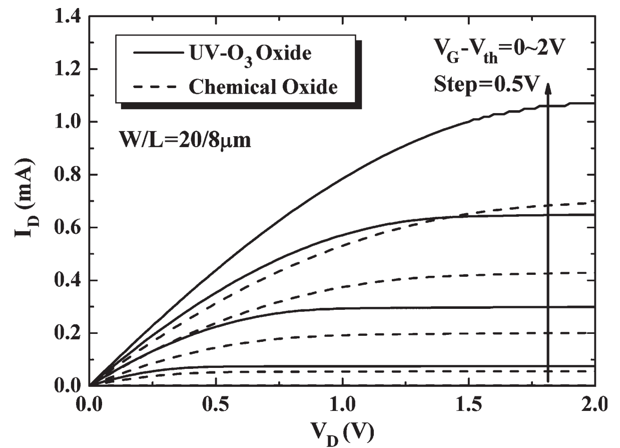

Fig. 3. I_D–V_D characteristics of the HfAlON nMOSFET with interfacial UV-O_3 oxide or chemical oxide.

EOT_{inv} for the HfAlON dielectric with interfacial chemical oxide should be due to further interfacial reaction during high-κ deposition and, subsequently, high-temperature PDA. The HfAlON dielectric with interfacial UV-O_3 oxide also exhibited both a smaller interface trap density N_{it} and oxide trap density N_{ot} than that with chemical oxide, which can be inferred from a steeper C–V curve near flatband and a smaller flatband voltage V_{fb}. Moreover, the C–V hysteresis, which was evaluated using the V_{fb} shift between two different sweep directions, can be reduced from 15 mV for the HfAlON dielectric with interfacial chemical oxide to 4 mV for the device with interfacial UV-O_3 oxide, which also showed that interfacial UV-O_3 treatment can suppress the trapped charge density within the HfAlON gate stack. The gate leakage current density of the HfAlON nMOSFET with interfacial UV-O_3 oxide or chemical oxide is shown in the inset. Even with slightly thinner EOT_{inv}, the HfAlON dielectric with interfacial UV-O_3 oxide can reduce leakage current that is larger than one order of magnitude, particularly, at low gate voltage, as compared with the HfAlON dielectric with interfacial chemical oxide.

Fig. 2 exhibits the typical transconductance G_m and subthreshold characteristics of the nMOSFET with HfAlON stacked gate dielectric. The HfAlON dielectric with interfacial UV-O_3 oxide clearly had a significant improvement in peak G_m and subthreshold swing (SS). Peak G_m can be increased larger than two times in HfAlON nMOSFET while replacing chemical oxide with UV-O_3 oxide. The SS can be reduced from 114 mV/dec for the HfAlON dielectric with interfacial chemical oxide to 83 mV/dec for the device with interfacial UV-O_3 oxide, which also showed that UV-O_3 treatment can improve the interface properties of the HfAlON gate stack. The N_{it} measured by the charge-pumping method was 2.5×10^{11} and 7.3×10^{10} cm^{-2} for the HfAlON dielectrics with interfacial chemical oxide and UV-O_3 oxide, respectively (not shown), and consisted of the C–V curves and subthreshold characteristics shown in Figs. 1 and 2. Hence, the apparent subthreshold behavior $(V_G - V_{\text{th}} < 0)$ for the HfAlON dielectric with interfacial chemical oxide was believed to be mainly due to poor interfacial quality (large interfacial trapped charges, large SS, and high gate leakage current). The extracted effective electron mobility μ_{eff} from the split C–V method is compared in the inset. As can be seen, mobility improvement of nearly 30% was obtained in the HfAlON nMOSFET with interfacial UV-O_3 oxide compared to the device with interfacial chemical oxide. This suggested that UV-O_3 interfacial oxide growth prior to the HfAlON dielectric deposition was beneficial to reduce as-deposited trap density within the gate stack, which was partially due to reduced plasma damage during sputtering and reduced interfacial reaction during 900 °C PDA.

Fig. 3 measures the well-behaved output I_D–V_D characteristics of the HfAlON nMOSFET with interfacial UV-O_3 oxide or chemical oxide. It is confirmed that the saturation drain current can be increased to be larger than 50% for the HfAlON nMOSFET with interfacial UV-O_3 oxide compared to the device with interfacial chemical oxide. The generated interface trap density ΔN_{it} and oxide trap density ΔN_{ox} for the nMOSFET with HfAlON stacked gate dielectric during constant voltage stress (CVS) at $V_G - V_{\text{th}} = 1$ V are shown in Fig. 4, where ΔN_{it} was extracted from the charge-pumping current increment and ΔN_{ox} was calculated from the difference between the total trap charge density (deduced from the threshold voltage V_{th} shift) and the interface trap density.

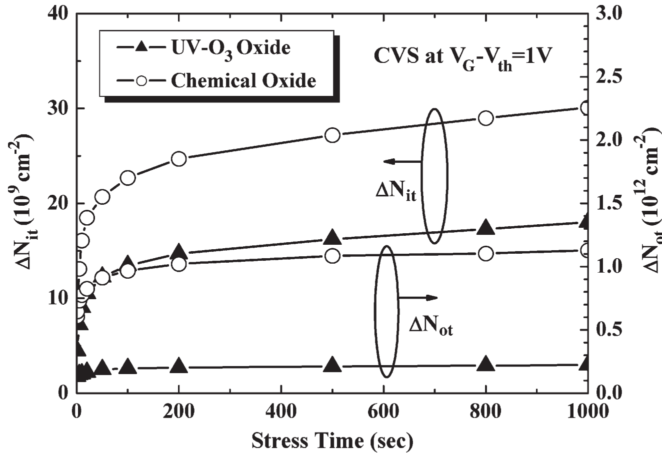

Fig. 4. Generated interface trap density $\Delta N_{\rm it}$ and oxide trap density $\Delta N_{\rm ot}$ of the HfAlON nMOSFET with interfacial UV-O_3 oxide or chemical oxide during CVS at $V_G - V_{\rm th} = 1$ V.

The increment of $N_{\rm it}$ and $N_{\rm ot}$ for the device with interfacial chemical oxide is much larger than that for the device with interfacial UV-O_3 oxide. In addition, trap generation during CVS was preferred to be within the HfAlON dielectric rather than at the interface, implying that the dielectric reliabilities at low stress voltage would be dominated by the bulk properties of the HfAlON gate stack.

The superior electrical characteristics of the HfAlON dielectric with interfacial UV-O_3 oxide can be explained by the high oxide density [7]. The UV-O_3 oxide had comparable oxide density as thick thermal oxide and less interfacial suboxide states [7], which was helpful in reducing both as-deposited $N_{\rm it}$ and $N_{\rm ot}$ as well as diminishing stress-induced trap density generation. Moreover, high oxide density had been inferred to reduce plasma damage during reactive sputtering, suppress further interfacial reaction during HfAlON dielectric deposition and postdeposition high-temperature annealing, and result in a smoother interface [8]. Superior electrical characteristics and dielectric reliabilities were therefore obtained for the HfAlON dielectric with interfacial UV-O_3 oxide.

IV. Conclusion

As compared to those of the HfAlON nMOSFET with interfacial chemical oxide, the electrical properties of the HfAlON nMOSFET with interfacial UV-O_3 oxide were comprehensively studied. The HfAlON nMOSFET with interfacial UV-O_3 oxide exhibits leakage current reduction of nearly one order of magnitude, negligible C–V hysteresis, electron mobility of larger than 30%, and saturation drain current increment as well as diminishing interface and oxide trap generation, mainly due to high oxide density, compared to that with chemical oxide. The results clearly indicate that high-density interfacial UV-O_3 oxide is beneficial in improving the electrical characteristics of the HfAlON gate dielectric and possesses a high potential to be integrated with further high-κ dielectric applications.

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